Design Methodology for Power-Constrained Low Noise RF Circuits

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Four Noise Parameters

- Minimum Noise Factor ($F_{min}$) : Best achievable noise performance
- Optimum Source Admittance ($Y_{opt}$) : Source admittance yielding $NF_{min}$
- Equivalent Noise Resistance ($R_n$) : Sensitivity of $NF$ when $Y_s$ differs from $Y_{opt}$

$$F = F_{min} + \frac{(Y_s - Y_{opt})^2}{G_s} R_n$$

Desired to be:
- Low $F_{min}$
- Small $R_n$
- $Y_s \approx Y_{opt}$
Integrated LNA Design
(Tuned LNA Architecture)

Basic Architecture

Conjugate Power Match

Off-Chip Matching

Controls noise performance. Why?
Integrated LNA Design (Continue) (Power Matched Design)

\[ F = F_{\text{min}} + \frac{(Y_s - Y_{\text{opt}})^2 R_n}{G_s} \]

\[ M_1 = 100/0.24 \]
\[ M_2 = 50/0.24 \]
\[ V_{DS1} = 2.5V \]
\[ V_{GS1} = 0.8V \]
\[ f = 4GHz \]

\[ Z_{\text{opt, best}} \]
\[ Z_{\text{conj, best}} \]

\[ NF_{LNA} \]
\[ NF_{\text{min, LNA}} \]

\( M_2 \) contribution is excluded.
Integrated LNA Design (Continue)
(Power Matched Design)

❖ Optimum $L_s$ is bias dependent and linearly scaled by the current specification.

❖ The achievable noise figure is independent of the current specification and quite close to the intrinsic $NF_{min}$.

*M_2* contribution is excluded.
Integrated LNA Design (Continue)
(Power Constrained Performance, $Z_s = Z_{in} = 50\Omega$)

Optimum Impedance ($Z_{opt}$)

Matched Cascode

Mismatched Cascode

$$F = F_{min} + \frac{(Y_s - Y_{opt})^2 R_n}{G_s}$$
Integrated LNA Design (Continue)
(Power Constrained Performance, $Z_s=Z_{in}=50\Omega$)

**Noise Resistance ($R_n$)**

![Graph showing noise resistance vs. gate bias of $M_1$]

**Noise Figure ($NF$)**

![Graph showing noise figure vs. gate bias of $M_1$]

\[
F = F_{min} + \left(\frac{Y_s - Y_{opt}}{G_s}\right)^2 R_n
\]
Integrated LNA Design (Continue)

(Impact of Pad Capacitance, $Z_s=Z_{in}=50\Omega$)

**Optimum Impedance ($Z_{opt}$)**

**Noise Resistance ($R_n$)**

\[ F = F_{min} + \frac{(Y_s - Y_{opt})^2 R_n}{G_s} \]
Integrated LNA Design (Continue)
(Impact of Pad Capacitance, $Z_s=Z_{in}=50\Omega$)

**Noise Figure (NF)**

- $W_2 = W_1/2$
- $V_{DD} = 2.0\,\text{V}$
- $f = 800\,\text{MHz}$
- $I_{DD} = 3.75\,\text{mA}$

**Gain ($s_{21}$)**

- $W_2 = W_1/2$
- $V_{DD} = 2.0\,\text{V}$
- $f = 800\,\text{MHz}$
- $I_{DD} = 3.75\,\text{mA}$
LNA Implementation (Continue)
(Implementation, \( Z_s = Z_{\text{in}} = 50\Omega \))

- 800MHz single-ended
- 0.24\(\mu\)m, silicided-poly, 5-metals
- \( W_1 = 90, \ W_2 = 45 \) (not optimized)
- 5\(\mu\)m-long gate fingers
- M5 spiral inductors w/ patterned ground shield
- M5/M1 pad capacitors
- 24-pin LLP package
- An off-chip inductor for \( L_g \)
LNA Implementation (Continue)
(Performance)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Measured Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>800 MHz</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>2.0 V</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>7.5 mW</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>0.9±0.2 dB</td>
</tr>
<tr>
<td>Available Gain</td>
<td>8.8 dB</td>
</tr>
<tr>
<td>$s_{11}$</td>
<td>-38.1 dB</td>
</tr>
<tr>
<td>IIP3</td>
<td>7.1 dBm</td>
</tr>
<tr>
<td>Die Area</td>
<td>0.19 mm$^2$</td>
</tr>
</tbody>
</table>

Just adds 0.3dB to $NF_{min}$
Conclusions

❖ Overall $NF$ is controlled by $L_s$: Optimal $L_s$ achieves $NF$ close to intrinsic $NF_{min}$ with a perfect power match.

❖ For a fixed $Z_s$, simultaneous choice of $V_{gs}$ and width of input stage is most critical in design.

❖ Mismatched cascode stage determines the lower limit of noise figure.

❖ Pad capacitance provides another design flexibility.

❖ CMOS LNA can be competitive with GaAs and Bipolar in low GHz range.