Gate Bias Induced Heating Effect and Implications for the Design of Deep Submicron ESD Protection

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Purpose

- To investigate the impact of gate bias on ESD protection:
  Why does ESD performance degrade with high gate bias?

- To establish design guidelines that would be important for the ESD protection circuit designs
Typical ESD protection design for Output Buffer

NMOS options

Excessive gate coupling may occur for output NMOS with Vdd charging through the diode
Introduction

- Under ESD conditions with high gate bias (excess gate coupling), the failure threshold current of the NMOS is known to degrade

Polgreen et al., TED. 1992
Chen et al., EOS/ESD Symp. 1997
Introduction

- Degradation is technology dependent and its impact on protection designs have not been fully explored

- For advanced technologies, ESD strength degradation with high gate bias seems to depend on the finger width

- The finger width and substrate bias also determine the conduction uniformity and are important for overall protection design

Oh et al., IRPS 2001
Second Breakdown Triggering Current ($I_{t2}$) with $V_{gs}$ for silicided NMOS

Beyond 0.35μm tech.

- $I_{t2}$ degradation doesn’t follow the $I_{sub}$ with low $V_{gs}$

$\Rightarrow$ Implying new physical mechanism

Need to identify main cause of this degradation for robust design of ESD protection
Output NMOS Failure

2KV Human Body Model (HBM)
Test Simulation

I_{HBM} [A]

High current I-V

V_h

V_d

M1= 400/0.25
M3= 50/0.25
M5=M7=10/0.25

M2= 100/0.25
M4=M6=20/0.25
**Under HBM ESD stress, gate potential \((V_n)\) of output NMOS may be higher than \(V_g\), depending on the pre-drive circuit conditions**

→ **Output NMOS weaker than Protection NMOS**

- **Case 1**: \(n_1, n_2, p_1, \& p_2 \rightarrow \text{GND}\)
- **Case 2**: \(n_1, n_2 \rightarrow \text{GND} \quad p_1, p_2 \rightarrow V_{dd}\)
Failure of output NMOS due to excess gate coupling

Failure of NMOS in HBM test

High gate coupling lowers ESD strength, output NMOS fails earlier than the protection device

Significantly reduces the effectiveness of the ESD protection design
Experiments

Transmission Line Pulsing (TLP) Test for 1.5V & 3.3V NMOS for 0.13 μm tech.
$I_t2$ with $V_{gs}$

- Impact of $V_{gs}$ on $I_t2$ depends on $W_F$ despite different process and gate structures
Width dependence of $I_{t2}$ degradation

- $I_{t2}$ improved for wide NMOS with $V_{gs}$
- $I_{t2}$ reduced for narrow NMOS with $V_{gs}$
  → implying two competing mechanisms depending on $W_F$

- For advanced silicided wide finger width NMOS, $I_{ESD}$ is non-uniform

$V_{gs}$ effects are influenced by the extent of lateral uniformity of $I_{ESD}$
Non-Uniform $I_{\text{ESD}}$ Conduction

Non-uniform $I_{\text{ESD}}$ conduction for the 0.13$\mu$m Technology

$I_{\text{ESD}}$ distribution by EMMI (3.3V NMOS)
Simulations and Analysis

Mixed Mode Transient Simulation (@ t=10ns)

$I_{ESD} = 10 \text{mA/\mu m}$

$L_{poly} = 0.175 \text{ \mu m}$

$I$-V with time

$I$-V curve

$V_{t1}$
Current density modulated by $V_{gs}$ within channel area $\rightarrow$ local temperature changes.
As $V_{gs}$ increases, temperature distribution more localized as well as $T_{peak}$ gets higher.
In addition, location of $T_{\text{peak}}$ moves closer to the surface with $V_{gs}$

$\rightarrow$ more vulnerable to surface damage
Impact of $V_{\text{sub}}$

- The turned on width increases with $V_{\text{sub}}$ and $I_{E\text{SD}}$ flows deeper into the substrate.
Compensate for degradation of $I_{t2}$ with $V_{gs}$

$V_{gs} = 3V$

$T_{peak}$

$V_{sub} = 0V$

$V_{sub} = 1V$

$V_{gs}$ induced heating can be alleviated with $V_{sub}$
Two competing mechanisms of gate bias effect depending on $W_F$

For $W_F$ where $I_{ESD}$ is uniform $V_{gs}$ induced heating degrades $I_{t2}$

Impact of $V_{sub}$ on reduction of $I_{t2}$ with $V_{gs}$
Implications for ESD Protection

Design Window for High Performance ESD Protection Devices

- $V_{gs}$ effect
- Gate-coupled NMOS
- Gate-grounded NMOS
- $V_{sub} > 0V$
  - Compensate for adverse

Uniformity:
- $I_{ESD}$
- $W_{eff} = W_{F}$
- $W_{crit} = W_{crit}$

Non-uniformity:
- $I_{ESD}$
- $W_{eff} = W_{crit}$
- $W_{F}$
Design Consideration

- For the substrate trigger protection, \textit{ggNMOS} can be used with $V_{\text{sub}}$
- For \textit{gcNMOS} without $V_{\text{sub}}$, the gate should be designed with $R$ & $C$ to maintain gate bias below $I_{t2}$ roll-off
- For the output \textit{NMOS}, size should be carefully determined according to gate-coupling level (since no $V_{\text{sub}}$ is available and gate-coupling is unpredictable)
Summary

- Investigated $I_{t2}$ degradation with $V_{gs}$ for advanced ESD protection design
- Gate bias induced heating effect is the root cause of $I_{t2}$ reduction with $V_{gs}$
- Improved understanding and provided new insight into ESD protection
- Also, showed $V_{sub}$ can compensate for the adverse $V_{gs}$ effect
- Presented design windows for efficient and robust ESD protection