# Numerical Study of Flicker Noise in p-Type $Si_{0.7}Ge_{0.3}/Si$ Heterostructure MOSFETs

Chia-Yu Chen, *Student Member, IEEE*, Yang Liu, *Member, IEEE*, Robert W. Dutton, *Fellow, IEEE*, Junko Sato-Iwanaga, Akira Inoue, and Haruyuki Sorada

***Abstract*—Device-level simulation capabilities have been developed to investigate low-frequency noise behavior in p-type $Si_{0.7}Ge_{0.3}/Si$ heterostructure MOS (SiGe p-HMOS) transistors. The numerical model is based on the impedance field method; it accounts for a trap-induced carrier number fluctuation, a layer-dependent correlated mobility fluctuation, and a Hooge mobility fluctuation in the buried and parasitic surface channels, respectively. Simulations based on such models have been conducted for SiGe p-HMOS transistors, and the results have been carefully correlated with experimental data. Quantitative agreement has been obtained in terms of the noise level dependence on gate biases, drain currents, and body biases, revealing the important role of the dual channels in the low-frequency noise behavior of SiGe p-HMOS devices.**

***Index Terms*—Flicker noise, heterostructure, MOSFETs, SiGe, 1/f noise.**

## I. Introduction

THE SUPPRESSION of low-frequency noise in active transistors is highly desirable in various analog/RF circuit applications. As the FET technologies continue to scale, their impact on device low-frequency noise performance needs to be carefully evaluated. Such effects can come from size (channel length/width) scaling, adoption of advanced doping profiles (pocket implantation), or incorporation of alternative gate and channel materials (high-$\kappa$ oxide, SiGe). Heterostructure MOS (HMOS) transistors with buried SiGe channels, particularly those operated using the dynamic threshold (DT) scheme, have exhibited attractive low-frequency noise performance [1], [2] owing to additional control of the body bias. In this paper, device-level flicker noise simulation capabilities have been developed and employed to investigate the low-frequency noise behavior in these SiGe p-HMOS devices.

Two sources are commonly regarded as to contribute to the flicker noise in MOSFET devices as reviewed in [3]—the channel carrier number fluctuations ($\Delta N$ theory [4]) and the mobility fluctuations ($\Delta\mu$ theory [5]). The latter is primarily related to phonon scattering; however, other scattering mechanisms such as surface roughness can also play a role. An improved model accounting for the effect of parasitic source/drain resistance was also proposed in [6] and [7]. More recently, the correlation between the carrier number fluctuation and the mobility fluctuation due to Coulomb scattering has been discussed [8]; a unified model was proposed ($\Delta\mu-\Delta N$ theory) to explain the origin of low-frequency noise in p-type MOSFETs (pMOS) [9]. The model was later critically reviewed in [10], where an improvement was suggested to consider the dependence on the inversion carrier density in modeling the screening effect. Such a modified unified model was later used for modeling flicker noise in both n- and p-type MOSFETs with high-$\kappa$ gate dielectrics [11], [12]. The unified model was also extended to qualitatively model the low-frequency noise behavior in SiGe p-HMOS [13]. In essence, the channel carrier number fluctuation is induced by the trapping/detrapping of oxide traps with energies close to the channel quasi-Fermi level [3], [4]. The unified model accounts for the mobility fluctuations due to remote Coulomb scattering from those trapped charges. In [13], different Coulomb scattering coefficients were considered for buried and parasitic surface channels, as those two channels are separated from the trapped charges by different distances. On the other hand, a modified Hooge model was proposed to explain the low-frequency noise origin in SiGe p-HMOS [14]. In that model, different Hooge parameters were used for the surface and buried channels, and noise sources between those two channels were assumed to be uncorrelated. The dominant component of the flicker noise in their p-HMOS was attributed to the Hooge model instead of the unified model [14].

In this paper, device-level flicker noise simulation capabilities have been developed to investigate the low-frequency noise behavior in SiGe p-HMOS devices. The numerical analysis of thermal noise in MOSFETs is achieved using the impedance field method (IFM) [15], which essentially computes the noise propagation from a local source to the terminals of interest. Combined with proper modeling of the local noise source, the integrated terminal noise can be obtained. The extension of the IFM for flicker noise simulations is based on the modeling of tunneling-based nonlocal charge trapping/detrapping [16], whereby the number fluctuations are quantitatively modeled. This method was implemented in a general device simulator, PROPHET [17], and used to investigate the flicker noise behavior in high-$\kappa$ gate oxide MOSFETs [18]. In this paper, an additional postprocessing step is used to take into account the correction term of correlated mobility fluctuations according to

Manuscript received December 13, 2007; revised March 10, 2008. This work was supported in part under the MARCO Materials, Structures, and Devices (MSD) Focus Research Center Program. The review of this paper was arranged by Editor M. J. Deen.

C.-Y. Chen and R. W. Dutton are with Center for Integrated Systems, Stanford University, Stanford, CA 94305 USA (e-mail: rdutton@stanford.edu).

Y. Liu is with the Stanford TCAD Group, Stanford University, Stanford, CA 94305 USA.

J. Sato-Iwanaga, A. Inoue, and H. Sorada are with the Advanced Devices Development Center, Matsushita Electric Industrial Company, Ltd., Osaka 570-8501, Japan.

Digital Object Identifier 10.1109/TED.2008.925329

the unified model as well as the contribution from the Hooge model. Layer dependence of the surface and buried channels are considered for the unified model and the Hooge model. Using simulation capabilities based on our improved numerical model, the flicker noise in p-type $Si_{0.7}Ge_{0.3}/Si$ HMOS is simulated and carefully correlated with experimental data in terms of its dependence on gate biases, drain currents, and body biases. The underlying cause of the observed flicker noise behavior is investigated with the aid of detailed device simulations. It is shown that, in general, the $\Delta N - \Delta\mu$ fluctuation and the Hooge mobility fluctuation processes are playing dominant roles in the turn-on and subthreshold regimes, respectively.

## II. Flicker Noise Models

The numerical device-level noise model is achieved by adopting the IFM and proper modeling of the local noise fluctuations, which are combined with tunneling-based nonlocal charge trapping/detrapping. The microscopic noise source of the number fluctuation is modeled as originating from the traps inside the gate oxide layers [19]. In addition to the Poisson and continuity equations, a rate equation for the trapped electron density is self-consistently solved, i.e.,

$$\begin{aligned} dn_t/dt &= G - R \\ &= [(N_T - n_t)/\tau - n_t \exp(E_T - E_F/k_B T)/\tau] \end{aligned} \tag{1}$$

where $n_t$ is the trapped carrier density, $N_T$ is the total trap density, $\tau$ is the tunneling time calculated based on the WKB method, $E_T$ and $E_F$ reflect the trap energy and the quasi-Fermi level, respectively, and $G$ and $R$ are the generation and recombination rates, respectively. It should be noted that this approach is nonlocal from a simulation viewpoint. The impedance field is then solved with the inclusion of this rate equation. According to Bonani and Ghione [20], the microscopic noise source inside the gate oxide is modeled as white generation–recombination noise in the following:

$$S_{\rm nt}(\bar{r}) = 2(G + R). \tag{2}$$

To account for the correlated Coulomb mobility fluctuation based on the inversion carrier density dependence [10], a postprocessing approach is adopted; the noise contribution is multiplied by a correction term, i.e.,

$$\eta = \left(1 + \mu\sqrt{n_{2\text{-D}}}/\mu_{c0}\right)^2 \tag{3}$$

where $n_{2\text{-D}}$ is the 2-D inversion carrier density, and $u_{c0}$ is a mobility fitting scattering parameter, which depends on the interface properties and the material of gate oxide [11]. In this approach, the correction applies to the sheet of 2-D inversion charge and produces satisfactory results for high-$\kappa$ bulk devices [18]. In modeling SiGe p-HMOS, the surface and buried channels possess quite different interface properties. The surface channel generally incurs higher $\Delta N$-induced mobility fluctuations compared to the buried channel due to the fact that it is closer to the oxide interface. Therefore, an improvement is made in this paper—the correction term is applied to the 3-D carrier density $n_{3\text{-D}}$, and the fitting mobility scattering parameter $\mu_{c0\_3\text{-D}}$ is a function of the vertical position, which is used to model the different noise properties of the two channels.

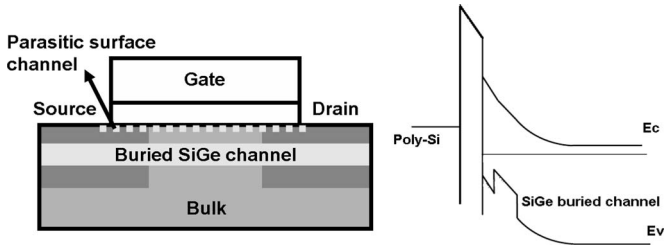


Fig. 1. Schematic plots of a p-type SiGe/Si HMOS device structure and a band diagram along the vertical direction.

The Hooge mobility fluctuation model was suggested to be the flicker noise source in SiGe p-HMOS [14]. This paper also accounts for its contribution. For SiGe p-HMOS, two uncorrelated Hooge parameters, i.e., $\alpha_{\rm cap}$ and $\alpha_{\rm SiGe}$ for the cap and SiGe channels, respectively, are used to model the respective noise components, i.e.,

$$\frac{S_{\rm id}}{I_d^2} = \left(\frac{q\alpha_{\rm cap}}{WLQ_{\rm cap}f}\frac{I_{d\,\rm cap}^2}{I_d^2} + \frac{q\alpha_{\rm SiGe}}{WLQ_{\rm SiGe}f}\frac{I_{d\,\rm SiGe}^2}{I_d^2}\right) \tag{4}$$

where $Q_{\rm cap}$ and $Q_{\rm SiGe}$ are the inversion charge densities at the surface and SiGe channels, respectively; $W$ and $L$ are the channel width and the channel length, respectively. The total drain current noise is calculated as the sum of the layer-dependent $\Delta N - \Delta\mu$ fluctuations and Hooge mobility fluctuations, i.e.,

$$S_{\rm id\_total} = S_{\rm id\_unified} + S_{\rm id\_Hooge}. \tag{5}$$

## III. Results and Discussions

The noise model has been used to numerically investigate the flicker noise behavior at various gate biases, drain currents, and body biases in SiGe p-HMOS. A schematic cross-sectional view of the SiGe p-HMOS is shown in Fig. 1. Two different SiGe p-HMOS devices and two control Si PMOS devices are used for this study on bulk and partially depleted (PD) SOI substrates, respectively. Table I gives a summary of simulated device structure parameters. In the simulations, the oxide trap density $N_T$ is set to $4 \times 10^{17}/(\text{cm}^3 \cdot \text{eV})$ and $4.7 \times 10^{17}/\text{cm}^3 \cdot \text{eV}$ for Si and SiGe devices, respectively, and the fixed interface charge density is $1.75 \times 10^{11}/\text{cm}^2$. For noise simulations, it is important to firstly ensure that the device dc characteristics are properly simulated. The carrier transport in the p-HMOS devices is modeled by solving the Poisson and electron and hole continuity equations under the drift-diffusion assumption. The Darwish model [21] with adjusted parameters has been adopted to model the effective field dependence of the carrier mobility. The transport of the carriers across the heterostructures is modeled as a thermionic emission process. Simulated and measured $I_d$–$V_g$ curves of the studied devices are shown in Fig. 2(a)–(d).

TABLE I
SUMMARY OF SIMULATED DEVICE PARAMETERS

| Devices | EOT | Si cap | SiGe channel | Gate length | Gate width | $V_{th}$ | Bulk thickness |
|---|---|---|---|---|---|---|---|
| Bulk p-MOS | 8nm | -- | -- | 1um | 10um | -0.44V | 500nm |
| SiGe p-HMOS | 8nm | 6nm | 14nm | 1um | 10um | 0.01V | 500nm |
| PD p-MOS | 6nm | -- | -- | 1um | 10um | -0.27V | 160nm |
| PD SiGe p-HMOS | 6nm | 9nm | 15nm | 1um | 10um | -0.14V | 160nm |

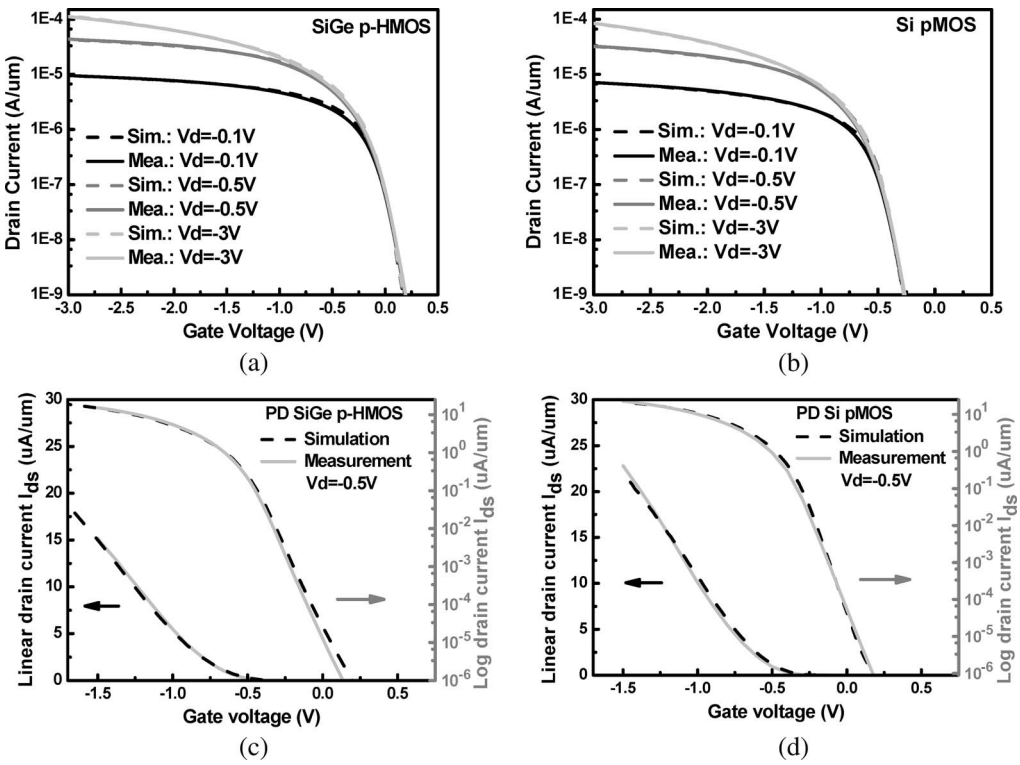


Fig. 2. Measured and simulated $I_d$–$V_g$ characteristics for (a) bulk $Si_{0.7}Ge_{0.3}$ p-HMOS, (b) control Si bulk pMOS, (c) PD $Si_{0.7}Ge_{0.3}$ p-HMOS, and (d) PD control Si pMOS.

### *A. Gate Bias and Drain Current Dependence*

The bulk SiGe p-HMOS and bulk Si control devices are used for this study. Different gate biases are applied, ranging from subthreshold to strong inversion for each device. In the layer-dependent correlated mobility fluctuation model, the 3-D mobility fitting parameter $\mu_{c0\_3\text{-D}}$ is set to $1.4 \times 10^{11}$ and $1 \times 10^{12}$ $\sqrt{\text{cm}}/(\text{V} \cdot \text{s})$ for the surface (Si) and buried (SiGe) channels, respectively. These values of $\mu_{c0\_3\text{-D}}$ correspond to 2-D parameter $\mu_{c0\_2\text{-D}}$ values of $5 \times 10^7$ and $3.57 \times 10^8$ $\text{cm}/(\text{V} \cdot \text{s})$ for the surface (Si) and buried (SiGe) channels, respectively. The value in the surface layer is consistent with the number reported in [11]. The larger value in the buried SiGe channel reduces the correlated mobility fluctuation term in the SiGe channel compared to that in the Si channel [note that larger $\mu_{c0\_2\text{-D}}$ corresponds to lower noise according to (3)]; the reduction factor between the two channels agrees well with that used in [13]. The Hooge parameters used in this paper are $6 \times 10^{-6}$ and $1 \times 10^{-5}$ for the SiGe buried channel and the surface channel, respectively, which are within the expected reasonable range of $10^{-4}$–$10^{-6}$ [22].

Our noise measurement setup follows that described in [23]. A noise analyzer, i.e., BAT 9812B, is used to amplify the current generated by test devices. HP 4142B provides the dc bias for test devices and provides $I$–$V$ measurements and the network signal analyzer SR 780 for the measurement of the spectral density of the noise in MOSFET. All pieces of equipment are controlled by NoisePro [24].

The normalized drain current noise $S_{\text{id}}/I_d^2$ at 10 Hz is plotted as a function of the gate voltage in Fig. 3. From Reimbold's theory [25], the gate bias dependence of $S_{\text{id}}/I_d^2$ should show a weak inversion plateau and then decrease in strong inversion. On the other hand, in the Hooge model, $S_{\text{id}}/I_d^2$ is usually inversely proportional to the inversion carrier density [26]. This leads to an exponential increase in noise in the Hooge model in the subthreshold regime with decreasing overdrive voltages. As shown in Fig. 3, the measured $S_{\text{id}}/I_d^2$ at subthreshold rapidly increases with decreasing overdrive biases, indicating the applicability of the Hooge model in this regime. As suggested from the simulated noise components in Fig. 3, the Hooge model is dominant in subthreshold, and the $\Delta N - \Delta\mu$ unified model plays a major role under strong inversion. The measured

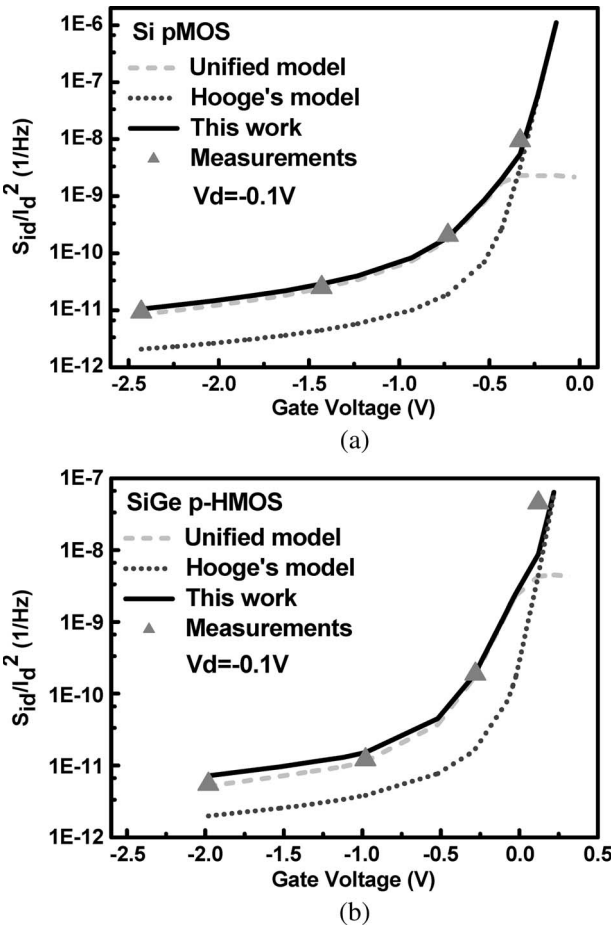


Fig. 3. Measured and simulated normalized drain current noise $S_{\rm id}/I_d^2$ at 10 Hz as a function of the gate voltage for (a) Si pMOS and (b) SiGe p-HMOS.

data for p-HMOS in [27] show similar noise behavior in subthreshold that is consistent with the model proposed in this paper. Moreover, flicker noise data for p-HMOS in strong inversion have been reported in [28] and [29], which show trends in agreement with the measured and simulated results in this paper. We note that an improved $\Delta\mu$-based model accounting for the effect of parasitic series resistance was proposed in [6]. We have found that it is not directly applicable in explaining the measured data in our devices when using realistic source/drain series resistance values.

In Fig. 4, the measured and simulated $S_{\rm id}$ are plotted against the gate bias for SiGe p-HMOS. Two simulations have been conducted with and without considering the layer dependence of the correlated mobility fluctuation model, respectively. It is evident that in the nonlayer-dependent case, $S_{\rm id}$ decreases as the overdrive gate voltage rises above threshold. This is because, as the overdrive voltage increases, more holes are spilled over into the surface channel. Without considering the difference in the mobility fluctuations, the surface channel has much lower mobility, and, therefore, the simulations lead to a reduction of $S_{\rm id}$. Conversely, only when the significant correlated mobility fluctuation in the surface channel is accounted for can simulations predict the increase in $S_{\rm id}$ with increasing overdrive voltages, which is in agreement with experimental data. Other measurement results [30] also have shown an increase

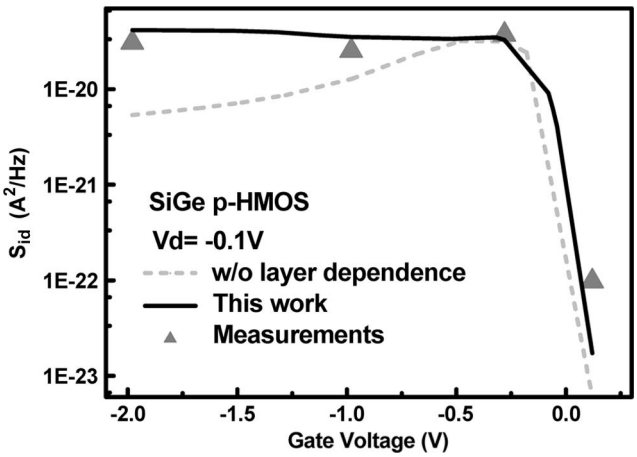


Fig. 4. Measured and simulated drain current noise $S_{\rm id}$ at 10 Hz as a function of the gate bias for SiGe p-HMOS. The gray dotted line neglects the layer-dependent contribution of the correlated mobility fluctuation, whereas, in this work, different fitting mobility scattering parameters are used in the Si cap layer and in the SiGe channel, and Hooge mobility fluctuations are also accounted.

in $S_{\rm id}$ with rising overdrive biases, which further confirms the validity of our model.

In Fig. 5, the normalized drain current noise $S_{\rm id}/I_d^2$ is plotted versus the drain current for the two devices—Si and SiGe p-MOSFETs. As can be seen from the figure, $S_{\rm id}/I_d^2$ and $(g_m/I_d)^2$ exhibit good correlation for both devices; this can be regarded as an additional evidence to support the unified model under inversion conditions [24]. On the other hand, the noise level increases with the lower drain current in subthreshold, which deviates from the saturation behavior of $(g_m/I_d)^2$. This also indicates that the Hooge model is playing a dominant role in subthreshold. This observation agrees with that reported in [13].

### *B. Body Bias Dependence*

The PD SiGe p-HMOS and PD Si pMOS devices are used for the study of body bias dependence, and the mobility fitting parameter $\mu_{c0\_3\text{-D}}$ is the same as the bulk devices. A contact to the body region has been fabricated in the PD devices to provide direct body biasing. Such a body contact was originally designed for DT mode operation, where the major device performance benefit came from efficient channel carrier modulation through body biasing [1], [2].

In Fig. 6, the simulated and measured drain current noise spectra are given, and four different body biases are applied, ranging from a reverse bias (0.2 V) to a forward bias ($-0.4$ V); the overdrive voltage is kept at $-0.3$ V for each device. The simulation results agree well with the noise measurements, and strong body bias dependence of the drain current noise is observed in the SiGe p-HMOS. The flicker noise level decreases by about an order of magnitude as the body bias is varied from a reverse bias to a forward bias in SiGe p-HMOS. However, under the same conditions, the Si control device shows no observable body bias dependence. It should be noted that in [14], the flicker noise body bias dependence was observed in Si pMOS, and the difference can be explained by the quality of surface roughness. Using the Darwish model, in this paper, the parameter $\delta$ of

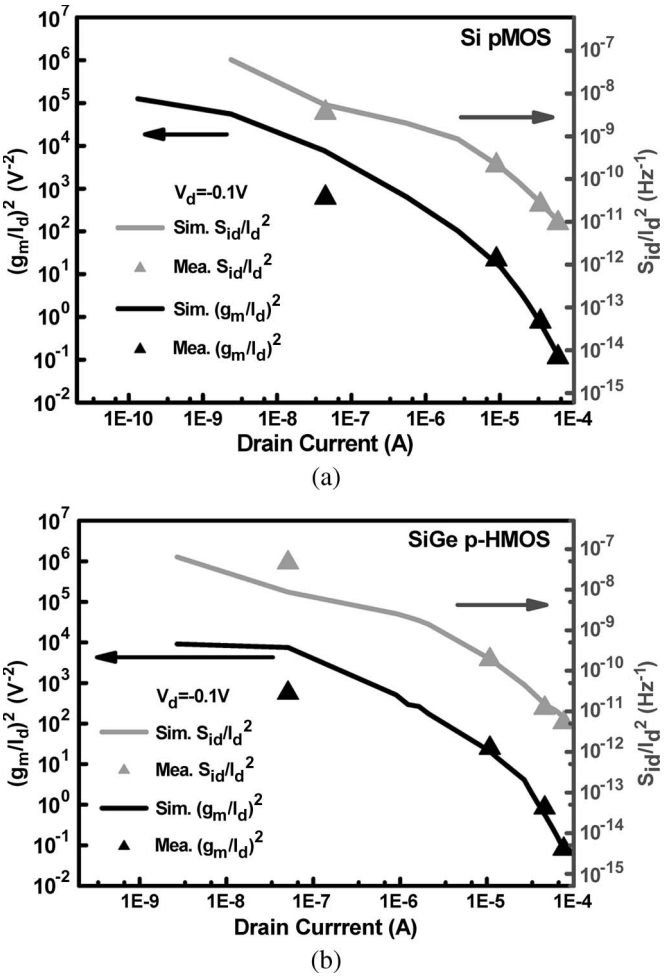


Fig. 5. Measured and simulated normalized drain noise $S_{\rm id}/I_d^2$ at 10 Hz (right $y$-axis) together with $(g_m/I_d)^2$ (left $y$-axis) as functions of the drain current. Data for (a) Si pMOS and (b) SiGe p-HMOS are shown.

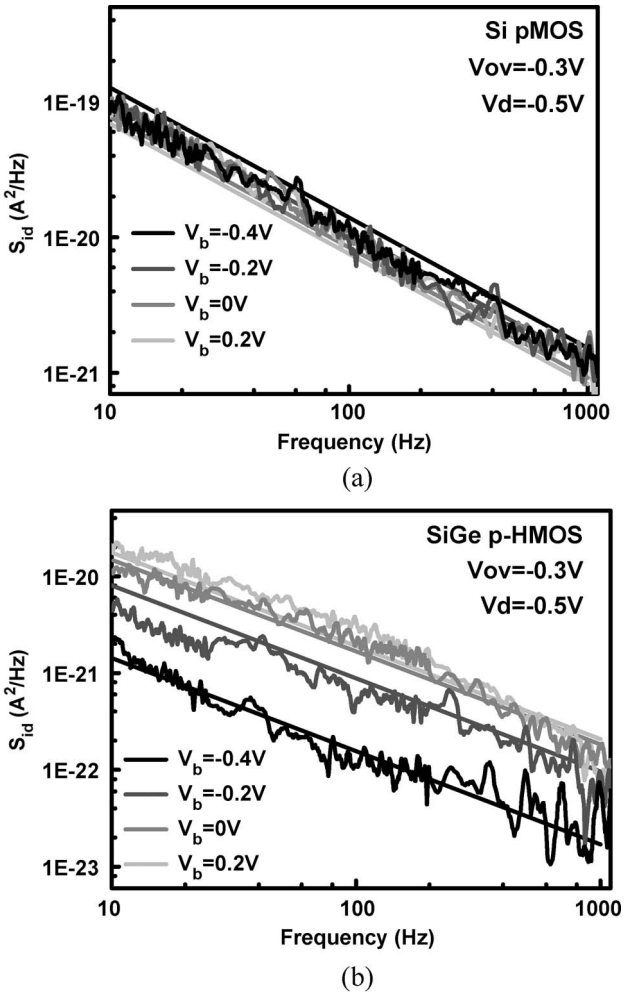


Fig. 6. Measured and simulated drain current noise spectra for (a) Si pMOS and (b) SiGe p-HMOS. The frequency range is 10 Hz to 1 kHz. Four body biases are used ranging from 0.2 to $-0.4$ V.

carrier mobility limited by surface roughness scattering $\mu_{\rm sr}$ is set as $4.1 \times 10^{15}$ V/s, which agrees with [21] and is about two orders-of-magnitude larger than [14]. In the Hooge model, $S_{\rm id}$ is inversely proportional to $\mu_{\rm sr}^2$ [5]; therefore, compared with [14], the effect of an effective vertical electrical field $E_{\rm eff}$ is about four orders-of-magnitude smaller in this paper.

In Fig. 7, the hole density in the Si cap layer and the carrier density in the SiGe channel, as functions of the body bias, are shown. The decrease in the body bias leads to the increased hole density in the buried channel and reduces the hole density in the Si cap layer. The strong body bias dependence of PD SiGe p-HMOS devices can be attributed to the redistribution of carriers between the two channels with the body bias change; the surface channel incurs higher mobility fluctuations than the buried channel. To clarify this point, in the inset of Fig. 7, simulated valence band diagrams are shown for two different body bias conditions, whereas the overdrive voltage is kept constant. It can be seen that as the body bias varies from a reverse bias to a forward bias, the buried channel is pulled closer to the quasi-Fermi level, so the carrier density in the SiGe buried channel increases.

Fig. 8 shows the drain current noise and the carrier density in the Si cap layer at different body bias conditions ranging

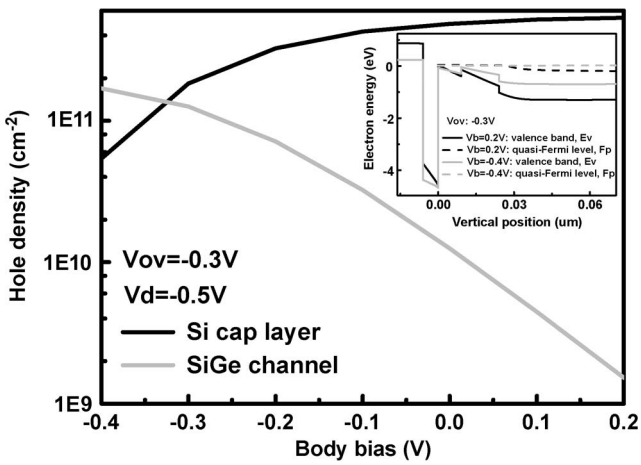


Fig. 7. Hole density in the Si cap layer and carrier density in the SiGe channel as functions of the body bias. The small plot is TCAD simulations of the band diagrams along the vertical direction for two body bias conditions ($V_b = 0.2$ V and $V_b = -0.4$ V).

from a reverse bias to a forward bias. The correlation between the flicker noise level and the hole density in the Si cap layer indicates that the flicker noise is mostly determined by the

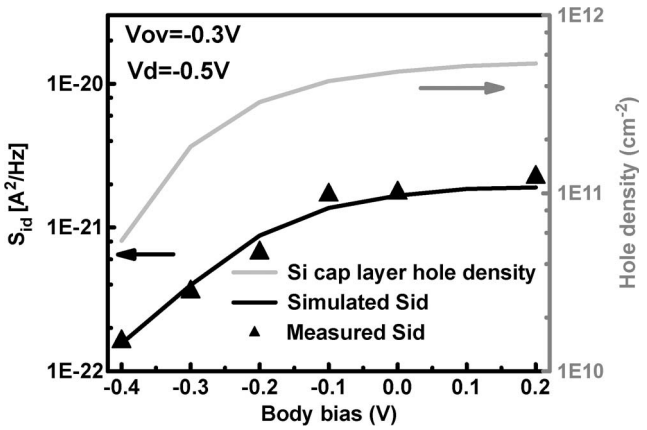


Fig. 8. Drain current noise $S_{\rm id}$ (left $y$-axis) at 100 Hz together with the hole density in the Si cap layer (right $y$-axis) as functions of the body bias.

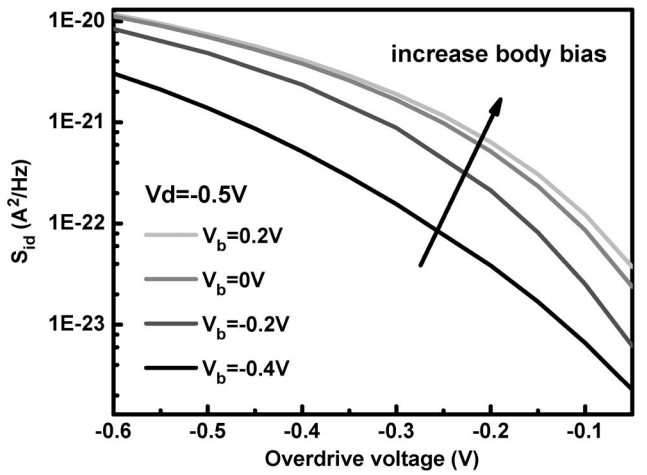


Fig. 9. Simulation data for the drain current noise $S_{\rm id}$ as a function of the overdrive voltage at a frequency of 100 Hz.

Si cap layer carrier density due to higher Coulomb scattering near the Si cap layer. In PD SiGe p-HMOS, the Si cap layer carrier density is efficiently modulated by the body bias, leading to strong body bias dependence of the flicker noise level.

In Fig. 9, the body bias dependence is also studied for different overdrive bias levels. When the overdrive voltage is small ($-0.05$ V), $S_{\rm id}$ is decreased by 16.4 times from the reverse bias to the forward bias. However, when the overdrive voltage increases ($-0.6$ V), the decrease in $S_{\rm id}$ from the reverse bias to the forward bias is just 3.8 times. In general, for a more negative overdrive voltage, smaller body bias dependence of the drain current noise level is observed. This can be attributed to the fact that for more negative overdrive voltages, the carrier concentrations in both channels are controlled by the gate electrode to a larger extent and, therefore, less sensitive to the body bias variation.

Fig. 10 shows the simulated two-channel carrier density as a function of the overdrive voltage for the reverse and forward body biases, respectively. It can be seen that when the forward body bias is applied, in a region of smaller negative overdrive, both buried and surface channels contribute to the total flicker noise. However, with larger negative overdrive, the hole density in the Si cap layer starts to dominate. Conversely, when the

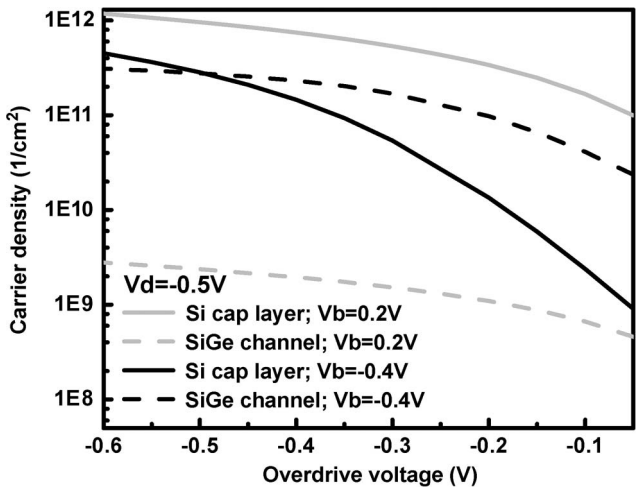


Fig. 10. Carrier density for both surface and buried channels as a function of the overdrive voltage in two different body biases, $-0.4$ and 0.2 V.

reverse body bias is applied, the hole density in the Si cap layer is dominant across the entire overdrive voltage range. For a larger negative gate bias, the hole density in the Si cap layer is dominant for both reverse and forward body biases, resulting in a less difference in the $S_{\rm id}$ values observed. However, with a smaller negative gate bias, hole densities in the Si cap layer and in the SiGe channel are dominant in the reverse and forward body biases, respectively; a larger difference in the body bias dependence is observed for this condition. The results are consistent with the gate bias dependence of $S_{\rm id}$ shown in Fig. 9.

## IV. Conclusion

Flicker noise mechanisms in the SiGe p-HMOS have been numerically investigated and correlated with experimental data. The analysis is based on the IFM with physical modeling of the local noise sources, including nonlocal trap/detrap processes from the gate dielectric. In particular, layer-dependent $\Delta N-\Delta\mu$ fluctuations with Hooge mobility fluctuations are applied to separate treatments of the buried and parasitic surface channels. Agreement with the observed variations of gate biases, drain currents, and body biases suggests the applicability of the proposed flicker noise model for SiGe p-HMOS.

## Acknowledgment

The authors would like to thank research support from Center for Integrated Systems. They would also like to thank the reviewers for useful suggestions for improving the manuscript and providing additional perspective on noise modeling issues.

## References

[1] A. Asai, J. Sato-Iwanaga, A. Inoue, Y. Hara, Y. Kanzawa, H. Sorada, T. Kawashima, T. Ohnishi, T. Takagi, and M. Kubo, "Low-frequency noise characteristics in SiGe channel heterostructure dynamic threshold pMOSFET (HDTMOS)," in *IEDM Tech. Dig.*, 2002, pp. 35–38.

[2] A. Inoue, A. Asai, Y. Kawashima, H. Sorada, Y. Kanzawa, T. Kawashima, H. Hara, and T. Takagi,"Low frequency noise (LFN) characteristics of SiGe channel SOI dynamic threshold MOSFETs (SiGe-SOI-DTMOS)

for low-power applications," in *Proc. IEEE Int. SOI Conf.*, 2003, pp. 149–150.
[3] A. Van Der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.
[4] A. McWhorter, "1/f noise and germanium surface properties," in *Semiconductor Surface Physics*. Philadelphia, PA: Univ. Pennsylvania Press, 1957, pp. 207–228.
[5] F. N. Hooge, "1/f noise sources," *IEEE Trans. Electron Devices*, vol. 41, no. 11, pp. 1926–1935, Nov. 1994.
[6] L. K. J. Vandamme, "On the origin of 1/f noise in MOSFETs," *Fluctuation Noise Lett.*, vol. 7, no. 3, pp. L321–L329, Sep. 2007.
[7] L. K. J. Vandamme, "1/f Noise in MOSTs: Faster is noisier," in *Advanced Experimental Methods for Noise Research in Nanoscale Electronic Devices*, J. Sikula and M. E. Levinshtein, Eds. Dordrecht, The Netherlands: Kluwer, 2004, pp. 109–120.
[8] R. Jayaraman and C. G. Sodini, "A 1/f noise technique to extract the oxide trap density near the conduction band edge of silicon," *IEEE Trans. Electron Devices*, vol. 36, no. 9, pp. 1773–1782, Sep. 1989.
[9] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal–oxide–semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, no. 3, pp. 654–665, Mar. 1990.
[10] E. P. Vandamme and L. K. J. Vandamme, "Critical discussion on unified 1/f noise models for MOSFETs," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2146–2152, Nov. 2000.
[11] B. Min, S. P. Devireddy, Z. Çelik-Butler, F. Wang, A. Zlotnicka, H.-H. Tseng, and P. Tobin, "Low-frequency noise in submicrometer MOSFETs with $HfO_2$, $HfO_2/Al_2O_3$ and $HfAlO_x$ gate stacks," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1679–1687, Oct. 2004.
[12] B. Min, S. P. Devireddy, Z. Çelik-Butler, A. Shanware, K. Green, J. J. Chambers, M. V. Visokay, and L. Colombo, "Low-frequency noise characteristics of HfSiON gate-dielectric metal–oxide–semiconductor-field-effect transistors," *Appl. Phys. Lett.*, vol. 86, no. 8, p. 082 102, Feb. 2005.
[13] G. Ghibaudo and J. Chroboczek, "On the origin of the LF noise in Si/Ge MOSFETs," *Solid State Electron.*, vol. 46, no. 3, pp. 393–398, Mar. 2002.
[14] M. von Haartman, A.-C. Lindgren, P.-E. Hellstrom, B. G. Malm, S.-L. Zhang, and M. Ostling, "1/f noise in Si and $Si_{0.7}Ge_{0.3}$ pMOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2513–2519, Dec. 2003.
[15] W. Shockley, J. A. Copeland, and R. P. James, "The impedance field method of noise calculation in active semiconductor devices," in *Quantum Theory of Atoms, Molecules and Solid State*, P. O. Lowdin, Ed. New York: Academic, 1966, pp. 537–563.
[16] F.-C. Hou, G. Bosman, and M. E. Law, "Simulation of oxide trapping noise in submicron n-channel MOSFETs," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 846–852, Mar. 2003.
[17] *PROPHET Technical Information*. [Online]. Available: http://www-tcad.stanford.edu/~prophet
[18] Y. Liu, S. Cao, and R. W. Dutton, "Numerical investigation of low frequency noise in MOSFETs with high-k gate stacks," in *Proc. SISPAD*, 2006, pp. 99–102.
[19] Y. Liu, A. Shanware, L. Colombo, and R. W. Dutton, "Modeling of charge trapping induced threshold-voltage instabilities in high-$\kappa$ gate dielectric FETs," *IEEE Electron Device Lett.*, vol. 27, no. 6, pp. 489–491, Jun. 2006.
[20] F. Bonani and G. Ghione, "Generation–recombination noise modeling in semiconductor devices through population or approximate equivalent current density fluctuations," *Solid State Electron.*, vol. 43, no. 2, pp. 285–295, Feb. 1999.
[21] M. N. Darwish, J. L. Lentz, M. R. Pinto, P. M. Zeitzoff, T. J. Krutsick, and H. H. Vuong, "An improved electron and hole mobility model for general purpose device simulation," *IEEE Trans. Electron Devices*, vol. 44, no. 9, pp. 1529–1997, Sep. 1997.
[22] G. Ghibaudo, "Low frequency noise and fluctuations in advanced CMOS devices," in *Proc. SPIE—Noise in Devices and Circuits*, M. J. Deen, Z. Çelik-Butler, and M. E. Levinshtein, Eds., 2003, vol. 5113, pp. 16–28.
[23] A. D. Lambert, B. Alderman, R. J. P. Lander, E. H. C. Parker, and T. E. Whall, "Low frequency noise measurements of p-channel $Si_{1-x}Ge_x$ MOSFETs," *IEEE Trans. Electron Devices*, vol. 46, no. 7, pp. 1484–1486, Jul. 1999.
[24] *NoisePro Manual*. [Online]. Available: http://www.celestry.com/pdf/noisepro.pdf
[25] G. Reimbold, "Modified 1/f trapping noise theory and experiments in MOS transistors biased from weak to strong inversion—Influence of interface states," *IEEE Trans. Electron Devices*, vol. ED-31, no. 9, pp. 1190–1198, Sep. 1984.
[26] R. P. Jindal and A. Van Der Ziel, "Phonon fluctuation model for flicker noise in elemental semiconductors," *J. Appl. Phys.*, vol. 52, no. 4, pp. 2884–2888, Apr. 1981.
[27] M. von Haartman, "Low-frequency noise characterization, evaluation and modeling of advanced Si- and SiGe-based CMOS transistors," "Ph.D. dissertation," Royal Inst. Technol. (KTH), Stockholm, Sweden, 2006.
[28] M. Myronov, O. A. Mironov, S. Durov, T. E. Whall, E. H. C. Parker, T. Hackbarth, G. Hock, H.-J. Herzog, and U. Konig, "Reduced 1/f noise in p-$Si_{0.3}Ge_{0.7}$ metamorphic metal–oxide–semiconductor field-effect transistor," *Appl. Phys. Lett.*, vol. 84, no. 4, pp. 610–612, Jan. 2004.
[29] P. W. Li, W. M. Liao, C. C. Shih, T. S. Kuo, L. S. Lai, Y. T. Tseng, and M. J. Tsai, "High performance Si/SiGe heterostructure MOSFETs for low power analog circuit applications," *Solid State Electron.*, vol. 47, no. 6, pp. 1095–1098, Jun. 2003.
[30] N. B. Lukyanchikova, M. V. Petrichuk, N. P. Garbar, L. S. Riley, and S. Hall, "A study of noise in surface and buried channel SiGe MOSFETs with gate oxide grown by low temperature plasma anodization," *Solid State Electron.*, vol. 46, no. 12, pp. 2053–2061, Dec. 2002.

**Chia-Yu Chen** (S'07) received the B.S. degree from National Central University, Taoyuan, Taiwan, R.O.C., in 2003 and the M.S. degree from Stanford University, Stanford, CA, in 2008, both in electrical engineering. He is currently working toward the Ph.D. degree in the Center for Integrated System, Stanford University.

In the summer of 2006, he was with KLA-Tencor, San Jose, CA, where he worked on flicker noise measurement. In 2007, he was with Berkeley Design Automation, Santa Clara, CA, working on transient flicker noise modeling. His research interests include noise modeling, noise measurement, and device scaling.

**Yang Liu** (M'03) received the B.S. degree from the University of Science and Technology, Hefei, China, in 1998 and the Ph.D. degree in physics from the University of Illinois, Urbana, in 2002.

In 2003, he joined the Stanford TCAD Group, Stanford University, Stanford, CA, as a Research Associate. His current research interests include the modeling and design of novel biological sensors, digital and analog electronic devices, and optoelectronic LEDs and lasers.

**Robert W. Dutton** (S'67–M'70–SM'80–F'84) received the B.S., M.S., and Ph.D. degrees from the University of California, Berkeley, in 1966, 1967, and 1970, respectively.

He held summer staff positions with Fairchild, Bell Telephone Laboratories, Hewlett-Packard, IBM Research, and Matsushita in 1967, 1973, 1975, 1977, and 1988, respectively. He is currently a Professor of electrical engineering with Stanford University, Stanford, CA, where he is the Director of Research with the Center for Integrated Systems. He has published more than 200 articles and graduated more than four dozens of doctorate students. His research interests include integrated circuit process, device, and circuit technologies, particularly the use of computer-aided design in device scaling and for RF applications.

Dr. Dutton was an Editor for the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN from 1984 to 1986 and was elected to the National Academy of Engineering in 1991. He was the recipient of the IEEE J. J. Ebers and Jack Morton Awards in 1987 and 1996, respectively; the Guggenheim Fellowship to study in Japan in 1988; the C and C Prize (Japan) in 2000; the Career Achievement Award from the Semiconductor Industry Association (SIA) in 2005 for his sustained contributions in support of research that is critical to SIA needs; and the Phil Kaufman Award.

**Junko Sato-Iwanaga** received the B.S. degree in physics from Kobe University, Kobe, Japan, in 1986.

In 1986, she joined the Advanced Devices Development Center, Matsushita Electric Industrial Company, Ltd., Osaka, Japan. She has been engaged in the research and development of RF device simulation of GaAs and SiGe devices.

Ms. Iwanaga is a member of the Institute of Electronics, Information and Communication Engineers and the Japan Society of Applied Physics.

**Akira Inoue** received the B.S. and M.S. degrees in electrical engineering from Tokyo Institute of Technology, Tokyo, Japan, in 1997 and 1999, respectively.

In 1999, he joined the Advanced Devices Development Center, Matsushita Electric Industrial Company, Ltd., Osaka, Japan. He has worked on the research of SiGe channel MOSFETs.

**Haruyuki Sorada** received the B.S. and M.S. degrees in electrical engineering from Osaka University, Osaka, Japan, in 1994 and 1996, respectively.

In 1996, he joined the Advanced Devices Development Center, Matsushita Electric Industrial Company, Ltd., Osaka. He has been engaged in the research and development of Si quantum devices and SiGe channel devices.