Implementation of Temperature Dependent Contact Resistance Model for the Analysis of Deep Submicron Devices under ESD

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Abstract

The specific contact resistance(ρ_C) at the metal/semiconductor interface is known to be a monotonically decreasing function of temperature. Therefore the temperature dependence of ρ_C has significant implications for the reliable electrothermal behavior of deep submicron devices under high current and high temperature conditions. In this work, the effect of contact resistance on the performance of ESD protection devices has been investigated by device simulation and experiment with test structures in a 0.13μm silicided CMOS process. A temperature-dependent model for ρ_C was implemented in a device simulator; results based on the new model are presented in comparison with results of a self-consistent Schottky diode model which unifies thermionic emission and tunneling effects.

Introduction

In advanced CMOS devices, the contact resistance between the silicide layer and doped Si source/drain regions constitutes a significant fraction of the total parasitic series resistance[1], resulting in significant degradation of circuit performance. Furthermore, under ESD conditions, contact resistance contributes an appreciable fraction of on-resistance since the conductivity of channel and substrate region is highly modulated. It is known that the current distribution associated with the silicided contact system in the source/drain structure is strongly influenced by the contact resistance value itself[2,3] and recent studies have shown that the self-heating caused by the contact resistance is also considerable under ESD conditions[4]. However, ρ_C at temperatures approaching thermal failure is much less than that of room temperature so that the constant ρ_C over a broad temperature range may cause incorrect estimation of heat generation in the contact system.

The purpose of this work is two fold, first to investigate the effects of contact resistance on the thermal profile of ESD protection devices, second to demonstrate thermal behavior of contact systems using device simulation.

Effects of Contact Resistance Variation on ESD

The schematic of a silicided NMOS transistor used in the transmission line pulsing(TLP) test and simulation is shown in Fig. 1 with the gate to source/drain contact spacing (GSCS/GDCS) and the n+ overlap with the source/drain contact (S/D_OL) indicated. The ρ_C of silicide/n+ source and drain regions ranges from 10^{-8} Ωcm^2 to 10^{-5} Ωcm^2, depending on process conditions. Fig. 2 shows the *IV* curve measured by TLP test and 2-D electrothermal simulation with various specific

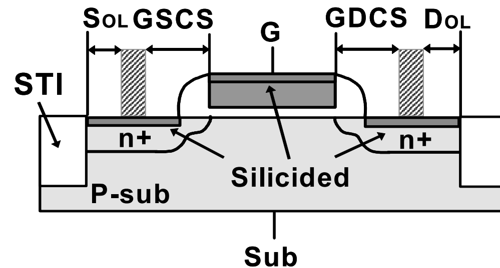

FIGURE 1. The schematic of a silicided NMOS transistor indicating the gate to source/drain contact spacing (GSCS/GDCS) and the n+ overlap with the source/drain contact (S/D_OL)

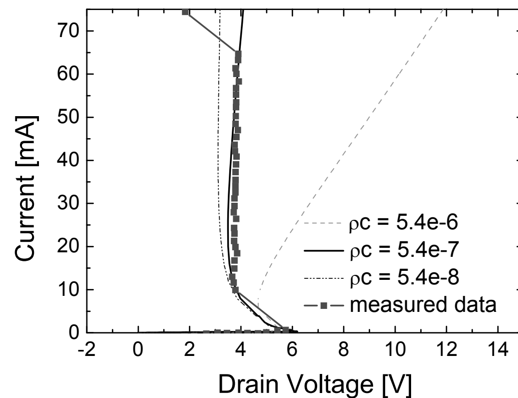

FIGURE 2. Measured TLP curve for the 1.5V NMOS transistor and simulation results with various specific contact resistances. The measured data matches well to the simulation results with ρ_c of $5.4x10^{-7}$ Ω cm^2

contact resistances. It is clearly shown that the on-resistance after snapback is significantly affected by ρ_C values and the measured curve are relatively well matched to the simulation results with ρ_C of 5.4 x 10^{-7} Ωcm^2. Electro-thermal simulations shown in Fig. 3 and 4 indicate that the temperature distributions with large current densities(4mA/um) change significantly with the variation of ρ_C. With ρ_C of 5.4 x 10^{-6} Ωcm^2 , the position of the highest temperature is located near shallow trench isolation(STI) region of the source side. However, with ρ_C of 5.4 x 10^{-7} Ωcm^2 and 5.4 x 10^{-8} Ωcm^2, the peak temperature is observed at drain/substrate junction beneath the gate. Fig. 3 shows the comparison of the temperature profile(at I=4mA/um) along the channel for different ρ_C . It can be observed that higher ρ_C causes considerable heating at the source side. Unexpectedly large heating at the source side in Fig. 4a can be explained by investigating the current flow vectors in Fig. 5. The current at the source side spreads from the sidewall to the shallow trench isolation(STI) which blocks heat transfer from the contact so that the generated heat is confined between the STI and sidewall.

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Temperature of the source side abruptly increases within a very short time of several ns. On the contrary, at the drain side current flows through the narrow region close to the sidewall, and the heat generated in this region can be transferred to bulk relatively easily.

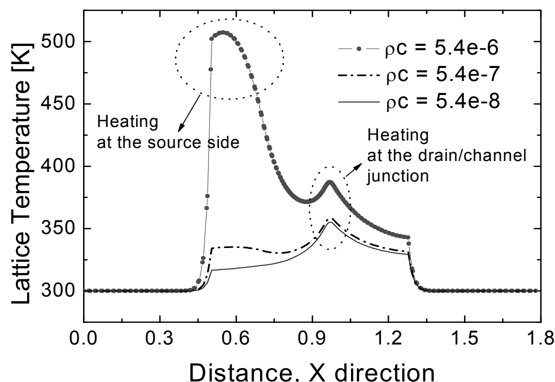

FIGURE 3. The temperature distribution along the channel(x-direction) for the devices with different ρ_c. Higher ρ_c causes considerable heating at the source side.

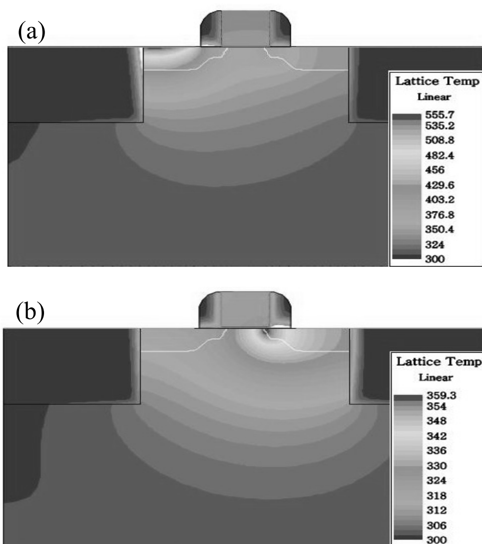

FIGURE 4. The temperature contours at I=4 mA/μm with (a) ρ_c = 5.4x10^{-6} Ω cm^2 and (b) ρ_c = 5.4x10^{-8} Ω cm^2

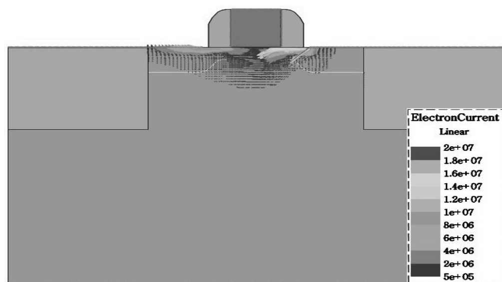

FIGURE 5. The current flow vectors of gate-grounded NMOS with ρ_c of 5.4x10^{-6} Ω cm^2, at I=4 mA/μm. At the source side, current is spread close to STI and the generated heat is confined in that region.

These steady-state simulation results are not able to reflect the actual transient situation. Considering that ρ_C is a decreasing function of temperature[2], the heat at the source side in Fig. 4a may be overestimated, and the result of Fig. 4b may underestimate the effect. To understand this phenomenon, physical insight can be obtained from the empirical data. The dependence of second breakdown triggering current It_2 has been investigated as a function of the gate-to-source/drain salicided contact spacing(GSCS and GSDS in Fig 1.) by Oh et al.[5]. It is shown that It_2 improves by increasing GDCS, mainly due to the reduction of current localization. It_2 also improves by increasing GSCS(as shown in Fig.6) due to an increase in the power dissipation volume. This observation correlates with the simulation results for high contact resistance. That is, with large GSCS, the heat generated by self-heating of source contact transfers to the bulk easily and the current level at thermal failure increases. However, Fig. 7 shows that GSCS variation does not have much effect on It_2 when current is uniformly distributed due to substrate bias, which implies that source contact heating is not that severe as in Fig. 4a.

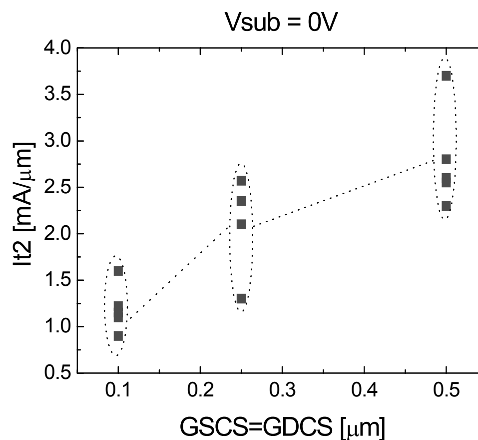

FIGURE 6. The current level at thermal failure(It_2) with gate-to-source/drain contact spacing(Vsub=0). As the spacing increases, It_2 also increases.

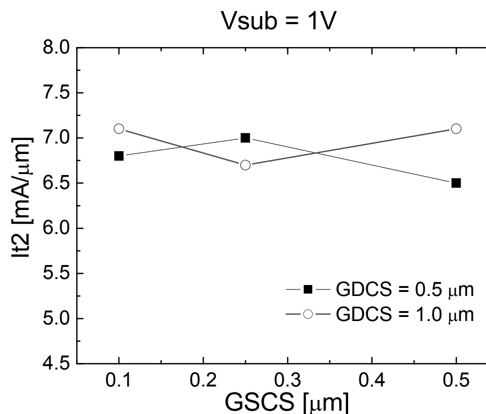

FIGURE 7. The current level at thermal failure(It_2) with gate-to-source contact spacing(Vsub=1). It_2 is nearly independent of gate-to-source contact spacing if current is almost uniform due to 1V substrate bias.

The overall investigation implies that the results from conventional device simulation with constant ρ_C are not

satisfactory for analysis of deep submicron devices at high temperatures. Therefore, for reliable electrothermal simulation of ESD events, it is essential to trace the dynamic variation of contact resistance as a function of temperature within very short time periods.

Implementation of Contact Resistance Model

Two contact models were implemented in a device simulator to account for the temperature dependent distributed contact resistance. The first method uses a hetero-junction model of the silicide layer and bulk Si, complete with thermionic emission and tunneling current at each node[6]. A simulated band-diagram is shown in Fig. 8a for a $TiSi_2/n^+$ Si junction at 0.2 V forward bias. This model can show the details of carrier transport, but requires excessive grid at the tunneling barrier. The second method is illustrated in Fig. 8b, where a temperature dependent ρ_C extracted from the numerical analysis is implemented as lumped elements, distributed over the contact surface. This approach doesn't require additional grid and is able to capture the essential physical phenomenon demonstrated using the first method.

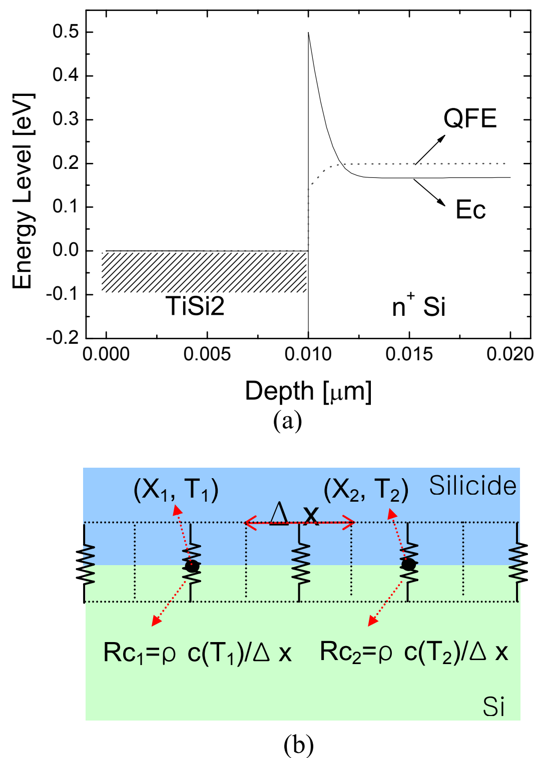

FIGURE 8. Two different methods for the implementation of temperature-dependent ρ_c model, (a) hetero-junction simulation with unified tunneling and thermionic emission(with 0.2 V bias applied) and (b) distributed contact resistance with temperature-dependence.

The simulation results with the complete hetero-junction physical model are shown for a Ti/n^+Si Schottky barrier diode(SBD) with various doping concentrations(Fig. 9) and ambient temperatures(Fig. 10). As shown in Fig. 10, the simulated *IV* curve at 300 K matches quite well to the experimental result[6] and the high temperature behavior can be predicted as well.

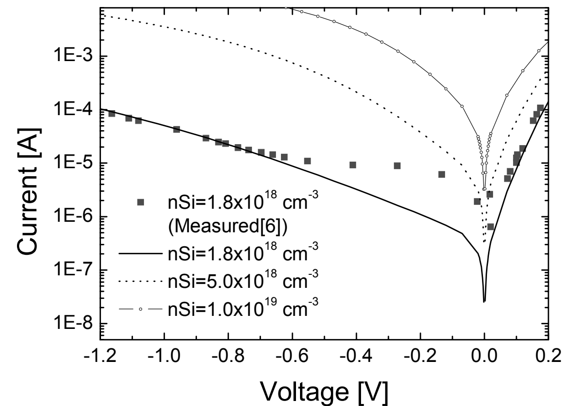

FIGURE 9. *IV* curves of $TiSi_2$/nSi diode (simulation results with various doping concentrations of Si and comparison with the measured data[6])

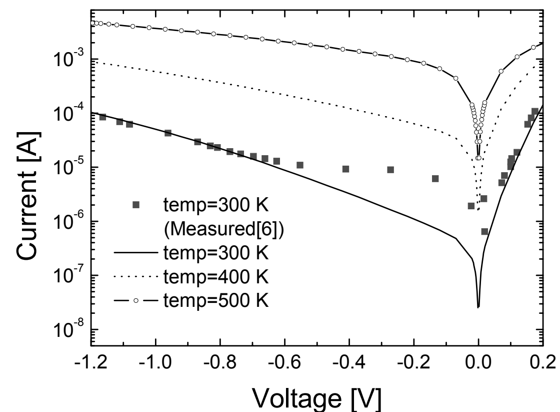

FIGURE 10. *IV* curves of $TiSi_2$/nSi diode(simulation results with various ambient temperatures). As temperature increases, current at a certain bias voltage also increases.

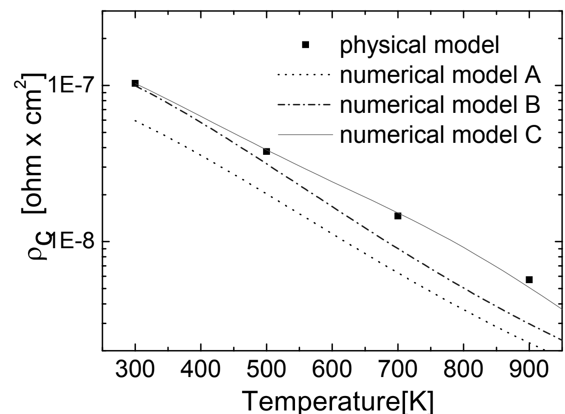

FIGURE 11. Specific contact resistivity(ρ_c) vs. temperature, calculated by various numerical models and physical model.

The numerical model for contact resistance[2, 7] is based on two assumptions; 1) free carriers are fully depleted within the depletion region; 2) the quasi-Fermi level is flat across the depletion region. By comparing numerical models against the

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physical model, it is demonstrated that the above two assumptions lead to significant deviations particularly at high temperatures. In Fig. 11, model A indicates the model with both assumptions and model B is only with the second assumption. The numerical model is extended by removing these assumptions[8]. In the improved model, a unified contact resistance expression is explicitly obtained and the results(model C in Fig. 11) shows excellent match with those from the physical model. In Fig. 12, the ρ_C values extracted from the complete hetero-junction model simulations with various ambient temperatures and doping concentrations are compared with the new numerical model. Similar trends of doping and temperature dependence can be clearly observed.

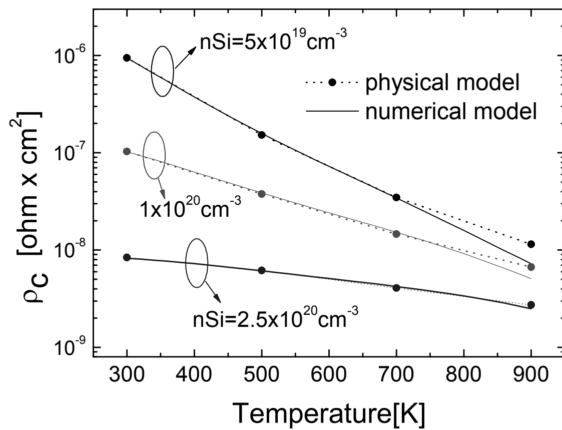

FIGURE 12. Comparison between the ρ_c extracted from heterojunction simulation and those from numerical model. Both show considerable and similar temperature-dependence.

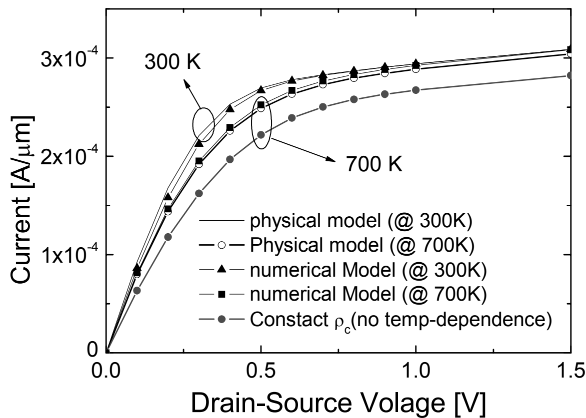

FIGURE 13. MOSFET *Ids vs Vds* curves(@ 300K and 700K) with various contact resistance models.

Fig.13 shows the simulated I_{DS}-V_{DS} curves at 300K and 700K for a 0.13 μm silicided NMOS transistor at V_{GS} 1.5 V using the two contact models. Assuming constant ρ_C in the numerical model, about 7~10% decrease in the drain current is observed as temperature rises from 300K to 700K, because the carrier mobility in the channel decreases at higher temperatures. However, taking the temperature dependence of ρ_C into account, this current decrease is considerably reduced in both of the two models, since the decrease of contact resistance at higher temperatures compensates the increase of the channel resistance. Fig. 14 shows the fraction of the drain current as a function of the position along the contact simulated with the two models at two different temperatures. It is observed that as temperature increases, current localization is more severe due to the reduction of contact resistance as predicted in [2], which may degrade the ESD robustness. It is shown again that the numerical model can reproduce the carrier transport behavior simulated by the fully physics-based hetero-junction model.

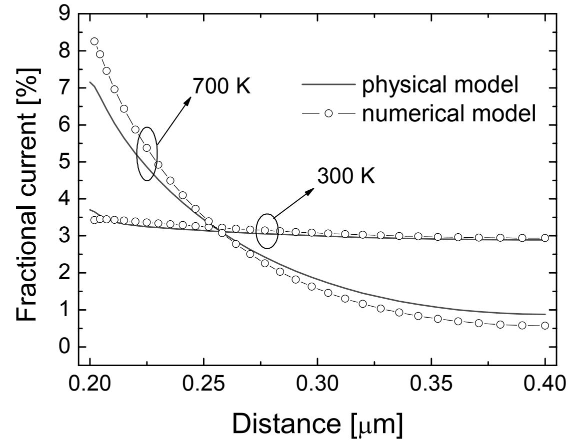

FIGURE 14. Fraction of the drain current as a function of the position from the edge of the spacer. Both contact resistance models implemented can predict current localization at high temperatures.

Conclusions

This work shows that for deep submicron silicided devices, the variation of the specific contact resistance has a major impact on ESD reliability through localized heating. For reliable electrothermal simulations of ESD, it is essential to trace the dynamic variation of contact resistance as a function of temperature within very short time periods. The temperature dependent contact resistance model is implemented in a device simulator and the validity of this model is checked with results for 0.13μm MOS transistors. The model is capable of predicting the high-current and high-temperature behavior and is useful for the analysis of ESD reliability.

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