Layout-Based 3D Solid Modeling of IC Structures and Interconnects Including Electrical Parameter Extraction

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Outline

- Background and Motivation
- System Configuration
- Layout-Based 3D Solid Modeling
- Level-Set Method for Surface Meshing of Complex Geometry
- Capacitance Extraction for a Four-Transistor SRAM Cell
- Summary and Discussion

Background and Motivation

Design Data

Layout (GDSII)
Process
information...

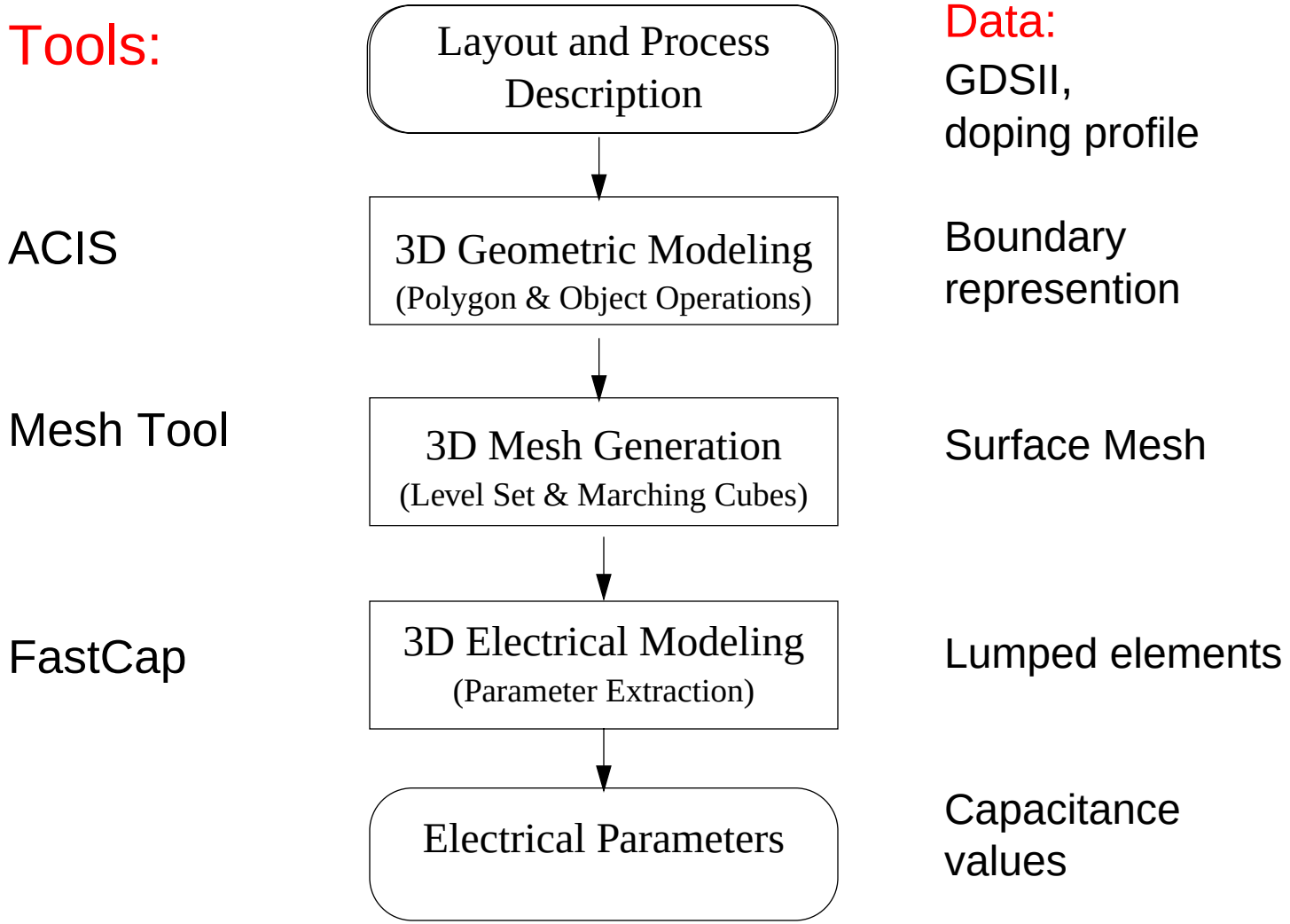
Electrical Parameters
and Circuit
Performance

Capacitance,
inductance,
cross talk, circuit
delay...

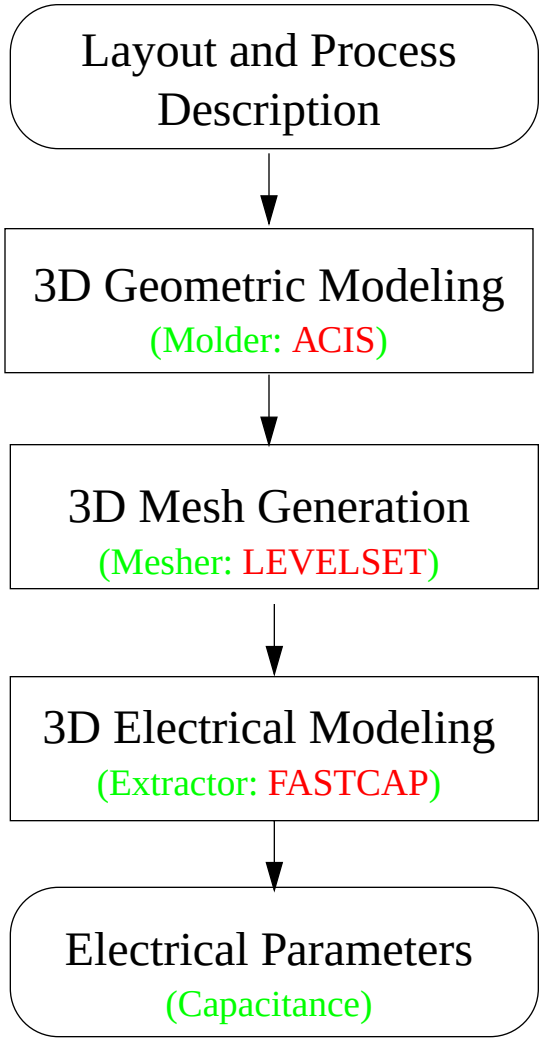
Background and Motivation

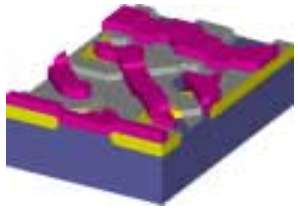
- Timely technology development requires the prediction of circuit performance based directly on the design data.
- Need to link directly the impact of layout and processing on the electrical characteristics of complex IC structures and interconnects.
- Current commercial tools are still evolving to provide abilities of modeling IC structures with complex 3D geometry.

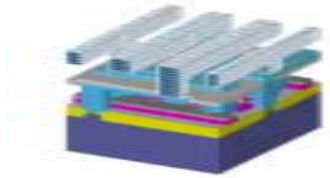
System Configuration

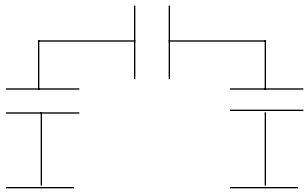


System Configuration









Layout-Based 3D Solid Modeling

- Generating input files for the geometry modeler to specify the structure of each component in a 3D object
- Running the geometry modeler to obtain description files for the geometry
- Converting the output files from the geometry modeler to geometry files readable to 3D visualization program
- Displaying and manipulating 3D image using the visualization program

Layout-Based 3D Solid Modeling

C code:

```
main(argc, argv)
   int argc;
   char *argv[];
{ ......
uniteObjs("sw_birdbeak", "oxide", fpo->file);
......
}
```

ACIS, Test Harness:

```
wire    clip \
        0.550  7.250 0.0 \
        0.550  7.250  0.450
sweep   wire frame2 along clip
move    frame2 \
        0.0 0.0 -0.225
subtract        frame2 from oxide as oxide
```

VRML format:

```
Transform {
translation -. 5 0 -. 5
children
DEF Leg Shape {
appearance Appearance {
material Material { diffuseColor Is legColor }
}}
}
```

AVS format:

```
geom_set_cur_cli_obj top
shell "ui" shell
panel Application -w app_panel -p ui -xy 0,0 -wh
        259,1024
panel "Top Level Stack" -w master_stack -p
        Application \
 -xy 2,100 -wh 256,595
```

Solid Modeling to Elec. Extraction

ACIS output:

(*.swracis files)

```
loop $-1 $-1 $22 $7 #
plane-surface $-1 0 4.25 0 0 1 0 0 0 1 0 #
shell $-1 $-1 $-1 $23 $8 #
face $-1 $24 $25 $9 $-1 $26 0 #
```

acis2br

Boundary representaion:

(*.f, *.v)

```
f 1 2 3 4
f 5 6 7 8
f 9 10 11 12

v 5 5.8 4.48
v 0 5.8 4.48
```

acis2ls

LevelSet input file:

(*.polyg)

```
facet
3
4.206570 1.793430 0.000000
4.206570 1.793430 -0.100000
4.431570 2.018430 -0.100000
```

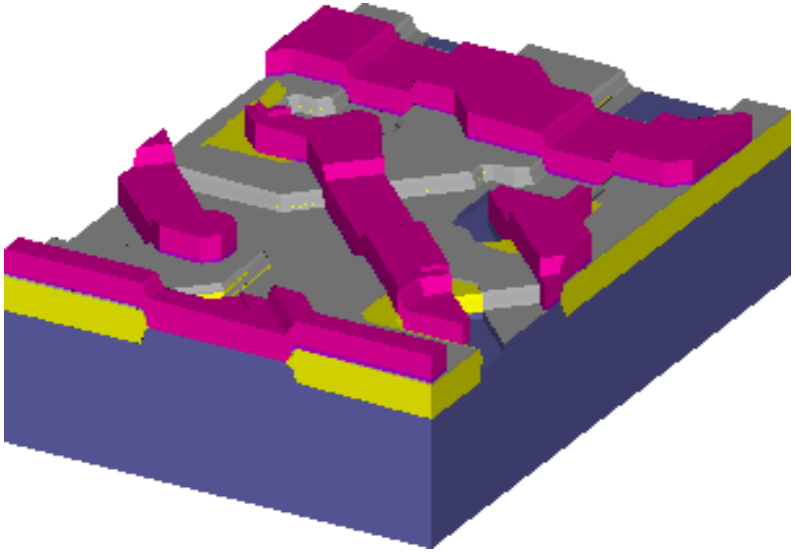
LevelSet

FastCap input file:

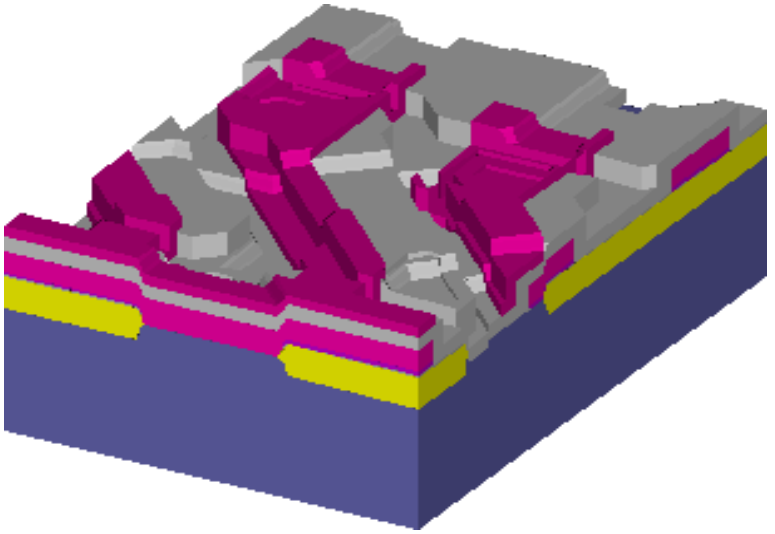
(*.dat)

```
Q 1 -0.15592 0.1338 0.3328
-1.2231 0.1133 0.5228
1.0001 0.9888 0. 3328
0.4002 0.8222 0.1233
```

Layout-Based 3D Solid Modeling



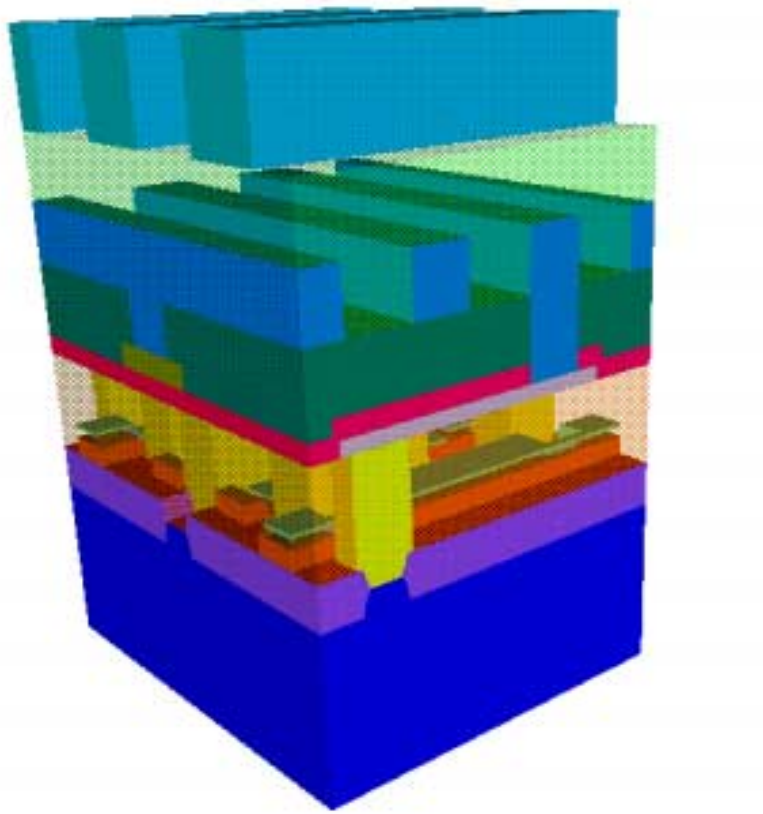
Solid geometry after the first poly layer is formed.



Solid geometry after the second poly layer is formed.

Layout-Based 3D Solid Modeling

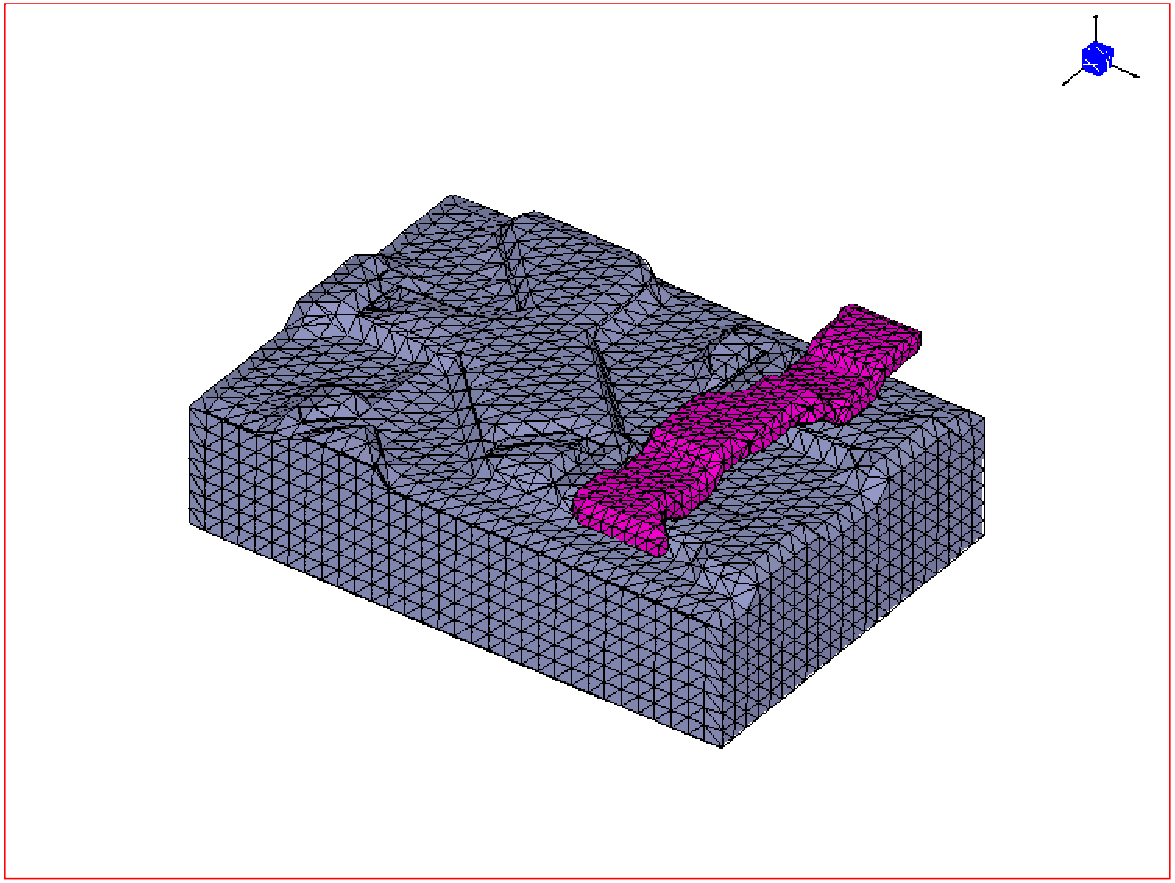
- SRAM in VRML format displayed by VRML browser across Internet with two insulating layers transparent



Level-Set Method for Surface Meshing of Complex Geometry

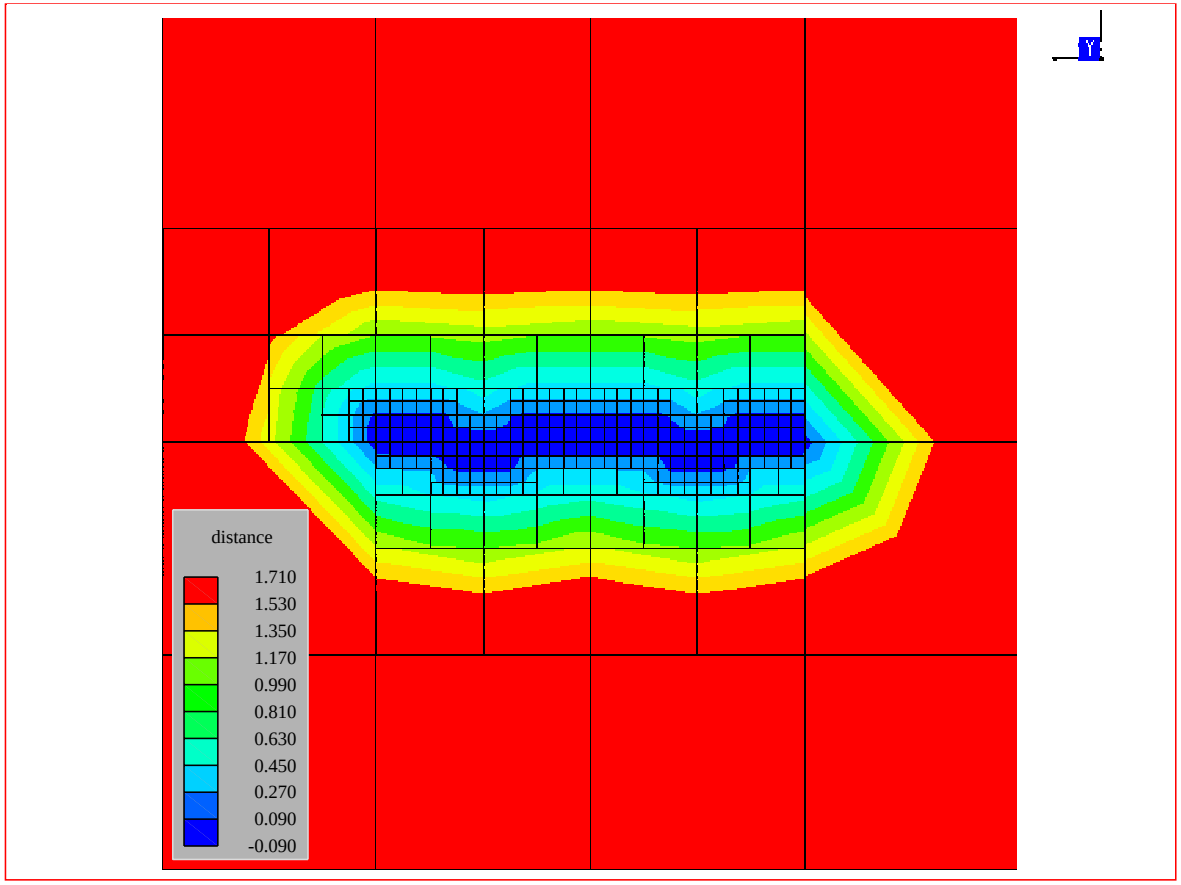
- Surface polygons from the solid modeler are triangulated into a coarse mesh.
- Octants containing the geometric object are subdivided recursively until a predefined refinement criteria is satisfied.
- Octants intersecting the surface are segmented into triangles.
- Local connectivity is extracted from the octree grid.

Level-Set Method for Surface Meshing of Complex Geometry



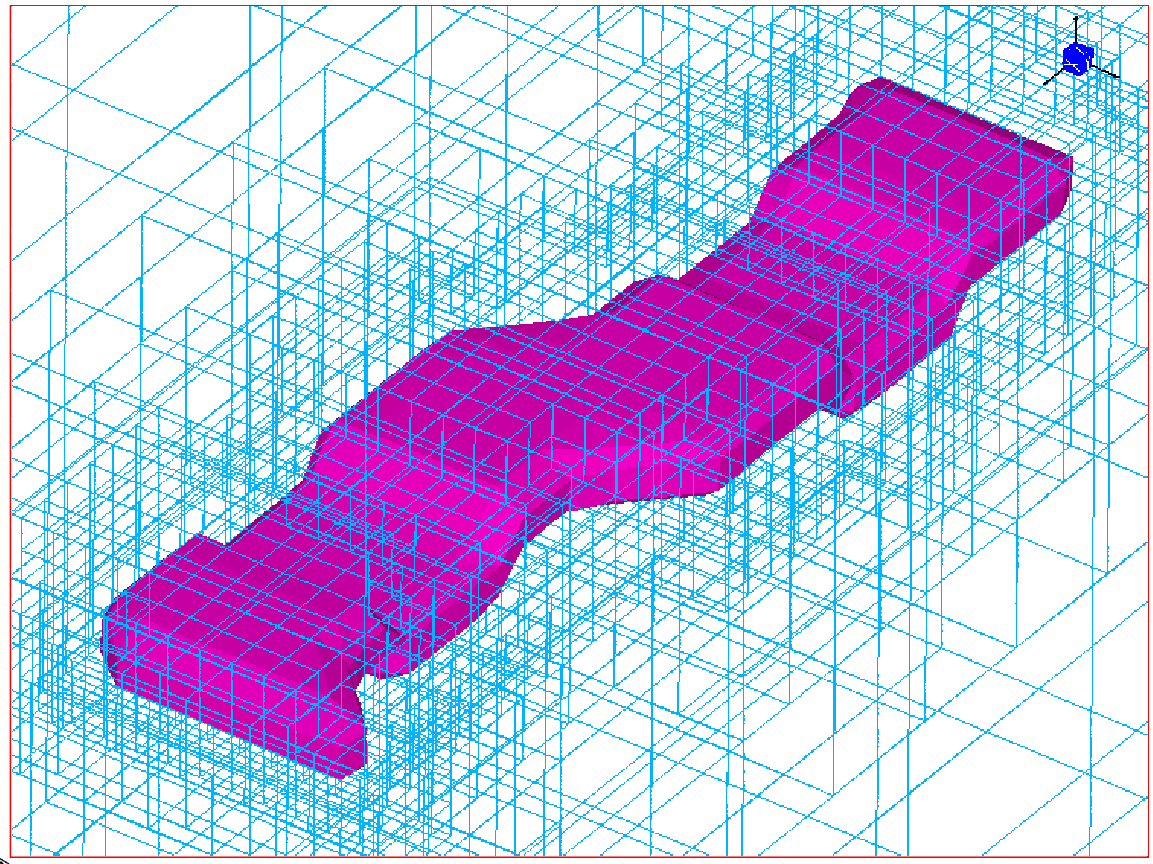
Word line in the SRAM cell

Level-Set Method for Surface Meshing (cont'd)



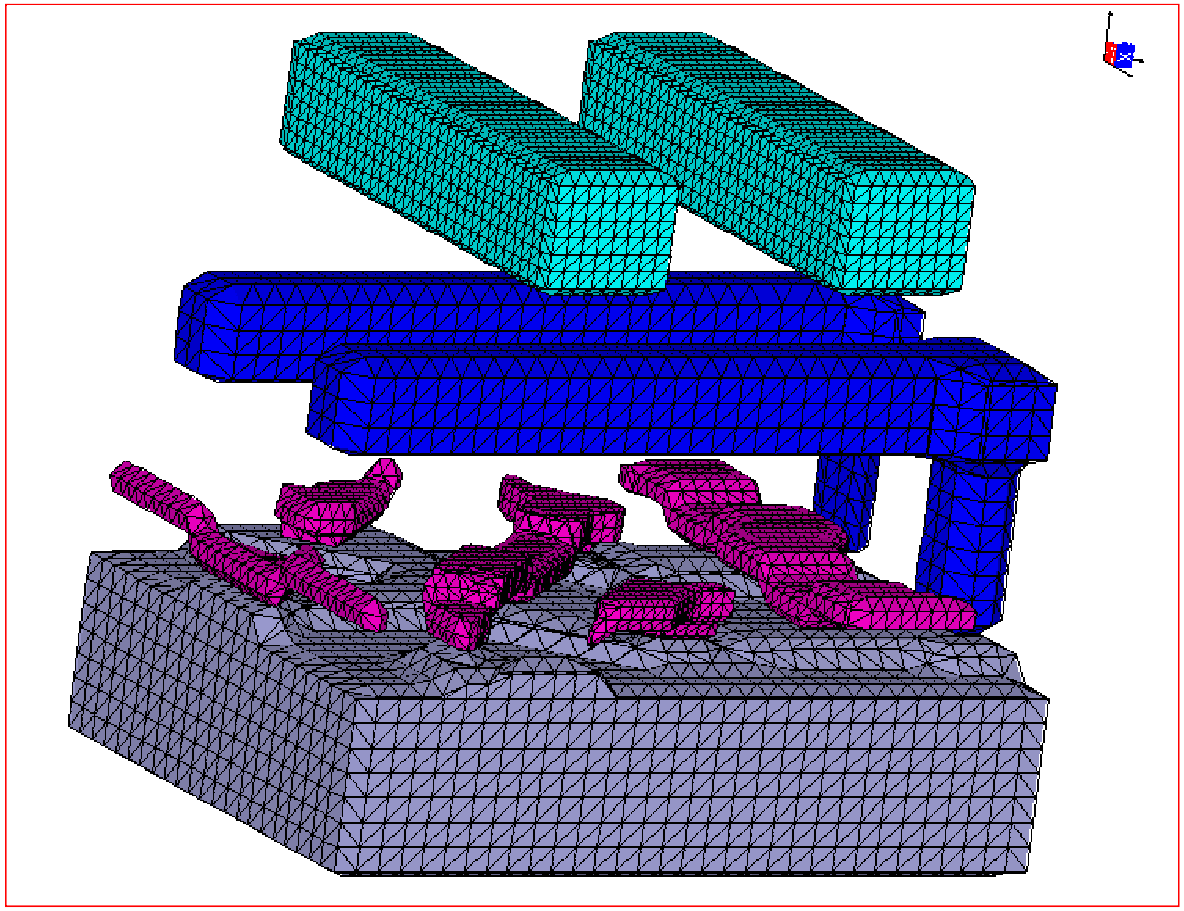
Mesh sectioning and distance contour for the word line

Level-Set Method for Surface Meshing (cont'd)



Iso-surface and octree for the word line

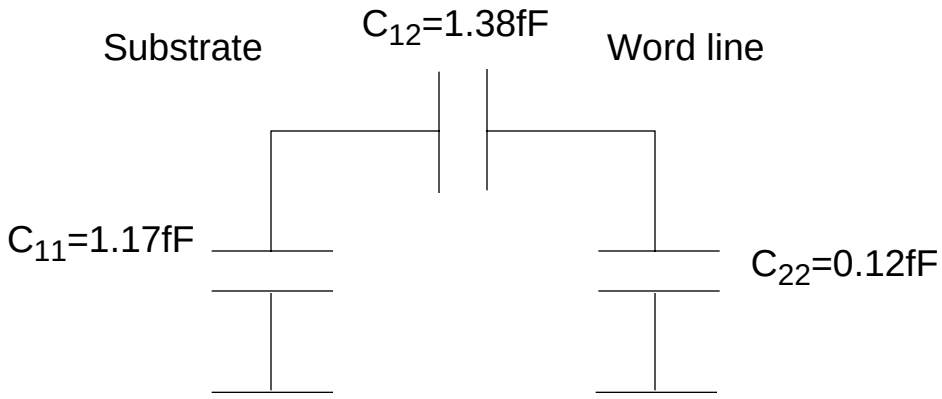
Level-Set Method for Surface Meshing (cont'd)



Mesh result for substrate, first poly layer and metal layers

Capacitance Extraction

- FASTCAP is used to analyze the realistic structures.
- The complete electrical model that FASTCAP provides for the word line vs. substrate:



Capacitance Extraction

- Capacitance among word line, bit lines and substrate:

Table 1: Capacitance Extraction Results (fF)

	substrate	word line	bit line1	bit line2
substrate	2.92	1.27	0.36	0.36
word line		1.57	0.12	0.13
bit line1			1.01	0.27
bit line2				1.02

Realized Link from Geom. to Elec.

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Conclusions

- A technology based interconnect modeling approach
- More realistic 3D geometry modeling which can be updated based on the design of layout and process specification
- More robust and efficient level-set meshing capabilities
- More accurate electrical parameter extraction based on realistic structures.

Related Work

- To model packaging parasitics (e.g. bonding wire's inductance) based on fast 3D geometry capturing (to be presented in IEDM '98, S.F.)
- To combine 3D solid modeling of package/ bonding-wire with compact model of RF power devices (BJT, LDMOS) to provide macro model for circuit simulation (SPICE, MDS)
- On-chip interconnect analysis including inductance and EMI.