Measurement and Simulation of Interconnect Inductance in 90 nm and Beyond

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Outline

• Background and Motivation
• Test Structures and Measurements in 90 nm
• Simulations of Inductive Impacts on Signal Delay and Noise in 90 nm
• Inductive Impacts in Future Technologies
• Conclusions
Background and Motivation

• On-chip inductance impact on signal integrity has been a problem for deep-submicron designs.
• Since wires are more resistive and capacitive in 90 nm technology and beyond, the impacts on timing and noise need to be investigated.

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<tbody>
<tr>
<td>130nm</td>
<td>150</td>
<td>107</td>
<td>76</td>
<td>54</td>
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<td>90nm</td>
<td></td>
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<tr>
<td>65nm</td>
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<tr>
<td>45nm</td>
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<tr>
<td>Metal Thickness(µm)</td>
<td>1.14</td>
<td>0.8</td>
<td>0.56</td>
<td>0.39</td>
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Test Structures and Measurement

The chip layout in 90 nm

M9 - Signal - Gnd

Substrate

Network Analyzer

Probe Station
Measured and Simulated S-Parameters
(A Two-Return Structure)

Measured $S_{11}$

Simulated $R (S_{11})$

Simulated $Im (S_{11})$

Simulated $Re (S_{11})$

Extracted RLC (RAPHAEL)

A Circuit Macro Model

Relative Error < 5%

SISPAD, Sept. 2005, Tokyo
Inductive Impact on Clock Timing

Transistors:
- \( Gate_L = 0.1 \, \mu m \)
- \( W_{N(clk)} = 12 \, \mu m \)
- \( W_{N(sig)} = 3.8 \, \mu m \)

Wire length: \( 1500 \, \mu m \)

Routing Cross-Section

Driver input

Clock far end (Aggres. switching against clock)

Clock far-end

11 ps

Clock far end (Aggres. switching w/ clock)

0.56 \( \mu m \)

0.28 \( \mu m \)
Inductive Impact on Bus Noise

- Measured Here
- Noise at victim far end
- One of aggressor’s driver outputs
- M6 width and space: 0.56 µm
- M4 width and space: 0.28 µm
- Wire length: 1500 µm

Routing Cross-Section:
- Victim
- Gnd
Inductance Variations Due to Process Variations

\[
L_{\text{self}} = \frac{\mu_0 l}{2\pi} \left[ \ln \frac{2l}{(w + t)} + \frac{1}{2} \right]
\]

\[
\frac{\partial L_{\text{self}}}{\partial w} = \frac{-\mu_0 l}{2\pi(w + t)}
\]

Wire length: 1500 \( \mu \text{m} \)
RC Delay and RLC Delay in 90 nm

Coplanar clock wires in M8
Width = 2 µm, RLC extracted at 3GHz

\[ T_d = 0.5 \times R_{\text{line}} C_{\text{line}} \]

\[ T_d = \sqrt{L_{\text{line}} \times C_{\text{line}}} \]
Inductance Impact in Future Technologies

Clock wire in M8 and simulated at 3 GHz

- **Length2**: $LC$ Delay = $RC$ Delay
- **Length1**: $LC$ Delay = Transistor Delay

Inductance prominent
Conclusions

• Interconnect $RLC$ circuit macro models are bench-marked by measurements in 90 nm technology.

• Simulations reveal significant inductive impacts on clock timing and bus signal noise.

• The analysis shows that inductive impact on interconnect delay and cross-talk will not be alleviated in the 65nm and 45nm technologies.