Measurement and Simulation of Interconnect Inductance in 90 nm and Beyond

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Outline

- Background and Motivation
- Test Structures and Measurements in 90 nm
- Simulations of Inductive Impacts on Signal Delay and Noise in 90 nm
- Inductive Impacts in Future Technologies
- Conclusions

Background and Motivation

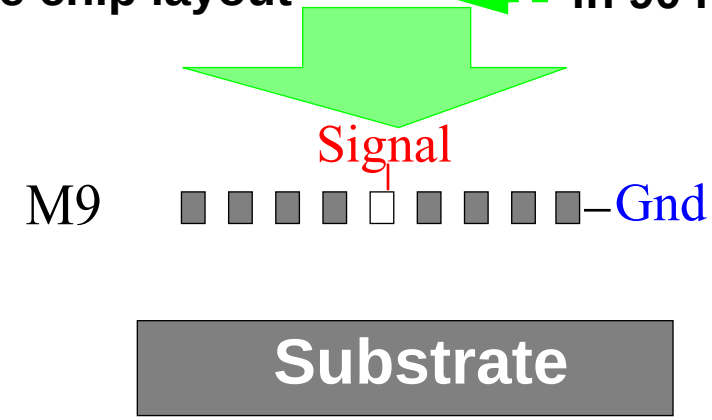
- On-chip inductance impact on signal integrity has been a problem for deep-submicron designs.
- Since wires are more resistive and capacitive in 90 nm technology and beyond, the impacts on timing and noise need to be investigated

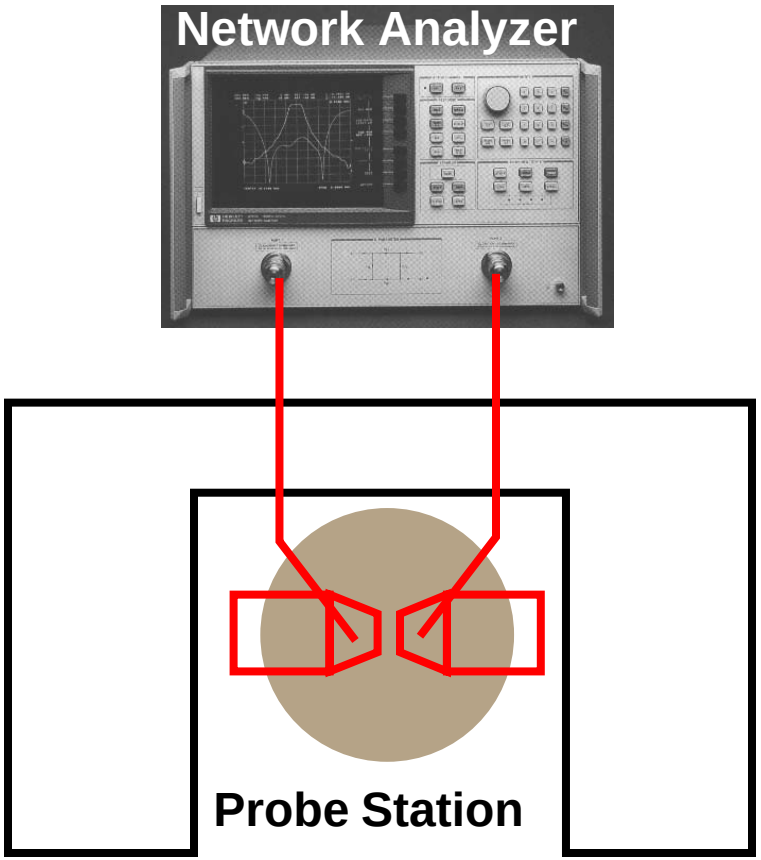
	2001	2004	2007	2010
Tech. Node	130nm	90nm	65nm	45nm
M1 1/2 Pitch (nm)	150	107	76	54
Metal Thickness(μm)	1.14	0.8	0.56	0.39

From ITRS'04

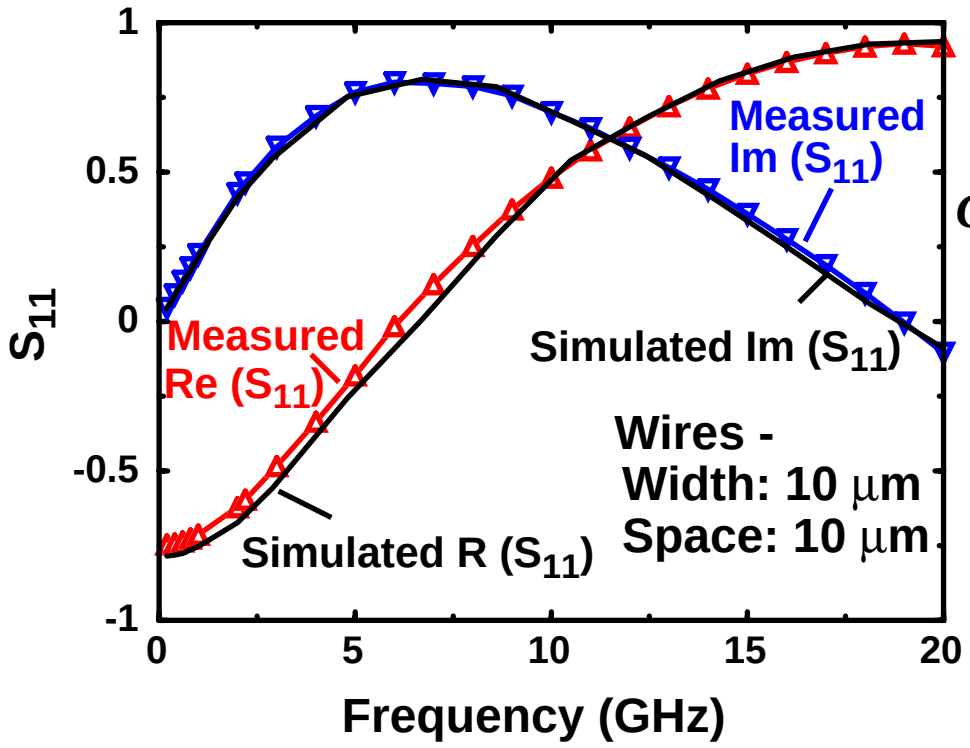
Test Structures and Measurement

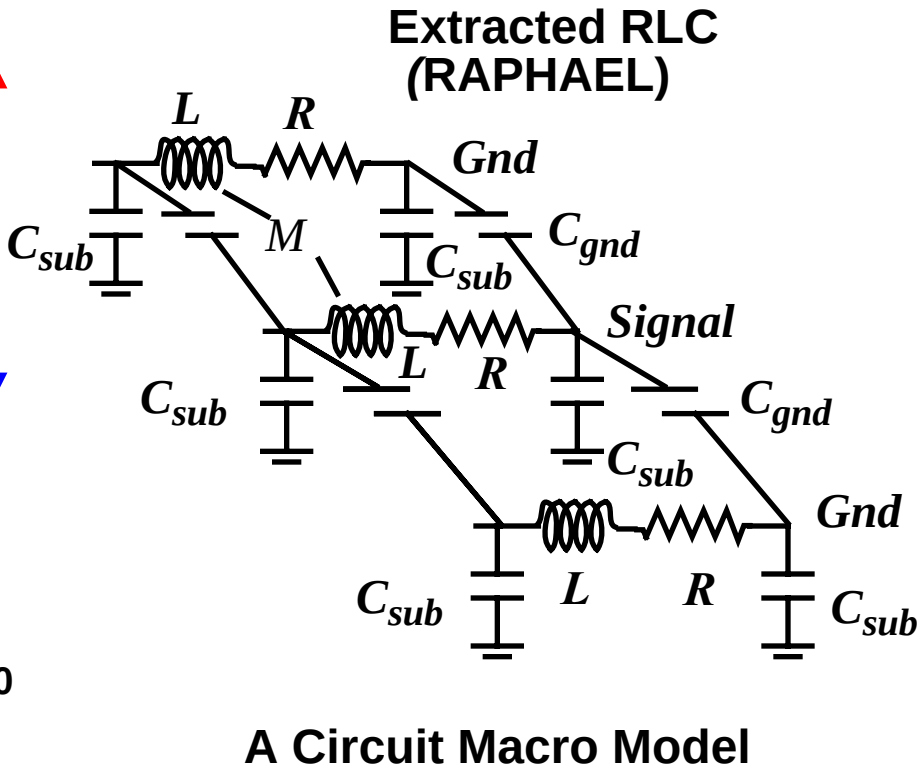
The chip layout in 90 nm





Measured and Simulated *S*-Parameters (A Two-Return Structure)

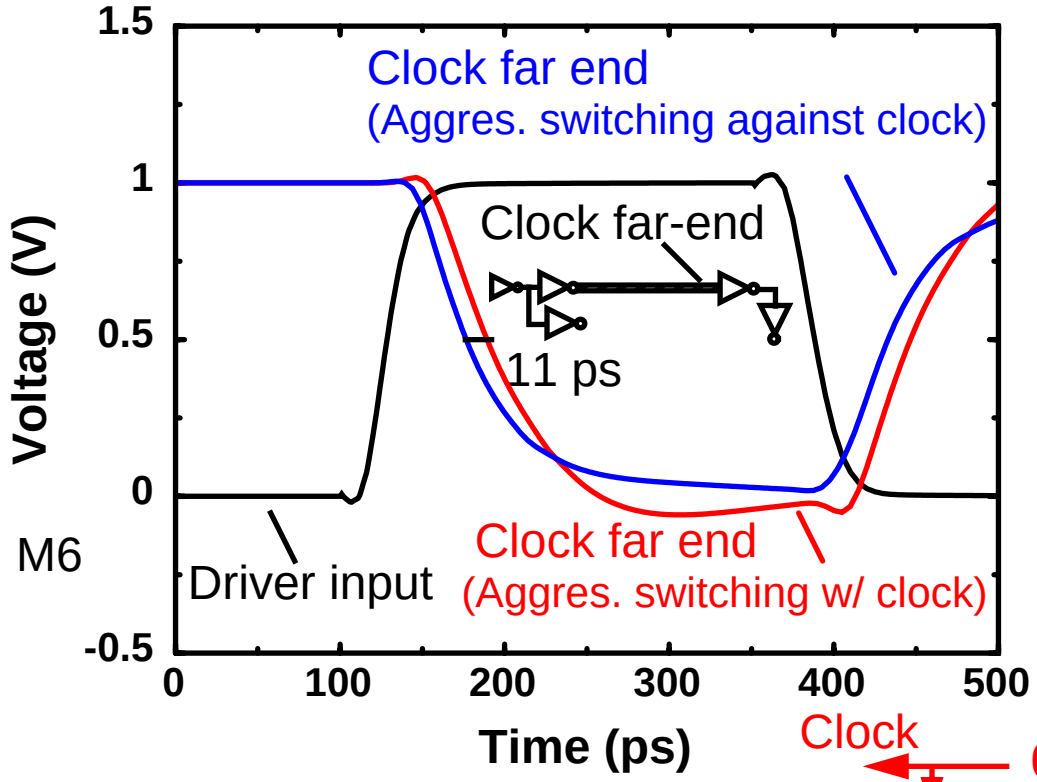




A Circuit Macro Model

Relative Error < 5%

Inductive Impact on Clock Timing



Transistors:

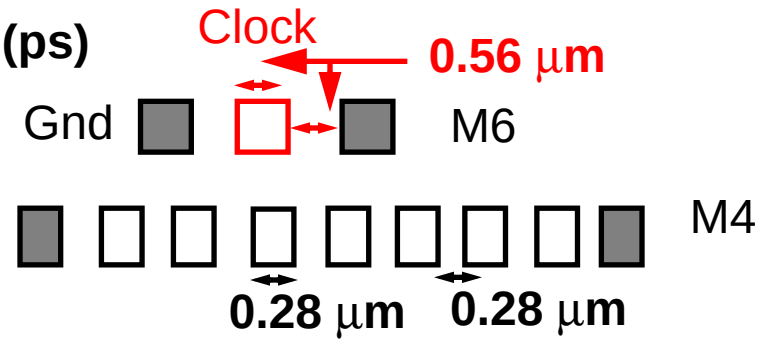
$Gate_L$ = 0.1 μm

$W_{N\,(clk)}$ = 12 μm

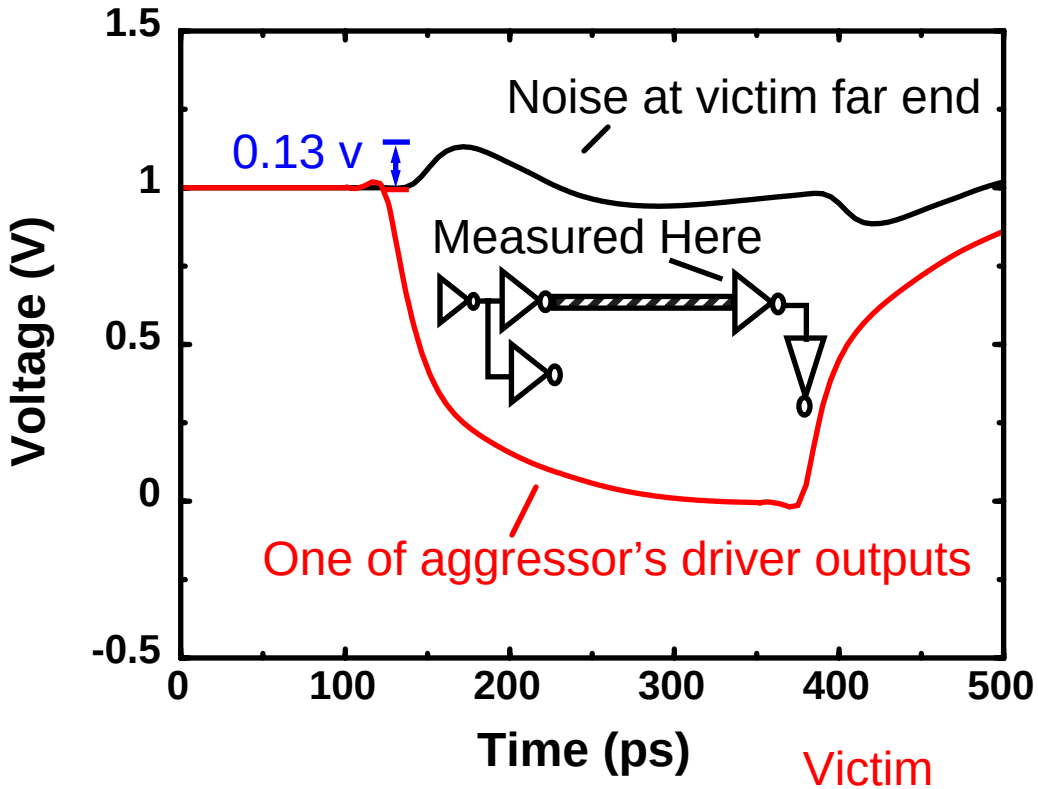
$W_{N\,(sig)}$ = 3.8 μm

Wire length: 1500 μm

Routing Cross-Section



Inductive Impact on Bus Noise

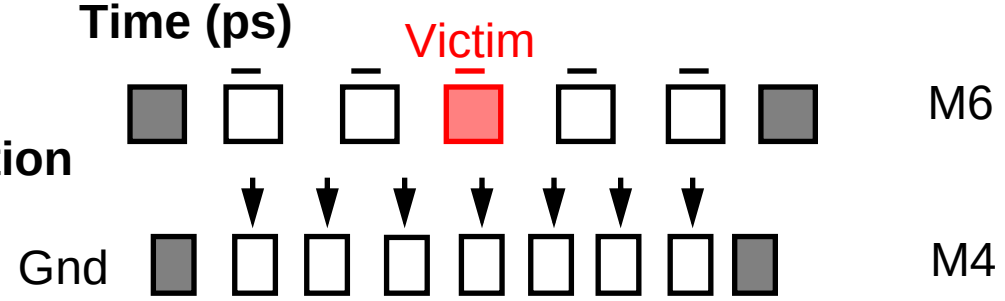


M6 width and space: 0.56 μm

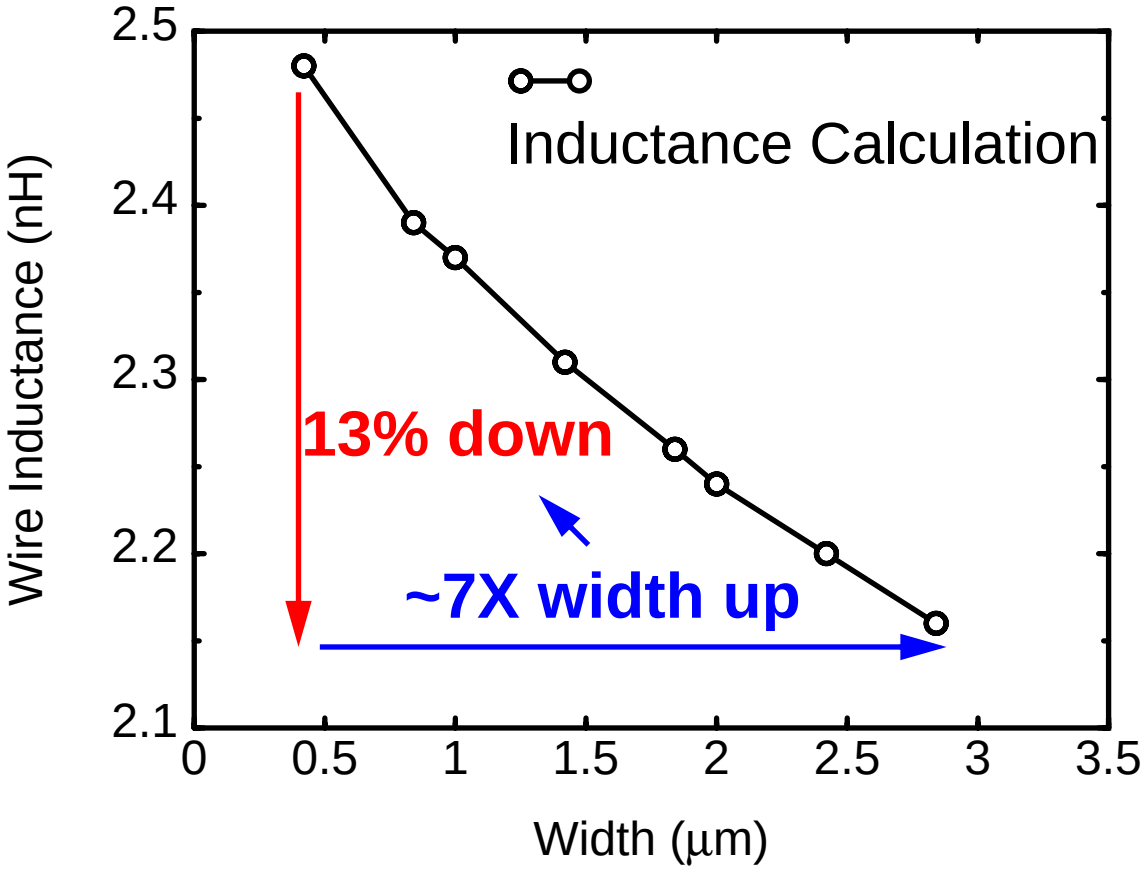
M4 width and space: 0.28 μm

Wire length: 1500 μm

Routing Cross-Section



Inductance Variations Due to Process Variations

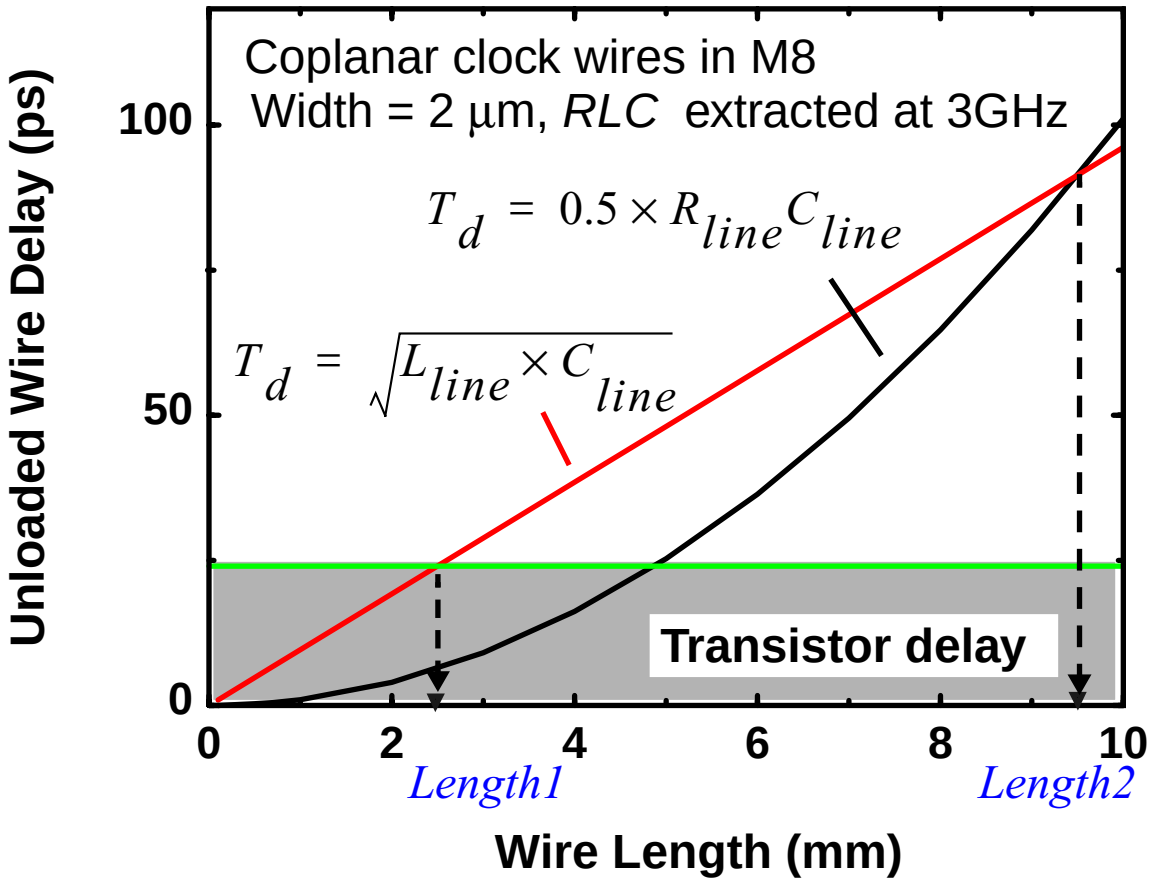


$$L_{self} = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{(w+t)} + \frac{1}{2}\right]$$

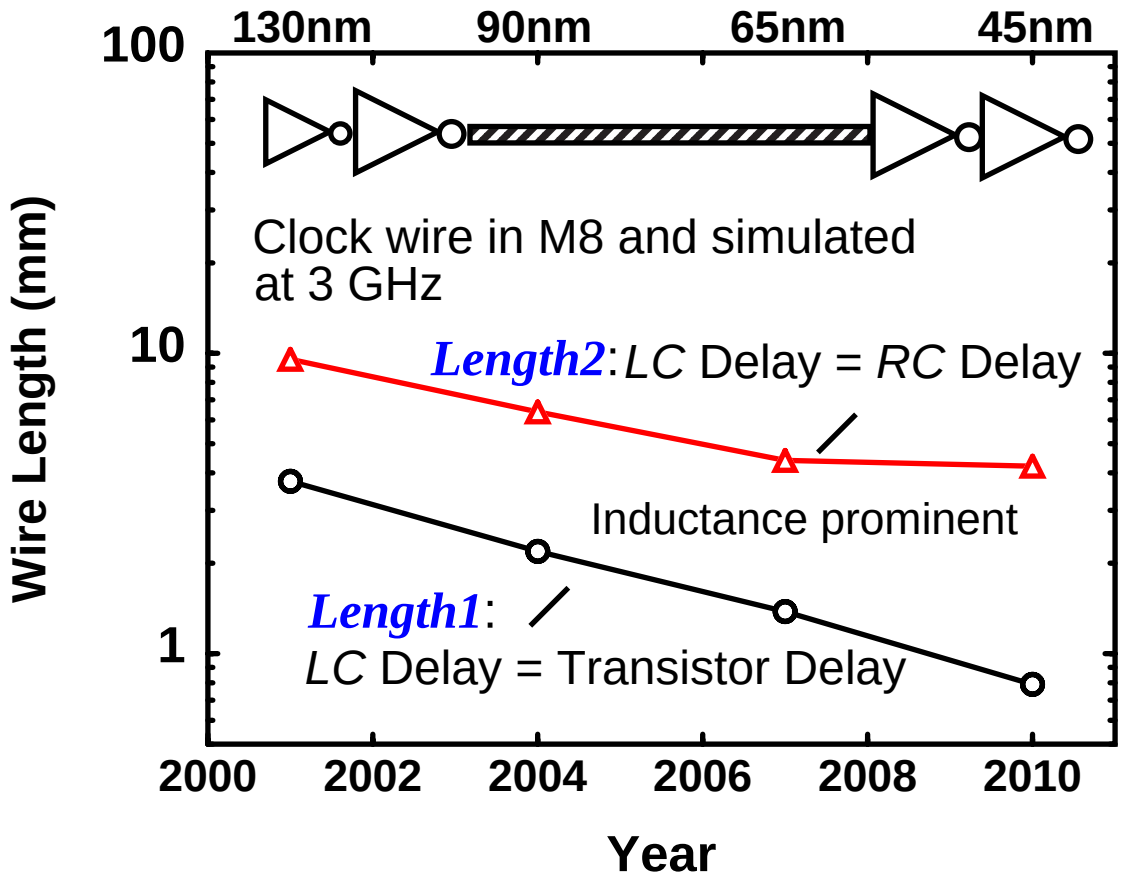
$$\frac{\partial L_{self}}{\partial w} = \frac{-\mu_0 l}{2\pi(w+t)}$$

Wire length: 1500 μm

RC Delay and *RLC* Delay in 90 nm



Inductance Impact in Future Technologies



Conclusions

- Interconnect *RLC* circuit macro models are bench-marked by measurements in 90 nm technology.
- Simulations reveal significant inductive impacts on clock timing and bus signal noise.
- The analysis shows that inductive impact on interconnect delay and cross-talk will not be alleviated in the 65nm and 45nm technologies.