High Frequency Characterization and Modeling of VLSI On-Chip Interconnects

Xiaoning Qi*, Bendik Kleveland†, Gaofeng Wang‡, Zhiping Yu, Simon S. Wong, Robert W. Dutton
Center for Integrated Systems, Stanford University
Stanford, CA 94305

Takeshi Furusawa
Central Research Lab. Hitachi, Ltd.,
Tokyo, 185-8601, Japan

Abstract— Modeling of on-chip inductance for chips with realistic power/ground wires and grids is presented. Analytical formulae as well as field solvers are used to analyze inductance of on-chip structures including power/ground grids, ground plane and substrate effects. Insights and design guidelines to reduce wire inductance are demonstrated. An accurate capacitance modeling approach is also presented.

I. Introduction

As semiconductor technology continues to scale, wires, not devices, gradually dominate the delay, power and area of microprocessors and ASIC designs. The constant increasing clock frequency combined with increased chip area results in the ratio of global wire delay to gate delay increasing at a super-linear rate. For sub-0.25 μm technology at gigahertz-scale clock frequencies, interconnects may exhibit transmission line behavior. This has spawned the need to accurately model the parasitics – resistance, inductance and capacitance – for on-chip wires.

In the analysis phase of design, lower metal layer's short on-chip wires can be modeled as lumped capacitive loads and longer wires can be modeled as lossy RC transmission lines. Any wire whose resistance is small compared with the impedance of the circuit driving it can be considered short. Because of their relatively high resistivity, short length, and tight pitch, lower metal layers on-chip wires almost have inductance values that are sufficiently low to be safely ignored. In modern IC technology with clock frequencies reaching the multi-gigahertz regime, long global interconnects on upper metal layers exhibit RLC transmission line effects. By using wider wires on upper metal layers for critical signal nets, such as clocks, and using copper interconnects, the wire resistance is reduced. As a result, the inductive impedance part, ωL, becomes comparable to the wire resistance, R. For these interconnects, inductance can no longer be ignored and needs to be carefully modeled. Inductive effects have been demonstrated in long wires in a 0.25 μm process and future technology generations [1]. For short wires, as the *time of flight* of the wires is smaller than the signal rise/fall time or gate delay (X_{GATE}), they can be modeled as RC elements. On the other hand, as the wire length is long enough so that the RC delay of the wire exceeds the propagation delay of a lossless electromagnetic wave along the wire (X_{WAVE}), this long wire can also be modeled as RC elements. Wires with length between these two cases are the wires which need to be modeled as RLC transmission lines. When technology advances, the inductive effects will affect progressively shorter wires as illustrated in Fig. 1. In addition, inductive crosstalk, especially for bus structures can no longer be ignored. Circuit simulations show larger noise and ringing of signal crosstalk due to inductive couplings.

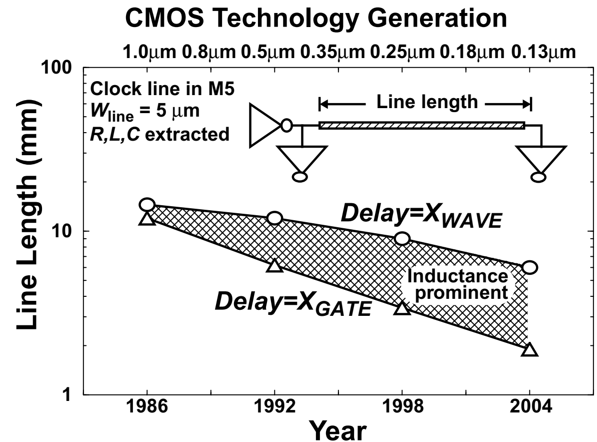


Fig. 1. Inductive effects vs. technology scaling. As technology advances, the wire length range where inductance is important becomes larger.

*Now with Sun Microsystems, 901 San Antonio Rd., USUN02-101, Palo Alto, CA 94303-4900
†Now with Matrix Semiconductor, 3230 Scott Boulevard, Santa Clara, CA 95054
‡Now with Intpax, 6 Results Way, Cupurtino, CA 95014

The most important milestone of on-chip inductance calculation came with the work of A. E. Ruehli who proposed *Partial Inductance* or *Partial Element Equivalent Circuit* (PEEC) concepts [2] [3]. Kamon and White used the partial inductance concepts and developed FASTHENRY to automate the inductance calculations [4]. Recently, the identification and modeling of on-chip transmission line effects have been reported by IBM researchers [5] [6] [7]. These papers pointed out the transmission line and inductive effects for on-chip interconnects using test chips and time domain analysis. In recent years, major industry microprocessor designs, such as Intel's Itanium and Compaq's Alpha chips, were reported to have to model the on-chip inductance [8] [9] [10] – both used co-planar waveguide structures, or ground plane for critical clock and signal wires to reduce inductance effects at the cost of chip area. Extraction methods based on applying a field solver to generate look-up tables and equivalent circuits for high frequencies have been reported [11] [12] [13]. Restle [14] presented IBM's full-wave extraction and simulation methods at DAC'99. Another practical approach for extracting approximate inductances of on-chip interconnects was reported by Shepard [15], which models signal and power/ground wires independently and localizes inductive coupling by assuming currents only return via nearby power and ground wires. With extracted inductances, signal integrity and delay optimization can be studied. Huang[16] and Cao [17] reported RLC signal integrity analysis and analytical models of noise and delay for high speed on-chip global interconnects. Analytical propagation delay formulae including inductance are studied and repeater insertion techniques were also proposed by [18]-[20], [21].

In this paper, characterization and modeling for VLSI on-chip interconnect including inductance and capacitance are presented. Design insights are obtained based on the detailed analysis of eletromagnetic fields of test chips. After some methodology introduction for simulation, inductance modeling for coplanar structure and power/ground grids is presented, followed by modeling of ground plane effects on inductance. Then, capacitance extraction is discussed. Finally, conclusions are summarized.

II. Simulation for Multi-Conductor Systems

It is well-known that capacitance is a quantitative measure of the ability of a conductor configuration to hold charge per unit applied voltage, or store electrical energy, and is a property of the physical arrangement of the conductors. Inductance is a measure of the ability of a conductor configuration to link magnetic flux, or store magnetic energy and is another property of the *physical layout* of the conductors [22]. To calculate inductance in a multi-conductor system, knowledge of the *physical* configuration of all conductors in the system is necessary. The frequency dependency of inductance comes from eddy currents which are induced by time varying magnetic fields and governed by *the law* of induction – Faraday's Law. Eddy currents manifest themselves as skin effects and proximity effects. In the case of skin effects, the eddy currents (or redistribution of time varying current) flowing through the cross section of a certain conductor is due to its own field, causing the current to flow near the surface of the conductor. By contrast, proximity effects take place when a conductor is subjected to a time-varying field due to the neighboring conductors [23]. To model interconnect capacitance, both capacitance to the ground/substrate as well as capacitance to the neighboring wires need to be taken into account.

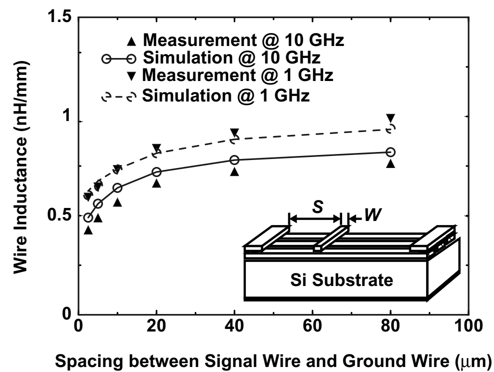


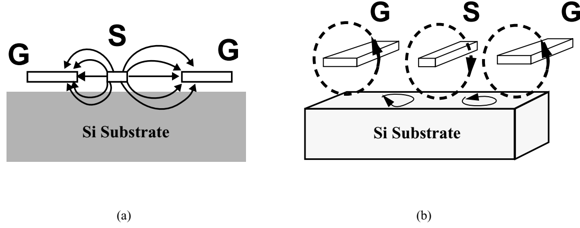
Fig. 2. Measurement and simulation comparison: inductance vs. wire spacing. The signal wire width is 6 μm. The ground wire width is 16 μm.

Because of complex multi-conductor configurations, long interconnects and fast signal rise and fall times, distributed circuit models consisting of R, L, C are required to predict signal delay or crosstalk. The R, L, C for each small segment can be obtained by partitioning the conductors into smaller segments, dimensions of which are much smaller than the wavelength of the significant frequency of the signals (e.g. 250 μm in current technology) [24].

III. Inductance Modeling for Coplanar Structure

A. Wire Inductance

A test structure, named as the coplanar conventional test structures, consist of coplanar waveguide structures on upper metal layers and some vertical wires on a lower metal layer. The coplanar waveguide structure is on the fifth metal layer which is about 5 μm above the substrate. Measurement results and FASTHENRY simulations for the coplanar conventional test structure are compared in Fig. 2. Analytical formulae are also derived to estimate the wire inductance [25]. Fig. 2 shows that inductance increases monotonically with the *spacing* between the wire and the nearest ground wire of the coplanar structure.



(a) (b)

Fig. 3. (a) Electric field couples to the substrate. (b) Magnetic field couples to the substrate shown by dashed lines. Eddy currents are also shown within the substrate.

Most current returns through the nearest ground wire for small spacings. For large spacings, return current is distributed between the two ground wires, which increases the current return loop and hence inductance. At higher frequencies, the inductance is decreased due to the proximity effects between the wires as well as between the wire and the substrate, which is more evident from the measurements.

B. *Substrate Effects on Wire Inductance*

The substrate is usually grounded, and the electromagnetic field of the signal wires can be coupled into the substrate at high frequencies. Electric fields couple to the substrate, generating conducting currents and displacement currents that flow both laterally and vertically. Time-varying magnetic fields couple to the substrate, generating eddy currents that flow parallel to the device above the substrate as shown in Fig. 3. As a result, the substrate can offer a portion of the return paths for current. With the eddy currents, the substrate can reduce wire inductance, especially for a highly conductive substrate. This phenomenon is evident for the wires without intermediate metal layers between the wires and the substrate. In this case, there is no shielding effects of the electromagnetic field of the wires, which might, otherwise, prevent the electromagnetic waves from penetrating into the substrate. It is more evident for the heterogeneous integrated IC microsystems where an additional substrate may exist above the upper metal layers.

Approximations can be made to have rough inductance estimation for some structures like the coplanar waveguide. To model the substrate effect, it can be treated as a return path beneath the signal wire according to proximity effects at high frequencies. The revised formula, including substrate effects, has the form (unit H/m):

$$\hat{L}_{coplanar} - k\frac{\mu_0}{2\pi}\left(\ln\sqrt{(\left(\frac{s+\frac{w_{gnd}+w}{2}}{h+\frac{1}{2\sqrt{\pi f\sigma\mu_0}}}\right)^2+1+A}\right) \quad (1)$$

where $A = \frac{1}{2}ln\left(\frac{\pi(s+\frac{w_{gnd}+w}{2})}{2(w_{gnd}+t)}\right)$. The $\hat{L}_{coplanar}$ is the inductance without substrate effects, h is the distance of

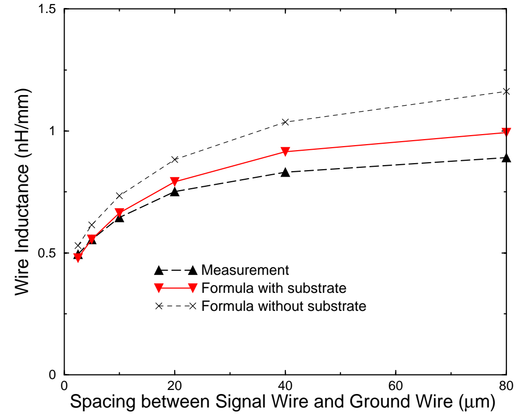


Fig. 4. Wire inductance with substrate effects. The substrate resistivity, ρ_{sub}, is 0.015 Ω-cm.

metal layer (center) from the substrate, w_{gnd} is the width of the ground wires, σ is the conductivity of the substrate, f is the signal frequency, s, w and t are the spacing between the signal wire and the nearest ground wire, signal wire width and thickness. k is the percentage of current returned via the substrate. When the spacing between signal wire and ground wire is larger than 20 μm, with a ground wire pitch of 251 μm, more current tends to return via the substrate (i.e. the proximity effect) which forms a smaller current loop, resulting in a reduction of wire inductance as shown in Fig. 4. This effect becomes more prominent for less resistive substrates.

IV. Inductance Modeling for Test Structures with Power/Ground Grids and Floating or Grounded Grids

For VLSI digital chips, power and ground are usually distributed through grid structures in order to minimize IR drops as well as to reduce ground bounce. Test chips with representative power and ground grids [1] have been used to study effects of these various parameters on inductance. Due to proximity effects, the nearest power and ground wires provide the return paths for most of the signal current through coupling. Since grid perpendicular to the signal wires do not contribute to the signal wire inductance (their mutual inductance is zero), only grid parallel to the signal wires are needed to calculate the signal wire inductance. Simulations and measurements show that, with the substrate excluded, multiple parallel (with signal wires) ground wires in ground grids reduce signal wire inductance because of the multiple parallel current return paths. However, if the substrate is included, the nearest ground wires and substrate dictate the current return paths. In this case, multiple parallel ground wires in the grid cannot effectively reduce signal wire inductance. To accurately calculate a signal wire inductance, nearby signal wires can be included in the simulation. Nearby wires

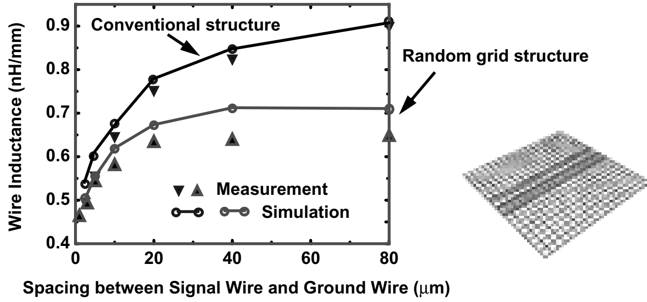


Fig. 5. Measurement and simulation: wire inductance at 3 GHz is reduced with floating grids on M1 and M2. The signal wire width is 5 μm. A random grids structure is shown on the right.

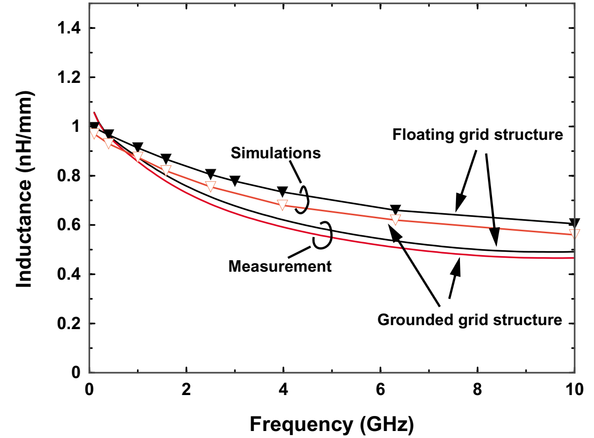


Fig. 6. Frequency dependency of wire inductance with floating or grounded grids on M1 and M2 layers.

terminated by large impedance values to the ac ground can be approximated as floating wires. They do not affect the signal wire inductance if these wires have widths smaller than 20 μm so that their eddy currents are small enough to be ignored; nearby wires terminated to the ac ground can be treated as ground wires. All the nearby wire effects on inductance can be incorporated into one signal wire inductance which can be used in circuit simulation for delay analysis. However, for crosstalk analysis in circuit simulation, partial inductance and partial mutual inductance of signal wires as well as nearby wires are needed. In the digital chip environment, if there are dense grids or ground planes on a given metal layer, they can generate eddy currents due to the existing time-varying magnetic field. A ground plane can shield electromagnetic fields and also offer current return paths for the signal current. In these cases, the signal wire inductance can be reduced significantly due to the return current and eddy currents in the dense grid or ground plane. Electromagnetic field solvers, such as FASTHENRY, can be used to simulate the eddy current effects based on constructed 3-D geometries of grids or ground planes. Fig. 5 compares the results of the conventional test chip with the results from a test chip which has coplanar waveguide structures on the fifth metal layer, and dense grids on the first and second metal layers across the chip. The chip is referred to as the random grid structure. For the conventional structure, inductance increases as the spacing to the nearest ground increases; while for the random grid structure, the inductance saturates around 20 μm and becomes independent of the spacing at larger spacings. The magnetic flux generated by eddy currents in the random grids opposes the magnetic field change, thus reducing the magnetic flux of the signal wires, and effectively reducing the inductance of the signal loop. The dense grids effectively change the electromagnetic field configuration in a manner similar to a continuous ground plane. As a result, wire inductance is primarily determined by the spacing from the wire to the grids. Each cell of the grids is about $15\mu m \times 15\mu m$. When the spacing between the signal wire and the nearest ground wire exceeds about 15 μm, the signal loop couples to the eddy current loops in the grids, and the effective magnetic flux is reduced. Fig. 6 shows the frequency dependency of the inductance. As the frequency goes up, the inductance decreases due to the time varying nature of the eddy currents. The same phenomena can be observed in the simulations and measurements if the grid structure is replaced by a continuous ground plane. Whether the grid structure is floating or grounded, it does not make much difference in the wire inductance due to the eddy current effects.

V. Ground Plane Effects on Wire Inductance

For VLSI chips, a ground plane sometimes is purposely designed and inserted between metal layers to shield electromagnetic waves in order to control the wire inductance of critical signal, clock and power nets. A densely populated grid structure, as seen in Section IV,. also exhibits ground plane effects. A ground plane alters electromagnetic fields due to the boundary conditions at the surface of the plane which need to be satisfied. For example, the electric field $\mathbf{E}$ must be perpendicular to the ground plane in the case of a perfect conductor. One major ground plane effect is that wire inductance is significantly reduced because of a more confined electromagnetic field, resulting shielding of signals. There are several previous studies of ground plane effects on wire inductance for PCBs. For example, microstrip lines have been studied by many groups. However, due to the nature of the problem, an exact analytical analysis is not possible for the general case of a microstrip of width w with finite thickness t [26]. Approximations have to be made to obtain a good estimation – for example the strip has to be assumed a very thin, perfect conductor carrying a transverse electromagnetic mode (TEM) wave. Some results for PCBs can not be directly used for on-chip interconnects because of geometry assumptions used in the derivation. Electromagnetic field solvers such as Maxwell [27] can be used to numeri-

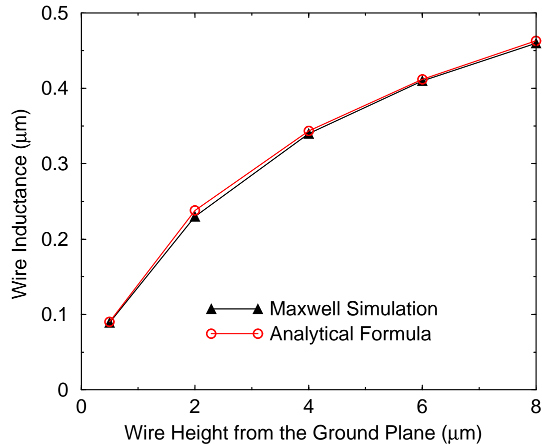


Fig. 7. A wire over a ground plane: Equation (4) results are compared with Maxwell simulation results. Wire height is the distance from the bottom of the wire to the top surface of the ground plane. The signal wire width is 5 μm and the thickness is 0.5 μm for both the signal wire and ground plane.

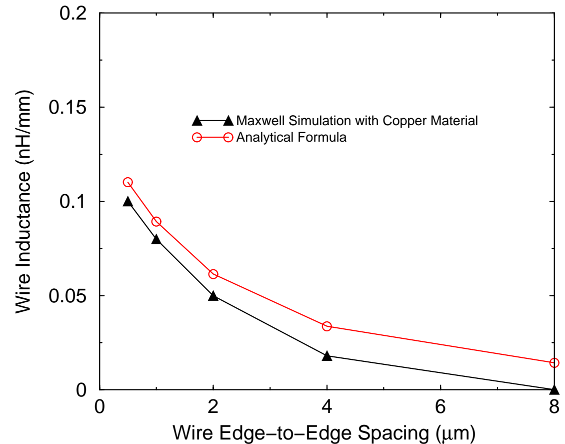


Fig. 8. Two wires over a ground plane: Mutual inductance results from Equation (3) are compared with Maxwell simulations with copper material at 3 GHz. The width of the two wires is 5 μm.

cally extract the inductance of this structure. To quickly estimate the inductance of wires over a ground plane and establish design insight, analytical formulae are desirable. Inductance estimations can be obtained from formulations of the characteristic impedance for transmission lines and their relationship with distributed inductances. It can be shown that the loop inductance of a wire over a ground plane is

$$L = 0.2 \ln \frac{2\left(h + \frac{t}{2}\right)\pi}{w + t} \text{nH/mm} \tag{2}$$

and the mutual inductance of two wires on a ground plane is

$$M = 0.2 \ln \left[1 + \left(\frac{2\left(h + \frac{t}{2}\right)}{D} \right)^2 \right] \text{nH/mm} \tag{3}$$

where h is the wire height (from the bottom of the wire) to the ground plane, w and t are the width and thickness of metal wire, and D is the center-to-center wire separation. To model the case when $h = 0$, an extra term Δ needs to be added in Equation (2) and the final result is

$$L = 0.2 \ln \left(\frac{2h\pi}{w + t} + 1 \right) \text{nH/mm} \tag{4}$$

Results from the analytical calculations are validated by comparing them with simulations using Maxwell. Fig. 7 shows the self-inductance calculated from Equation (4) and the Maxwell results. An excellent agreement has been achieved with this formula.

Fig. 8 plots the mutual inductance calculated from Equation (3) and the Maxwell simulation results. The mutual inductance decreases quickly as wire separation increases – much faster than the mutual inductance of two wires without a ground plane. This is due to the fact that the mutual inductance of two wires over a ground plane is inversely proportional to the square of the wire separation D in Equation (3).

VI. Capacitance Modeling of IC Structures

To model on chip interconnects as transmission lines, capacitance also needs to be accurately modeled [28]. Capacitance extraction capabilities based on more realistic and geometrically complicated structures is especially important for MEMS, RF integrated circuits as well as on-chip ICs. Non-planar IC structures need to be modeled correctly in order to extract the accurate capacitance of these complex geometries. Layout (GDSII files) and process (e.g., layer thickness or simulated bird's beak shape) information are incorporated using a custom C program. The control flow follows the actual processing sequence such as deposition and etching layer-by-layer. The resulting geometric model has been represented in Virtual Reality Modeling Language (VRML) browsers. The device can be studied layer by layer or as a full image using a simple browser. The level-set method [29] is adapted to generate a surface mesh of these 3-D structures. With this methodology, the geometries of on-chip interconnects can be modeled more realistically, and the capacitance can be extracted more accurately. To demonstrate this approach to model complex geometries, a complete surface mesh of a four transistor SRAM includes a substrate (grey), the polysilicon layer (purple), and the two metal layers (blue and sky blue) is shown in Fig. 9, where the polysilicon layer includes a wordline, a ground line and gate regions. The non-planar nature of the structures are fully captured with the solid modeling approach. To analyze realistic structures, FASTCAP [30] is used, owing to its ability to handle complicated surface topologies. For a cell size of $5 \times 7.25\mu\text{m}^2$ (feature size is 0.6 μm), capacitance between one bitline and the substrate is 1.75 fF

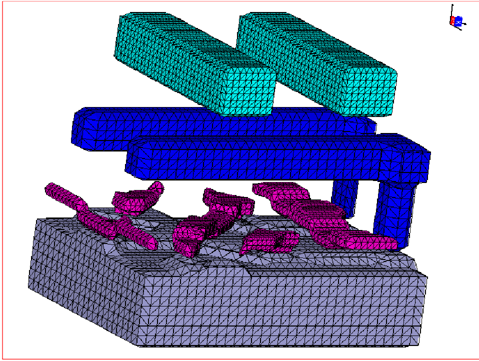


Fig. 9. Silicon substrate, polysilicon layer, the first and second metal layers in surface mesh.

while capacitance between the other bitline and the substrate is 1.77 fF. The capacitance between two bitlines is 1.07 fF. One can simulate the wordline, bitlines and the substrate as a whole structure.

VII. Summary and Conclusions

On-chip interconnect modeling is presented, which includes inductance and capacitance modeling. Results from both measurements and simulations show the growing impact of on-chip inductance for sub-0.25 μm VLSI. Inductance becomes a critical factor for intermediate (mm-scale) length wires. A physical inductance modeling is presented, which includes effects of 3-D geometry, as well as the overall complexity of multi-conductor environments, including consideration of substrate effects. Analytical formulae are used to estimate on-chip inductance for design guidelines. The modeling methodology and results are verified by experimental test chips. Modeling and measurement of test structures have shown good agreement up to 10 GHz. It is demonstrated that coplanar waveguides can confine the magnetic fields, offer nearby return paths and reduce overall wire inductance for critical signals. Power/ground grids can also offer nearby current return paths for signal wires. Dedicated ground planes can reduce wire self-inductance as well as wire mutual inductance. Analysis shows that, due to eddy current effects, densely populated grids resulting from designs including power/ground grids can reduce wire inductance significantly. On-chip capacitance modeling focuses on the link between the layout design data and electrical parameters based on very accurate and realistic complex 3-D geometries. Generated non-planar 3-D geometries can be viewed and studied layer by layer as illustrated with the SRAM example.

Acknowledgements

The authors would like to thank MARCO Interconnect Research Focus Center for funding support and Richard T. Chang and Niranjan Talwalkar of Stanford University for helpful discussions.

References

[1] B. Kleveland, X. Qi, L. Madden, R. Dutton and S. Wong, “Line inductance extraction and modeling in a real chip with power grid,” *Technical Digest of IEEE International Electron Devices Meeting*, pp. 901-904, Dec., 1999.

[2] A. E. Ruehli,“Inductance calculations in a complex integrated circuit environment,” *IBM J. Research Development*, pp. 470-481, Sept., 1972.

[3] A. E. Ruehli,“Equivalent circuit models for three-dimensional multi-conductor systems, ” *IEEE Trans. Microwave Theory and Tech.*, Vol. 22, No. 3, Sept., 1972.

[4] M. Kamon, M. J. Tsuk and J. K. White, “FASTHENRY: a multipole-accelerated 3-D inductance extraction program,” *IEEE Trans. Microwave Theory and Techniques*, pp. 1750, 1994.

[5] A. Deutsch, H. Harrer, C. W. Surovic, G. Hellner, D. C. Edelstein, R. D. Goldbaltt, G. A. Biery, N. A. Greco, D. M. Foster, E. Crabbe, L. T. Su and P. W. Coteus, “Functional high-speed characterization and modeling of a six-layer copper wiring structure and performance comparison with aluminum on-chip interconnections,” *IEEE Technical Digest of International Electron Devices Meeting*, pp. 295-298, Dec., 1998.

[6] A. Deutsch, Howard H. Smith, Christopher W. Surovic, Gerard V. Kopcsay, David A. Webber, Paual W. Coteus, George A. Katopis, W. Dale Becker, Allan H. Dansky, George A. Sai-Halasz and Phillip J. Restle, “Frequency-dependent crosstalk simulation for on-chip interconnects,” *IEEE Transaction on Advanced Packaging*, pp. 292-308, Vol. 22, No. 3, Aug., 1999.

[7] P. J. Restle, K. A. Jenkins, A. Deutsch and P. W. Cook “Measurement and modeling of on-chip transmission line effects in a 400 MHz microprocessor,” *IEEE Journal of Solid-State Circuits* Vol. 33, No. 4, April, 1998.

[8] S. Rusu and S. Tam, “Clock generation and distribution for the first IA-64 microprocessor,” *Digest of 2000 IEEE International Conference on Solid-State Circuits Conference* pp. 176-177, Feb., 2000.

[9] T. Xanthopoulos, D. Balley, A. Gangwar, M. Gowan, A. Jain and B. Prewitt, “The design and analysis of the clock distribution network for a 1.2 GHz Alpha microprocessor,” *2001 Digest of International Solid-State Circuit Conference*, pp.402-403, Feb., 2001.

[10] Shannon V. Morton, “On-chip inductance issues in Multiconductor systems,” *Proceedings of Design Automation Conference*, June, 1999.

[11] L. He, N. Chang, S. Lin and O. S. Nakagawa, “An efficient inductance modeling for on-chip interconnects,” *Proceedings of IEEE 1999 Custom Integrated Circuits Conference*, pp. 457-460, 1999.

[12] B. Krauter and S. Mehrotra, “Layout based frequency dependent inductance and resistance extraction for on-chip interconnect timing analysis,” *Proceedings of Design Automation Conference*, pp. 303-308, 1998.

[13] B. Krauter, S. Mehrotra and V. Chandramouli, “Including inductive effects in interconnect timing analysis,” *Proceedings of Design Automation Conference*, pp. 445-452, June, 1999.

[14] P. J. Restle, Albert Ruehli and Steven G. Walker, "Dealing with inductance in high-speed chip design," *1999 Proceedings of Design Automation Conference*, June, 1999.

[15] Kenneth L. Shepard and Zhong Tian, "Return-limited inductance: a practical approach to on-chip inductance extraction," *IEEE Transactions on CAD of Integrated Circuits and Systems*, pp. 425-346, Vol. 19, No. 4, April 2000.

[16] Xuejue Huang, Yu Cao, Dennis Sylvester, Shen Lin, Tsu-Jae King and Chenming Hu, "RLC signal integrity analysis of high-speed global interconnects," *2000 Digest of International Electrons Devices Meeting*, pp. 731-734, Dec., 2000.

[17] Yu Cao, Xuejue Huang, Dennis Sylvester, Norman Chang and Chenming Hu, "A new analytical delay and noise model for on-chip RLC interconnects," *2000 Digest of International Electrons Devices Meeting*, pp.823-826, Dec., 2000.

[18] Yehea I. Ismail and Eby G. Friedman, "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits," *1999 Proceedings of Design Automation Conference*, June, 1999.

[19] Yehea I. Ismail, Eby G. Friedman and Jose L. Neves, "Equivalent Elmore delay for RLC trees," *1999 Proceedings of Design Automation Conference*, June, 1999.

[20] Yehea I. Ismail, Eby G. Friedman and Jose L. Neves, "Repeater insertion in tree structured inductive interconnect," *Digest of IEEE/ACM International Conference on CAD*, pp. 420-424, Nov., 1999.

[21] K. Banerjee and Amit Mehrotra, "Analysis of on-chip inductance effects using a novel performance optimization methodology for distributed *RLC* interconnects," *2001 Proceedings of Design Automation Conference*, June, 2001.

[22] U. S. Inan and A. S. Inan, *Engineering Electromagnetics*, Addison-Wesley, Menlo Park, CA, pp.606-607, 1999.

[23] J. A. Tegopoulos and E. E. Kriezis, *Eddy Currents in Linear Conducting Media*, Lesevier Science Publishing Company Inc., New York, NY, 1985.

[24] S. Lin, N. Chang and Sam Nakagawa, "Quick on-chip self- and mutual-inductance screen," *Proceedings of IEEE 2000 International Symposium on Quality Electronic Design*, pp.513-520, 2000.

[25] Xiaoning Qi, Bendik Kleveland, Zhiping Yu, S. Simon Wong, Robert W. Dutton and Tak Young, "On-Chip Inductance Modeling of VLSI Interconnects," *2000 IEEE Solid-State Circuits Conference: Digest of Technical Papers*, pp.172-173, Feb., 2000.

[26] Richard E. Matick, *Transmission Lines for Digital and Communication Networks*, IEEE Press, Piscataway, NJ, 1969.

[27] *Maxwell 2D Parameter Extractor – User's Reference*, Ansoft Corporation, Pittsburgh, PA, Feb., 1993.

[28] Xiaoning Qi, S. Shen, Z. Hsiau, Z. Yu and R. Dutton, "Layout-based 3-D solid modeling of IC structures and interconnects including electrical parameter extraction," *IEEE International Conference on Simulation of Semiconductor Processes and Devices*, pp.61-64, Sept., 1998.

[29] Xe-Kai Hsiau et al., "Robust, stable, and accurate boundary movement for physical etching and deposition simulation," *IEEE Trans. on Electron Devices*, pp.44, Vol. 44, No. 9, Sept., 1997.

[30] K. Nabors and J. White, "FastCap: A multipole accelerated 3-D capacitance extraction program," *IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems*, pp.1447-1459, Vol. 10, No. 11, Nov., 1991.