High Frequency Characterization and Modeling of On-Chip Interconnects and RF IC Wire Bonds

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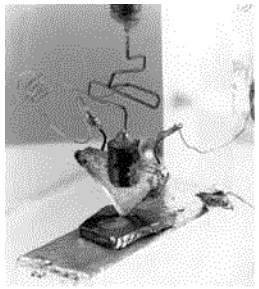
Outline

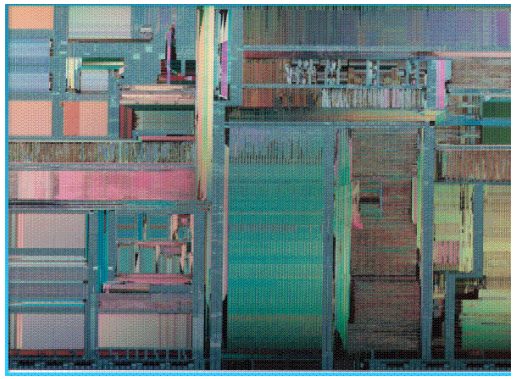
- Introduction
- On-Chip Inductance and Capacitance Modeling for VLSI Interconnects
- Off-Chip Interconnect Modeling for RF IC Packaging
- Summary

From Transistor to Microprocessor

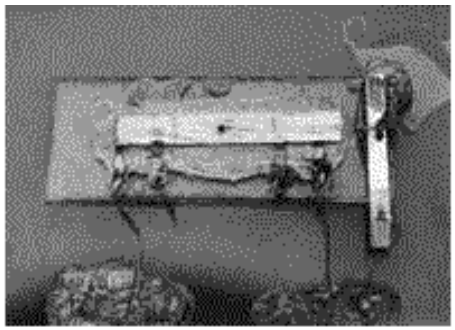


The First Transistor, 1947

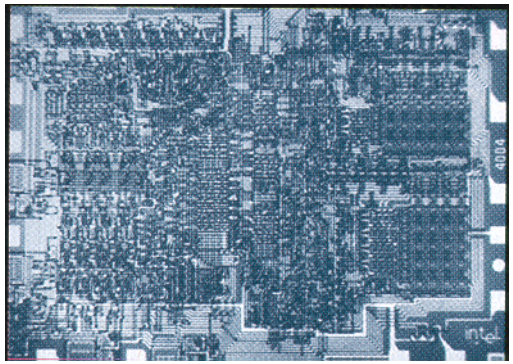
Wires are everywhere



The Pentium Processor

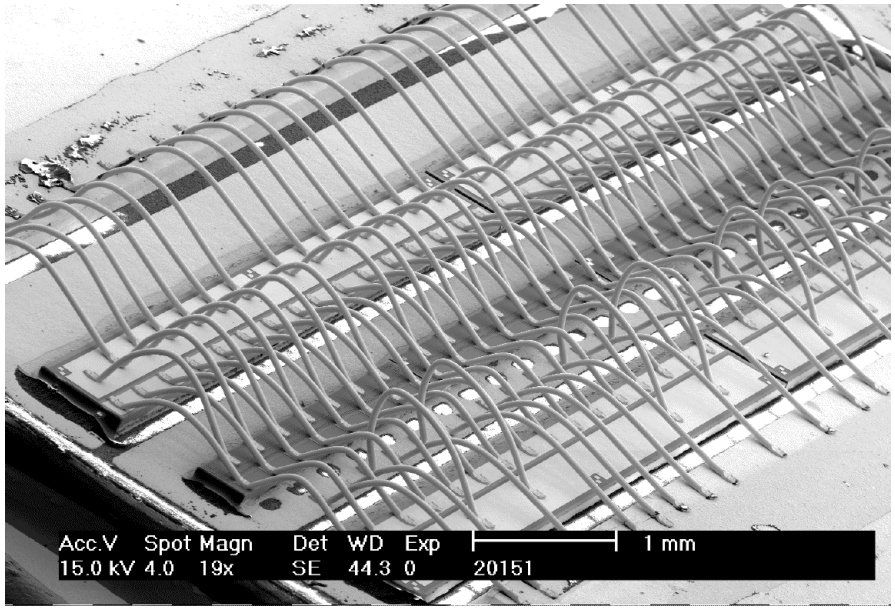


The First Integrated Circuit
1958



The First Microprocessor, the Intel 4004
1971

From On-Chip to Off-Chip



Bonding wires in the RF Power Transistors (BJT): Ericsson 20151

Interconnects - A Limiting Factor in VLSI DSM Era

"Interconnect scaling - the real limiter to high performance ULSI" - M. Bohr, IEDM'95

"The ratio of global wire delay to gate delay is going up rapidly"

"The ability to deal with inductance effects is an increasing requirement" - ITRS, 1999

"CAD tools need to deal with more wires" - M. Horowitz, ISSCC 2000

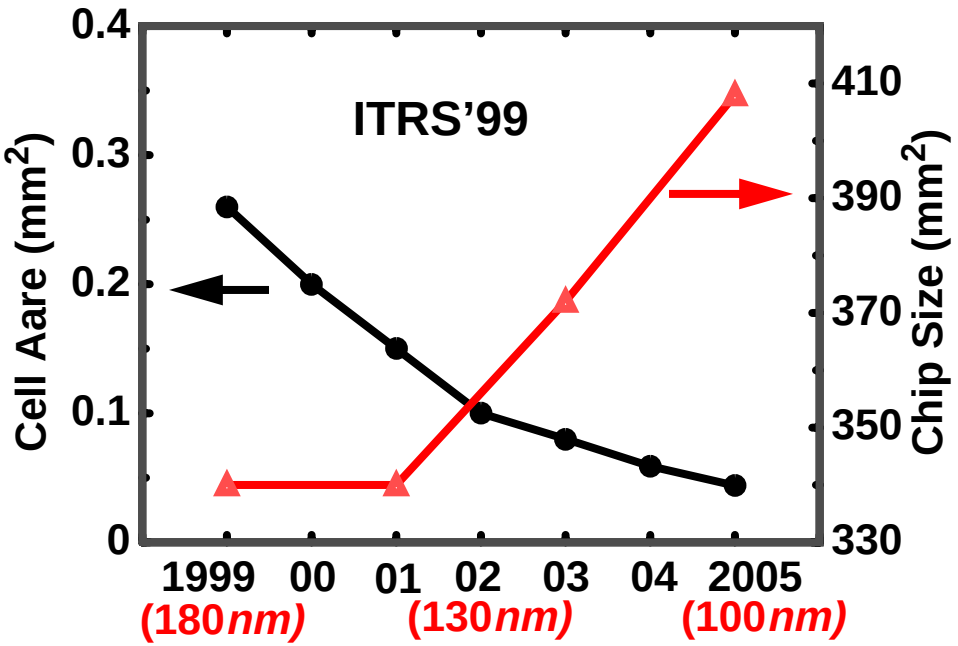
Simply, Lots of Wires

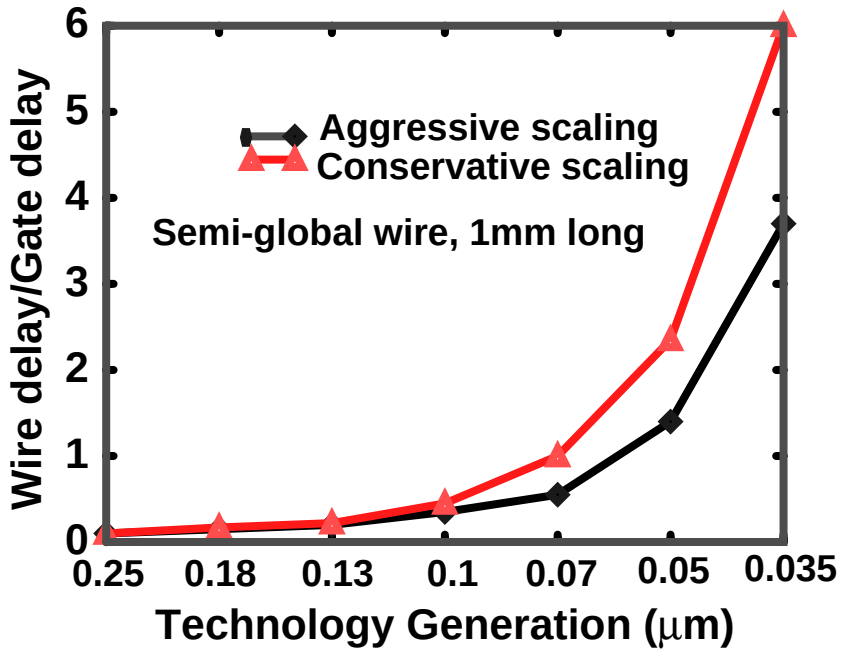
“I SEE WIRES.”

Outline

- Introduction
- **On-Chip Inductance and Capacitance Modeling for VLSI Interconnects**
  - **WHY inductance?**
  - **WHAT is inductance?**
  - **HOW to model inductance?**
  - **How to get accurate capacitance models?**
- Off-Chip Interconnect Modeling for RF IC Packaging
- Summary

Longer Wires, Faster Gates





"Fixed-length wires, relative to gates, worsen by 2x per generation. This is a big problem!"

(Horowitz, ISSCC'00)

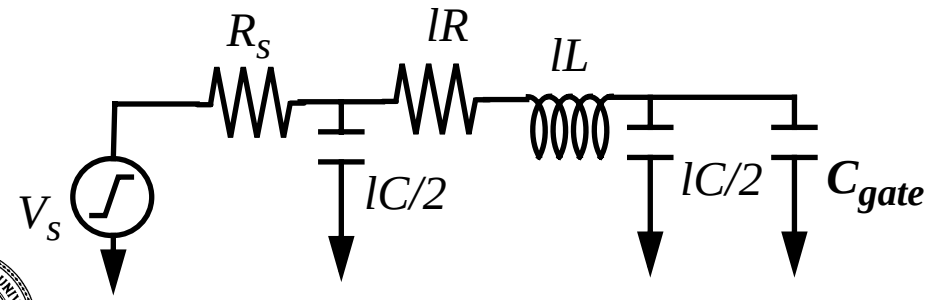
Transmission Line Model Needed

- **When $t_{rise} \leq t_{wiredelay}$: transmission line effects.**
- **Using wider wires on upper metal layers for critical signals nets like clocks, and copper technology, $j\omega L \sim R$.**
- **If $R \approx 0$, wire delay is $l\sqrt{LC}$ (*time of flight*).**
- **$P = IV$, low voltage, larger *I* swing, $\frac{di}{dt}$, ground bounce.**

Do We Need Inductance Modeling?

- **The Intel Itanium™ Processor:** ***"R-L-C model optimizes the placement... to minimize the overall delay of global clock."*** **- Rusu, ISSCC 2000**
- **The Digital Alpha 21264:** ***"To provide even control and predictability in signal-line and power-ground inductance,... designed two metal layers exclusively for the distribution of power and ground."*** **- Shepard IEEE Trans. on CAD, April. 2000**
- **Driver delay < *RC* wire delay < lossless TEM delay:**

  [IBM: Deutsch et al.]

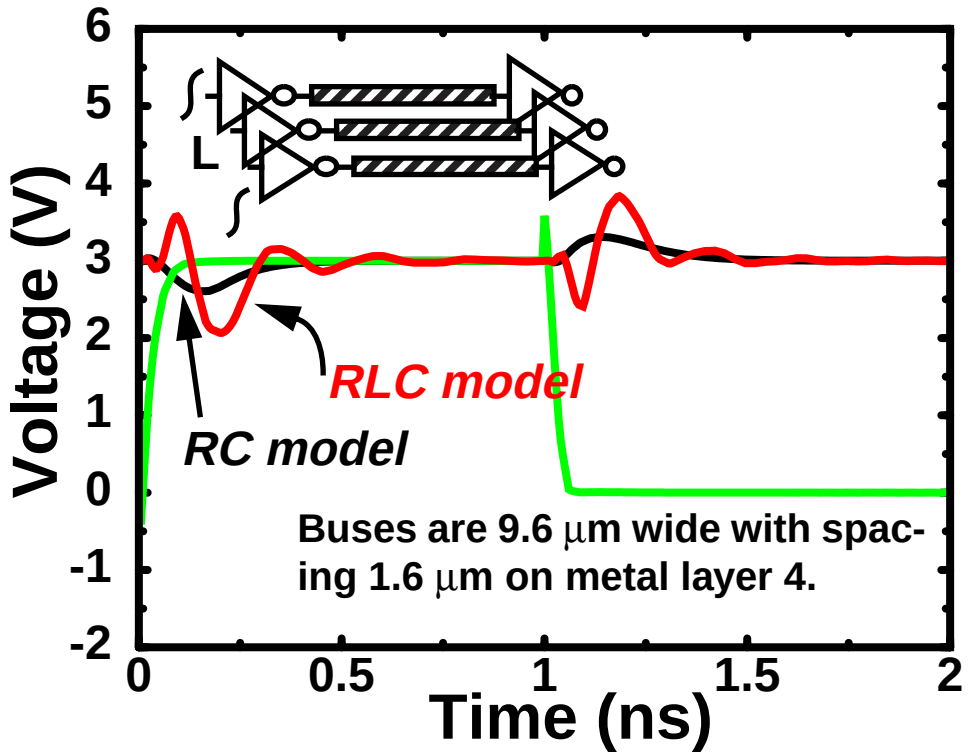


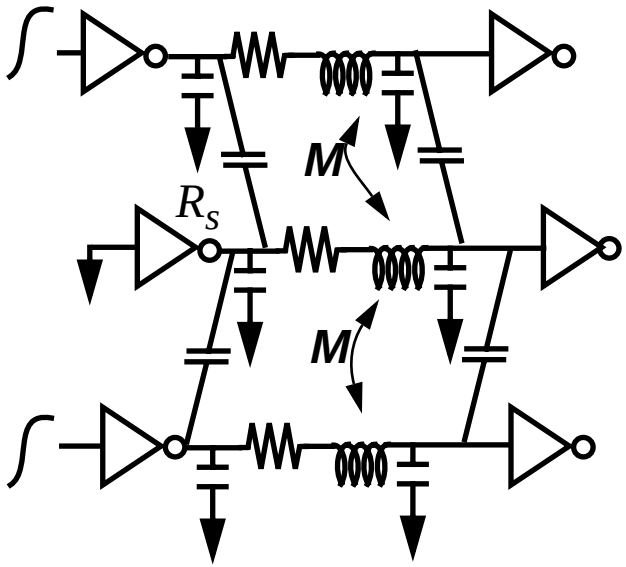
$$R_s C_{tot} < \frac{RCl^2}{2} < l\sqrt{LC}$$

l=wire length

$C_{tot}=C_{gate}+lC_{wire}$

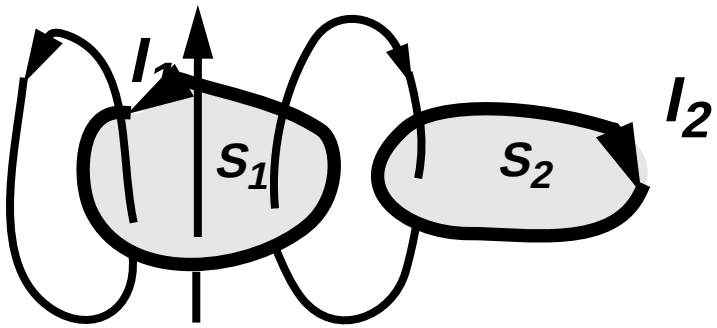
Inductive Cross Talk

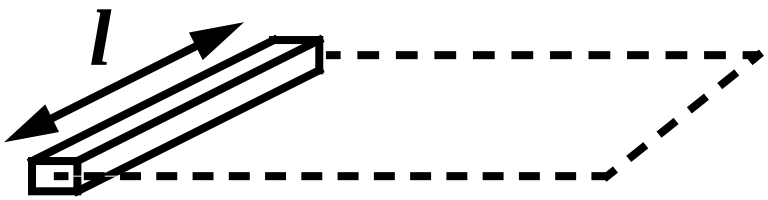




- **Mutual inductive coupling cannot be ignored.**

What Is Inductance?





$\mathbf{B_1}$

$$\Psi_{11} = \int_{s_1} \mathbf{B_1} \cdot d\mathbf{s_1} \qquad L_{11} = \frac{\Psi_{11}}{I_1}$$

$$\Psi_{12} = \int_{s_2} \mathbf{B_1} \cdot d\mathbf{s_2} \qquad M_{12} = \frac{\Psi_{12}}{I_1}$$

$$M_{12} = M_{21}$$

(Neumann'1890, Ruehli'72)

Good for IC Interconnection and constructing loop inductance

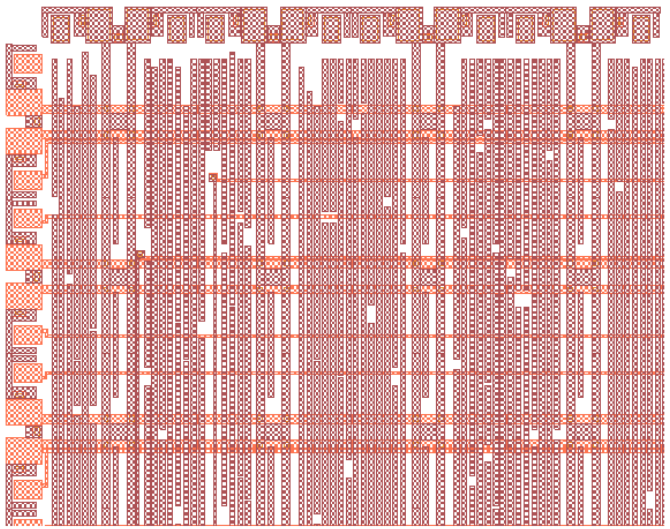
Previous Work

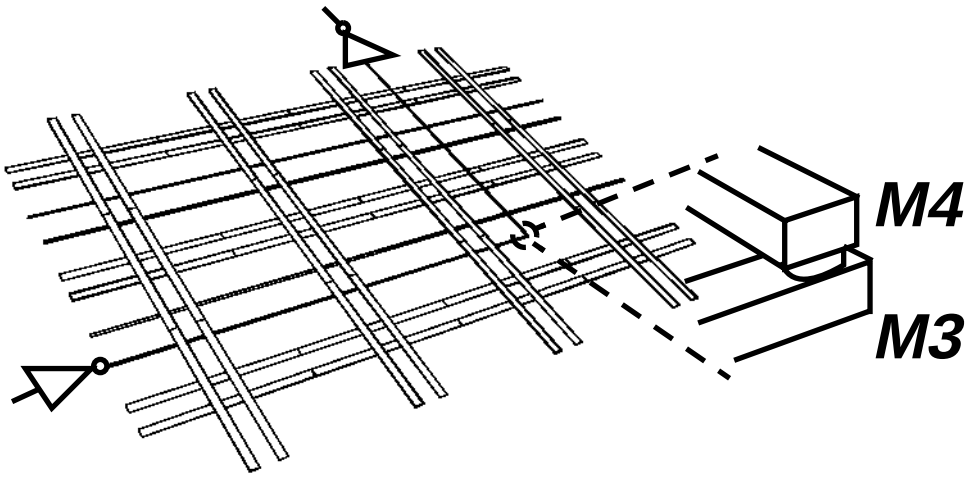
- **Partial inductance or Partial Element Equivalent Circuit (IBM: Ruehli'72).**
- **Field solvers, time domain measurement (IBM: Deutsch, Krauter'97) and frequency domain measurement (Stanford: Kleveland'99)**
- **Field solvers and lookup table. (HP: Lin, Chang'99)**

Approach of This Work

- **Automated 3D geometry modeling is based on layout and process information (Synopsys: Arcadia). EM field solvers are used to get "golden standard" results of inductance extraction for calibration.**
- **Analytical formulae of self/mutual inductance for quick estimation in CAD tools and establishing design guidelines.**
- **Verified with test structures.**

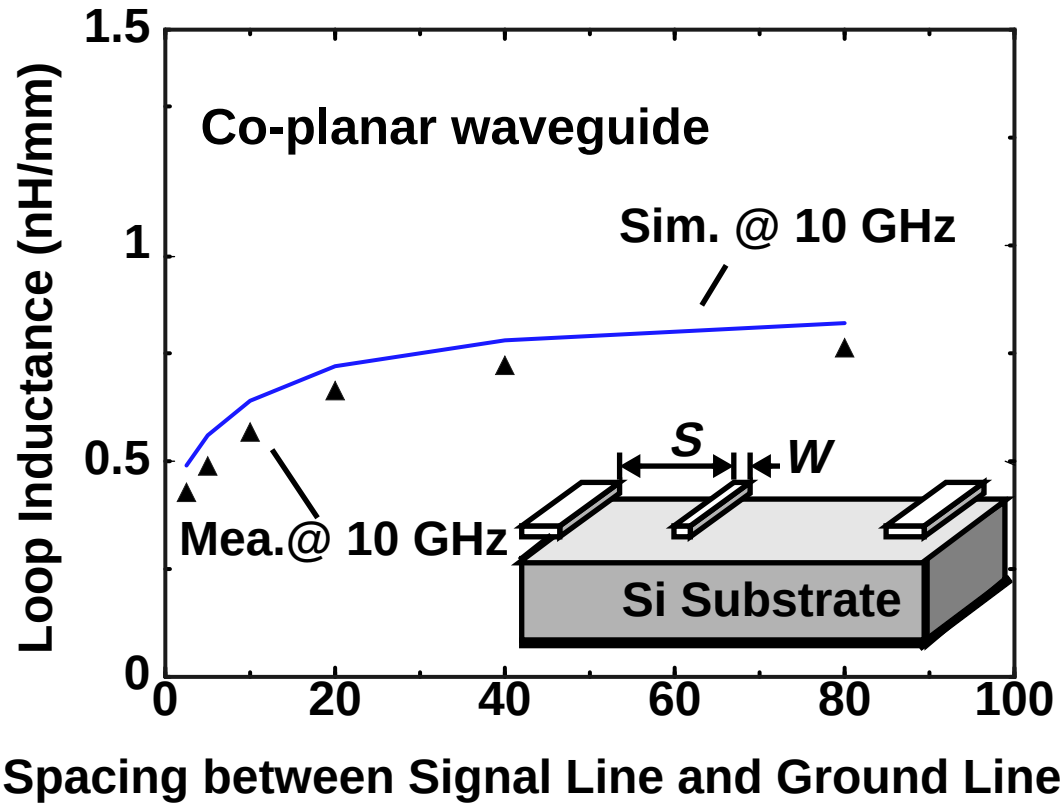
Extracted 3-D Geometry with Signal and Power/Ground Lines





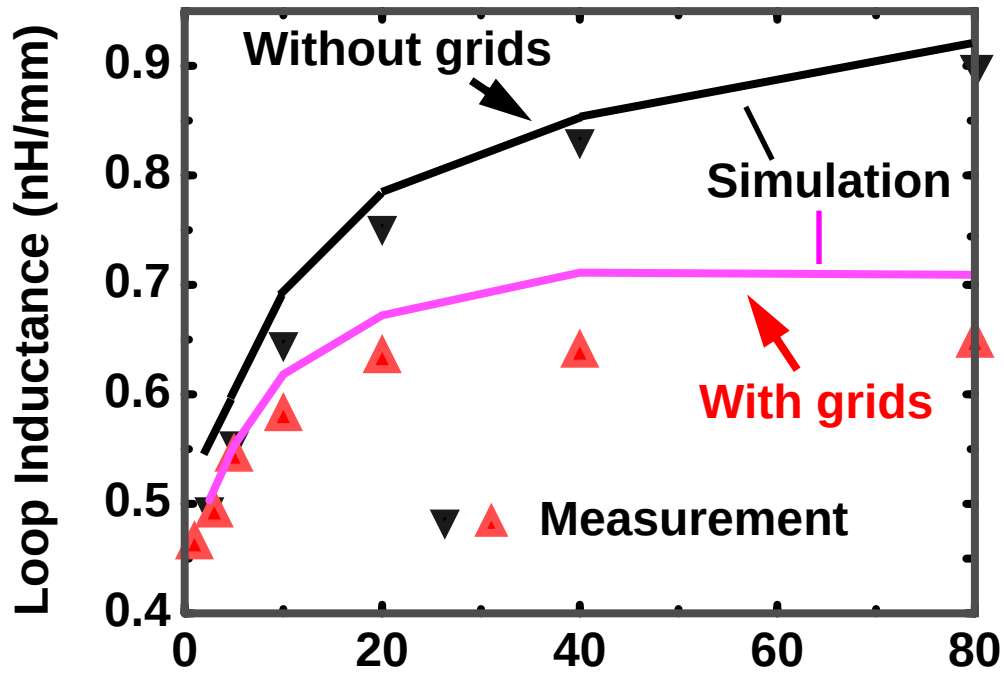
- **Automated geometry generation ready for 3D EM field solver inductance extraction**

On-Chip Loop Inductance Characterization



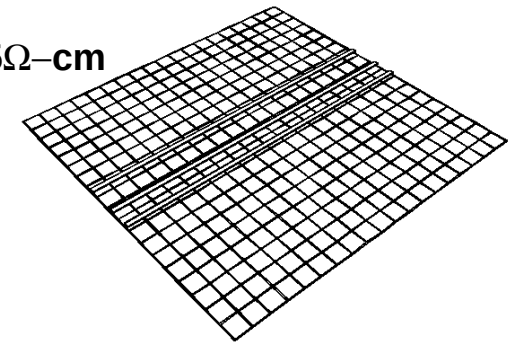
Spacing S is a critical factor for loop inductance

Loop Inductance with Ground Plane or Grids

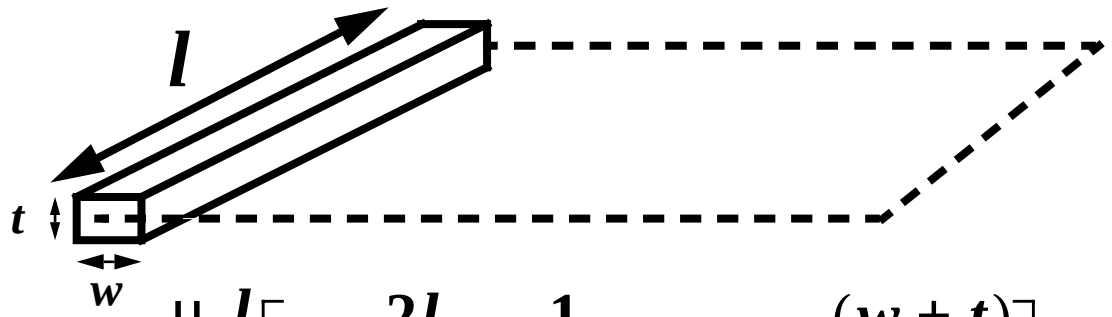


Inductance reduction due to eddy current effects - resulting from time varying magnetic fields.

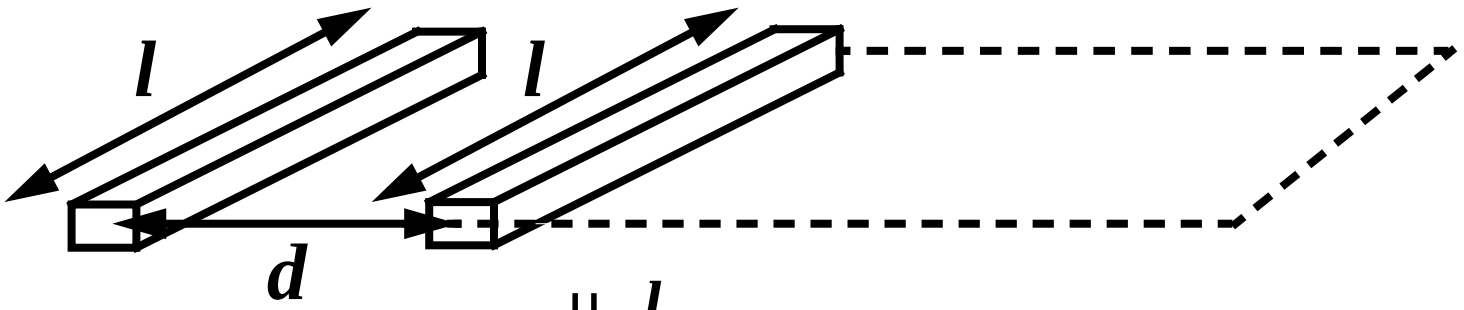
f = 3.0 GHz
w = 5μm
ρ = 0.015Ω–cm



Self/Mutual Inductance Formulae



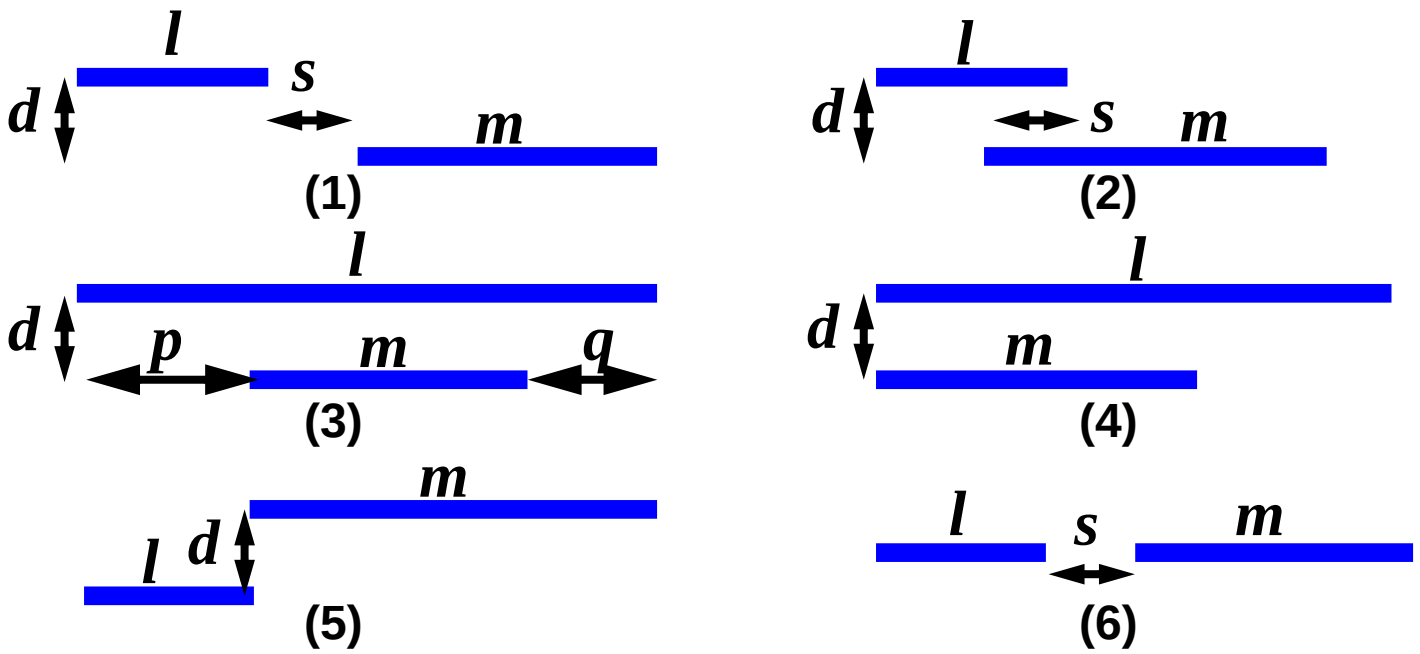
$$L_{self} = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{w+t} + \frac{1}{2} + 0.2235\frac{(w+t)}{l}\right]$$



$$M = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{d} - 1 + \frac{d}{l}\right]$$

(Rosa&Grover'16)

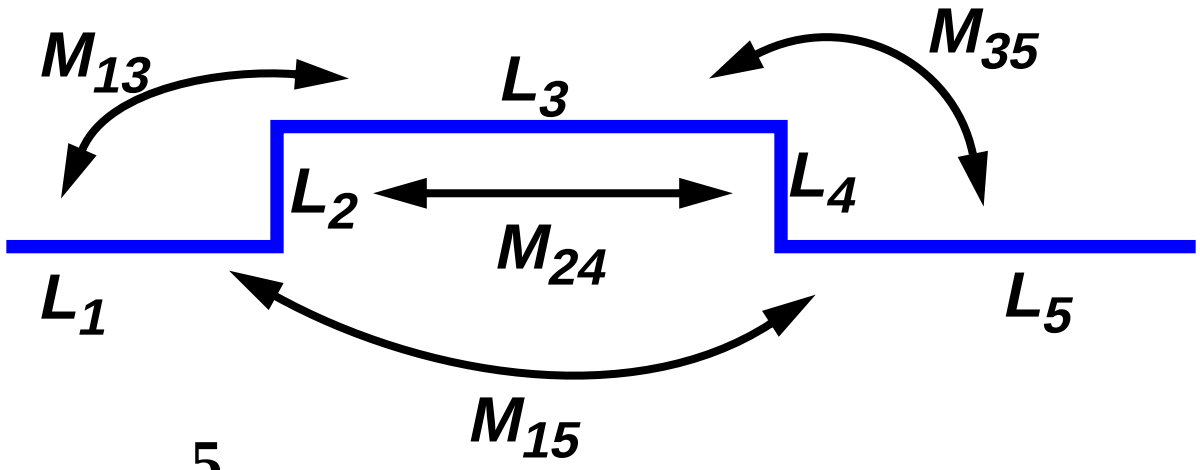
Analytical Formulae for Mutual Inductance



Case 4

$$M = \frac{\mu_0}{4\pi}\left[l \ln\left(\frac{l}{l-m}\right) + m \ln\left(4m\frac{(l-m)}{d^2}\right) - 2m + d \right]$$

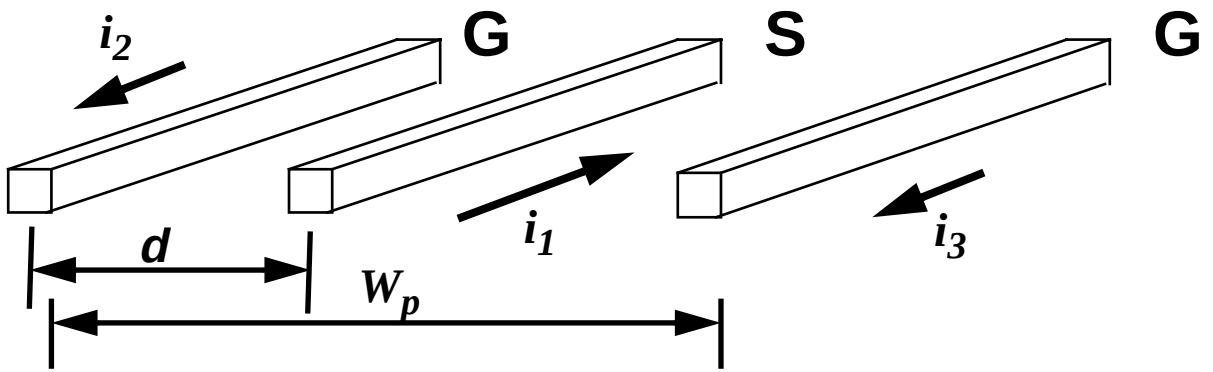
Estimation of Self Inductance of a Whole Wire



$$L_{total} = \sum_{i=1}^{5} L_i + 2M_{13} + 2M_{15} + 2M_{24} + 2M_{35}$$

- **Self inductances of all segments and their mutual inductances are needed.**

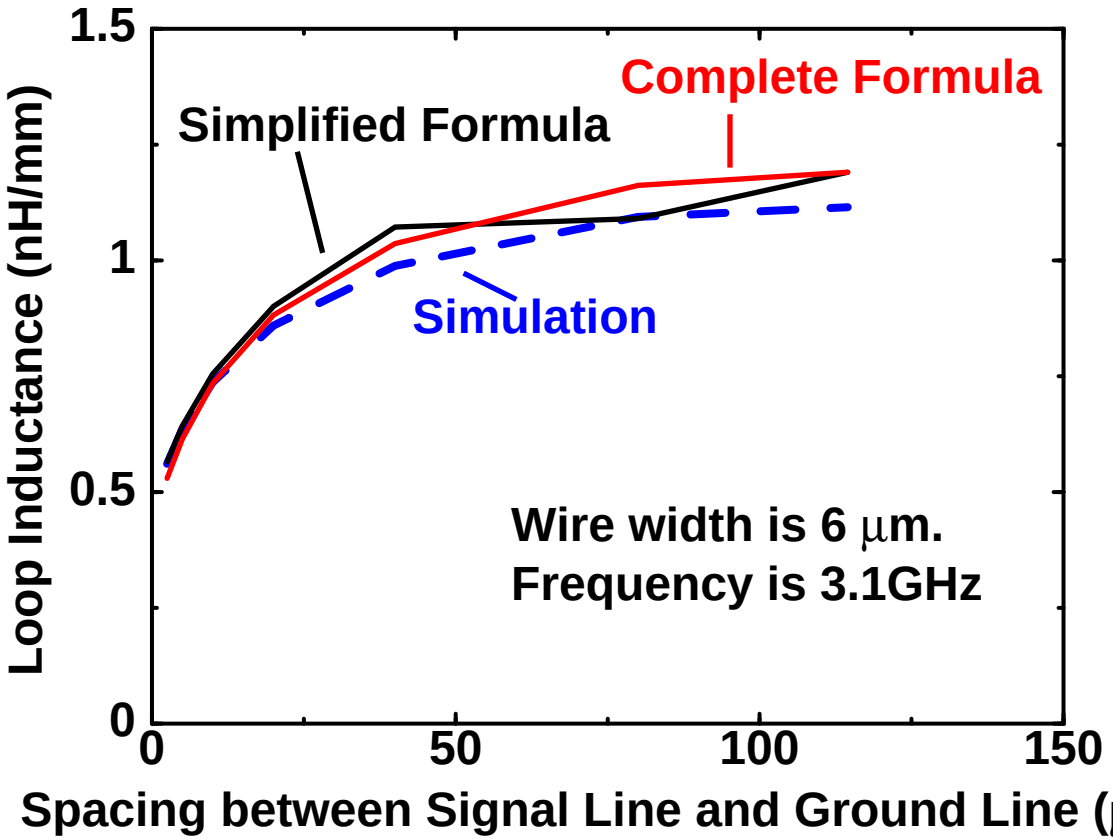
Analytical Formula for Coplanar Waveguide Structure



$$\hat{L}_{coplanar} = \frac{\mu_0}{2\pi}\left[\ln\frac{\pi d}{w_{sig}+t} + \frac{1}{2}\ln\frac{\pi d}{w_{gnd}+t} + \frac{1}{2}\ln\left(1-\frac{1}{\alpha}\right) + \frac{1}{2}\frac{\ln\dfrac{\pi w_p}{(\alpha-1)(w_{gnd}+t)}}{\ln\dfrac{\pi w_p}{w_{gnd}+t}}\ln(\alpha-1)\right]$$

$\hat{L}$: Inductance per unit length. w_{sig}, w_{gnd}: width of the signal/ ground wire. t: thickness of the metal layer, α: w_p/d

Formulae and Simulation for Coplanar Structure



Simplified Formulae (nH/mm):

$$\hat{L} = 0.3\ln\left(\frac{s+w}{w+t}\pi\right) - 0.1\ln 2 \qquad 2 \le \alpha < 4$$

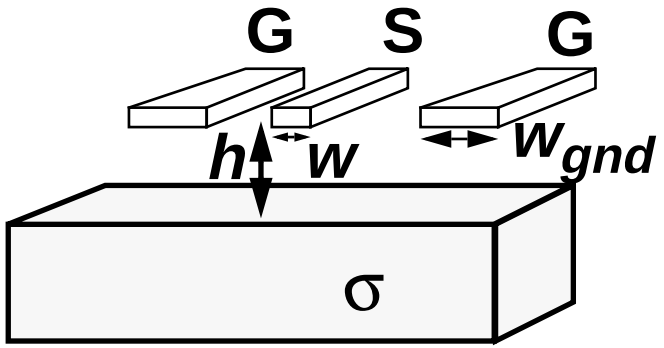
$$\hat{L} = 0.3\ln\left(\frac{s+w}{w+t}\pi\right) + 0.1 \qquad \alpha \ge 4$$

Formula with Substrate Correction

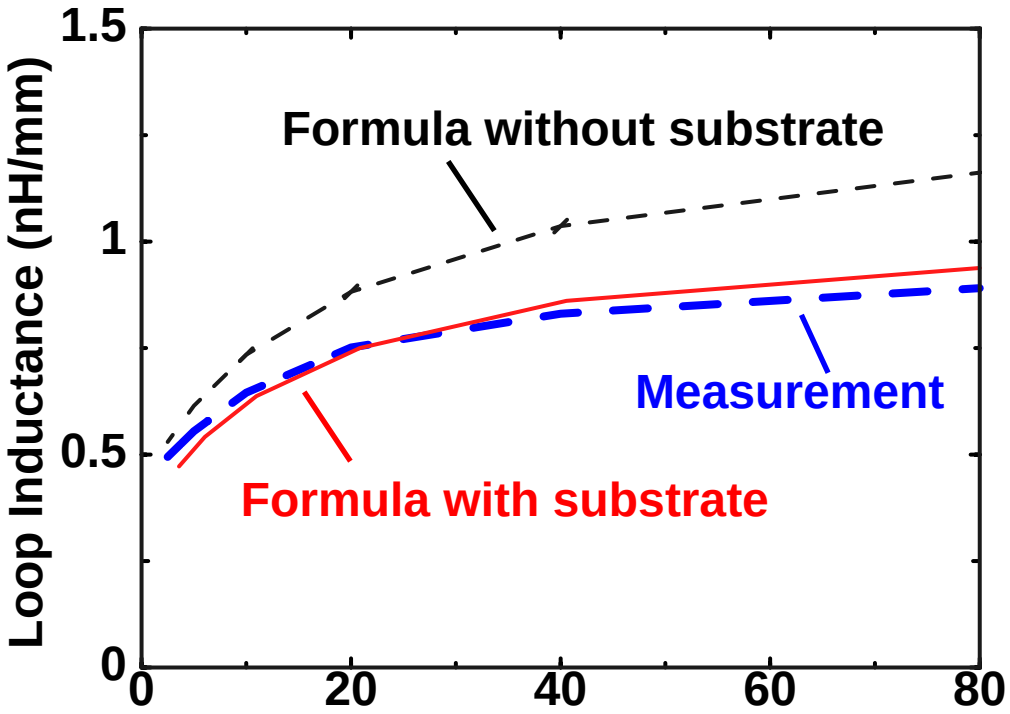
- **Magnetic field penetration into substrate and eddy currents - the current returns beneath the signal lines.**

$$\hat{L}_{total} = \hat{L}_{coplanar} - k\frac{\mu_0}{2\pi}\ln\left[\frac{\sqrt{\left[s+\frac{(w_{gnd}+w)}{2}\right]^2+h^2}}{h+\frac{1}{2\sqrt{\pi f\sigma\mu_0}}}\right]$$

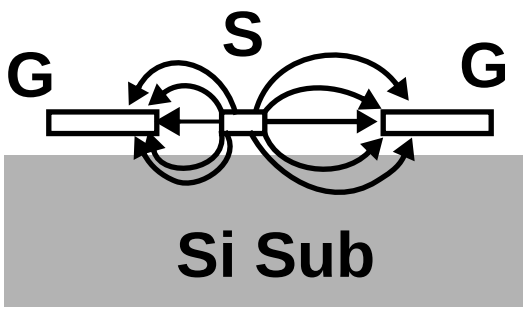
k: **the current distribution factor**



Loop Inductance with Substrate Effect



Inductance reduction due to the substrate



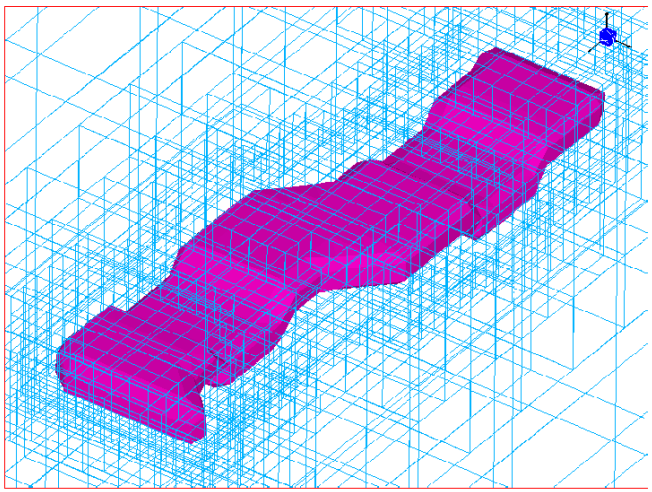
ρ_{sub}= 0.015Ω-cm

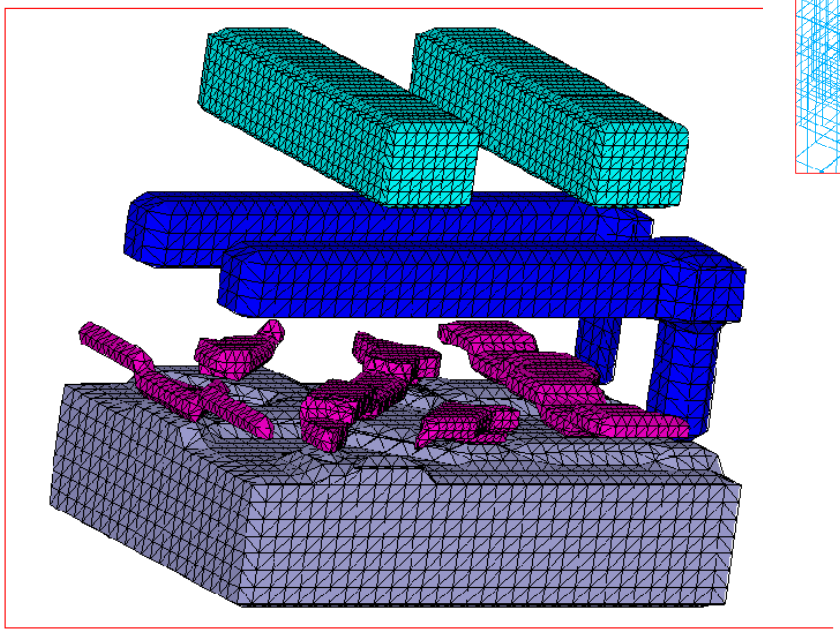
On-Chip Capacitance Modeling for IC Structures

- **Needed for accurate transmission line *RLC* parameters.**
- **Capacitance extraction based on complex non-planar 3-D geometries. Good especially for MEMS, RF IC.**
- **Link layout and process information with the electrical parameters.**

Non-Planar Structure Simulation

Word line





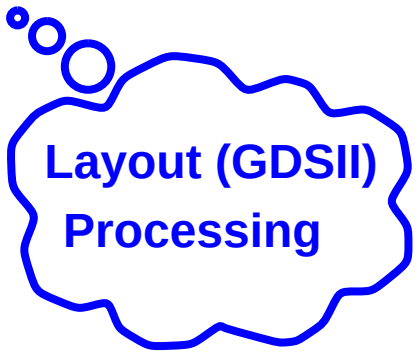
Mesh result for substrate, first poly layer and metal layers

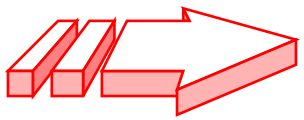
3-D Capacitance Extraction

	Sub	WL	BL1	BL2
Sub	2.92	1.27	0.36	0.36
WL	1.27	1.57	0.12	0.13
BL1	0.36	0.12	1.01	0.27
BL2	0.36	0.13	0.27	1.02

Units: fF

Design Data



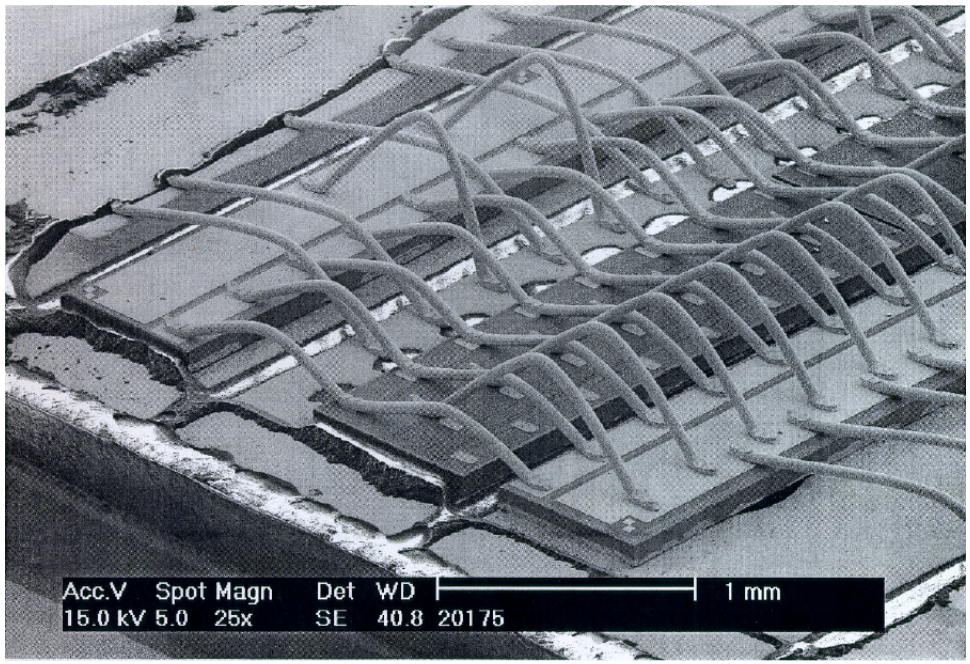


Electrical Parameters & Circuit Performance

Outline

- Background and Motivation
- On-Chip Inductance and Capacitance Modeling for VLSI Interconnects
- **From Die to Package: Off-Chip Interconnects (Wire Bonds) Modeling for RF IC Packaging**
  - ✧ Geometry modeling and equivalent circuit.
  - ✧ Simulation and measurement.
- Summary

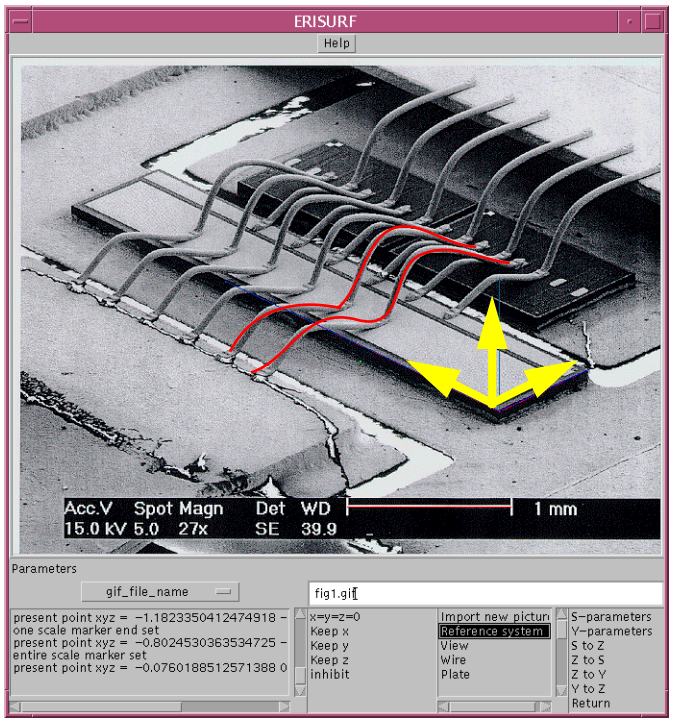
Bonding Wires at High Frequencies

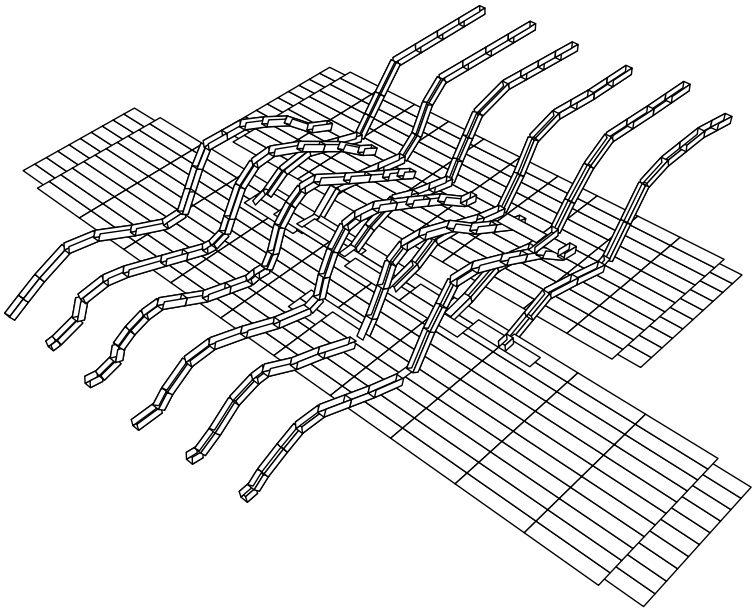


Inside of the package of a 55W bipolar transistor for 1.9 GHz PCS base stations

- **Packaging & circuit element**
- **Curvature is difficult to predict.**
- **Need 3D geometry modeling.**

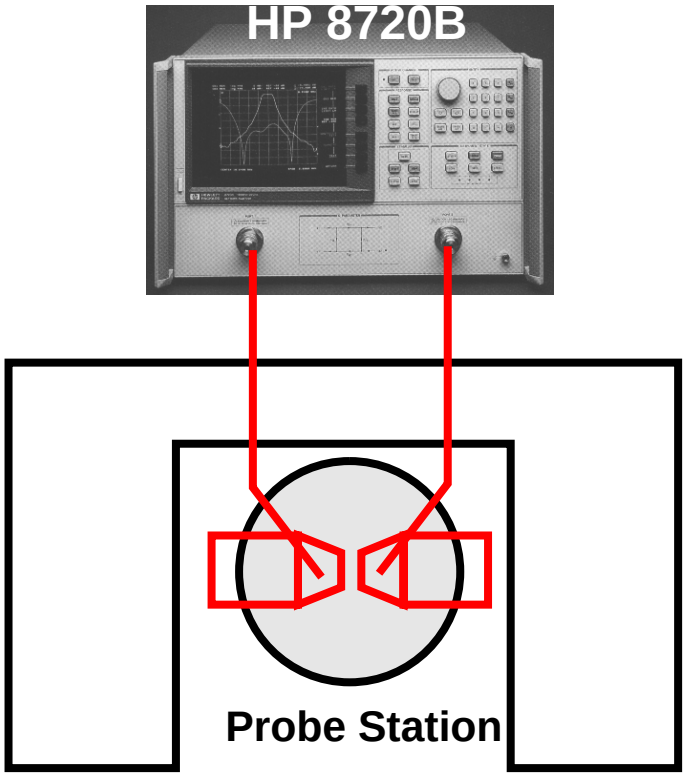
Interface and Extracted Geometry

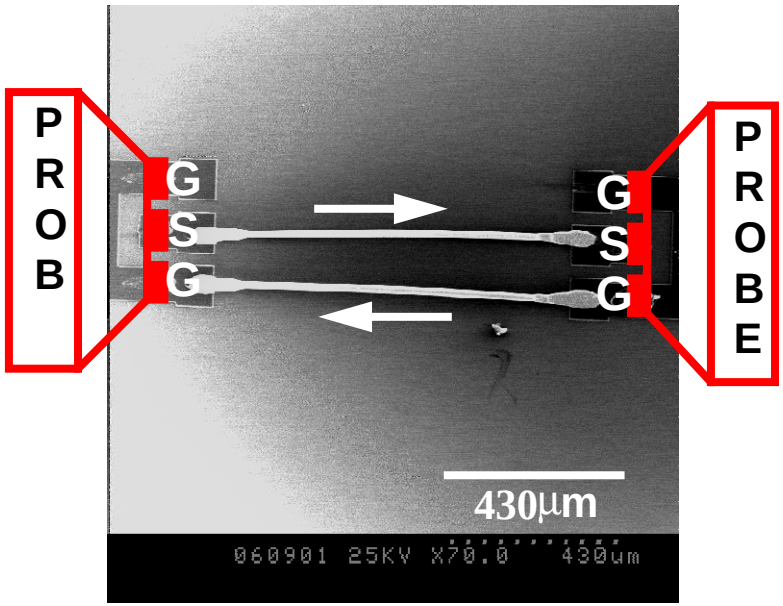




1. Define a reference coordinate system on an SEM photo;
2. Superimpose a drawing on the photo to emulate 3D movements;
3. Generate input files for simulators, e.g. FASTHENRY

Testing Setup

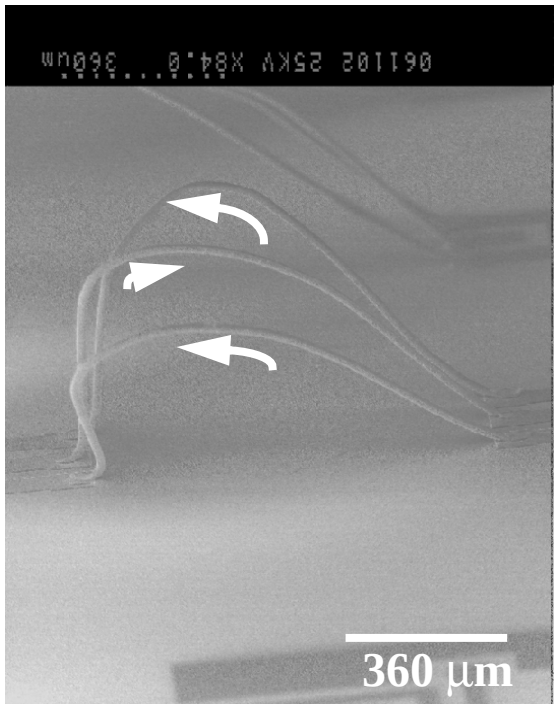




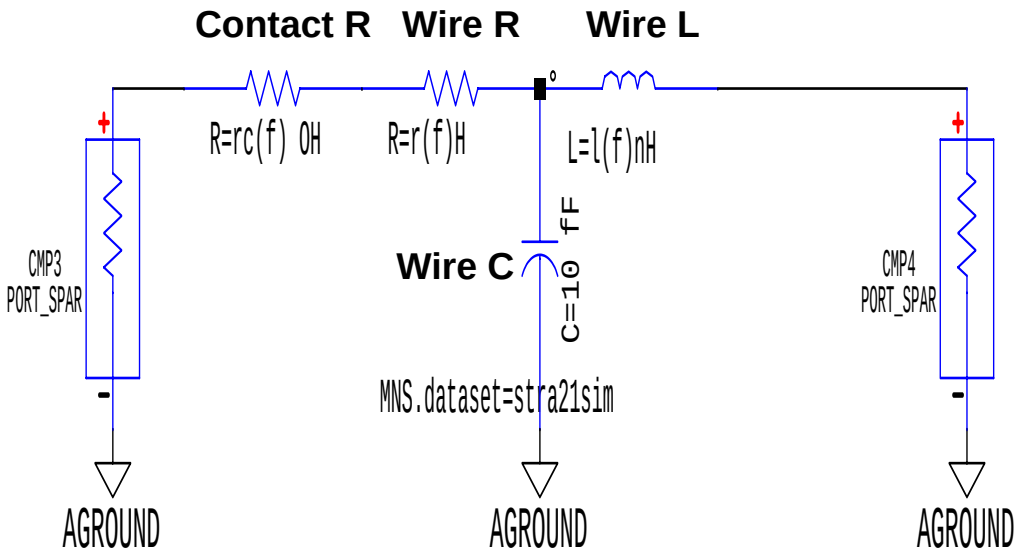
Device Under Test
(Stra21)

- Two port *S*-parameters were measured using Network Analyzer and co-planar G-S-G probe.

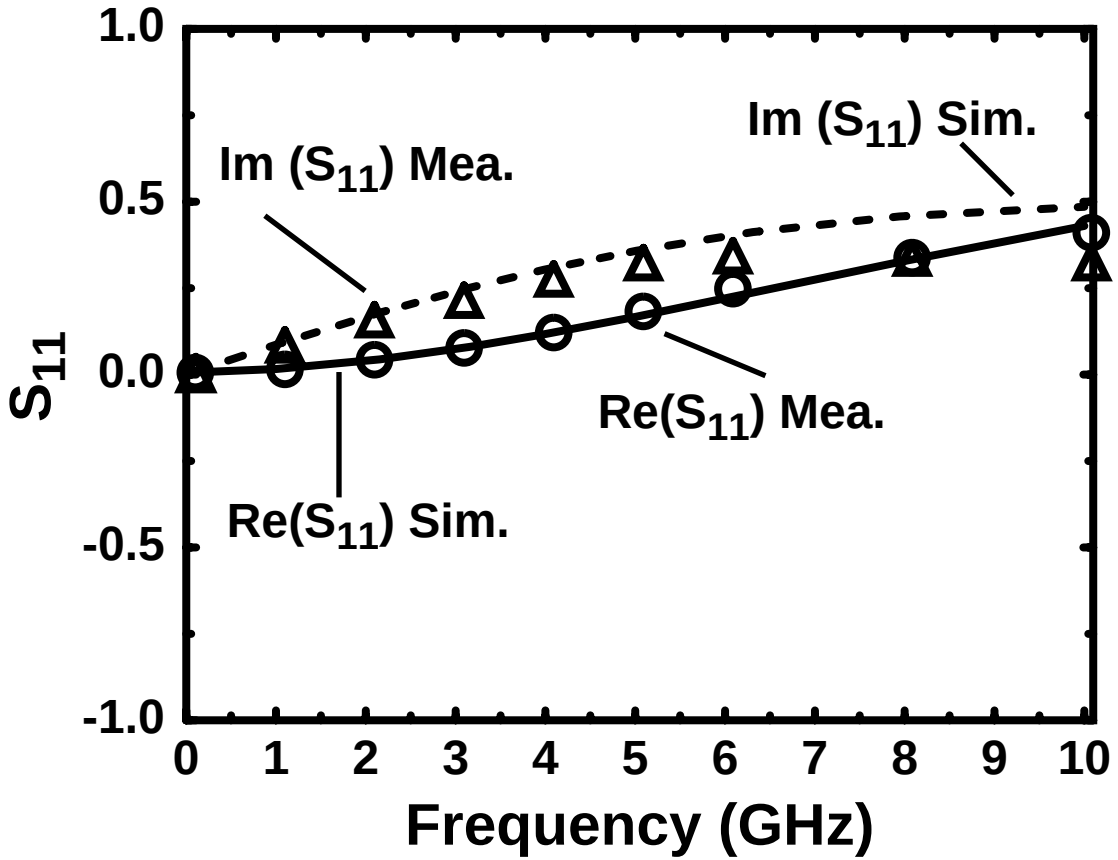
An Equivalent Circuit for Bonding Wires

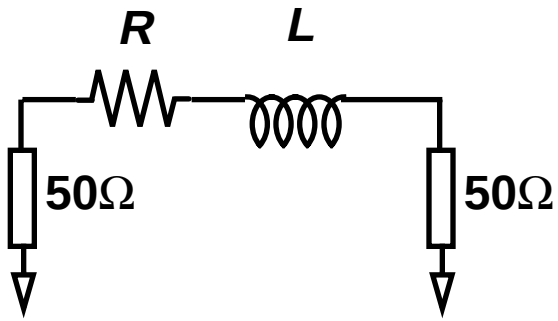


Test Structure Curv31



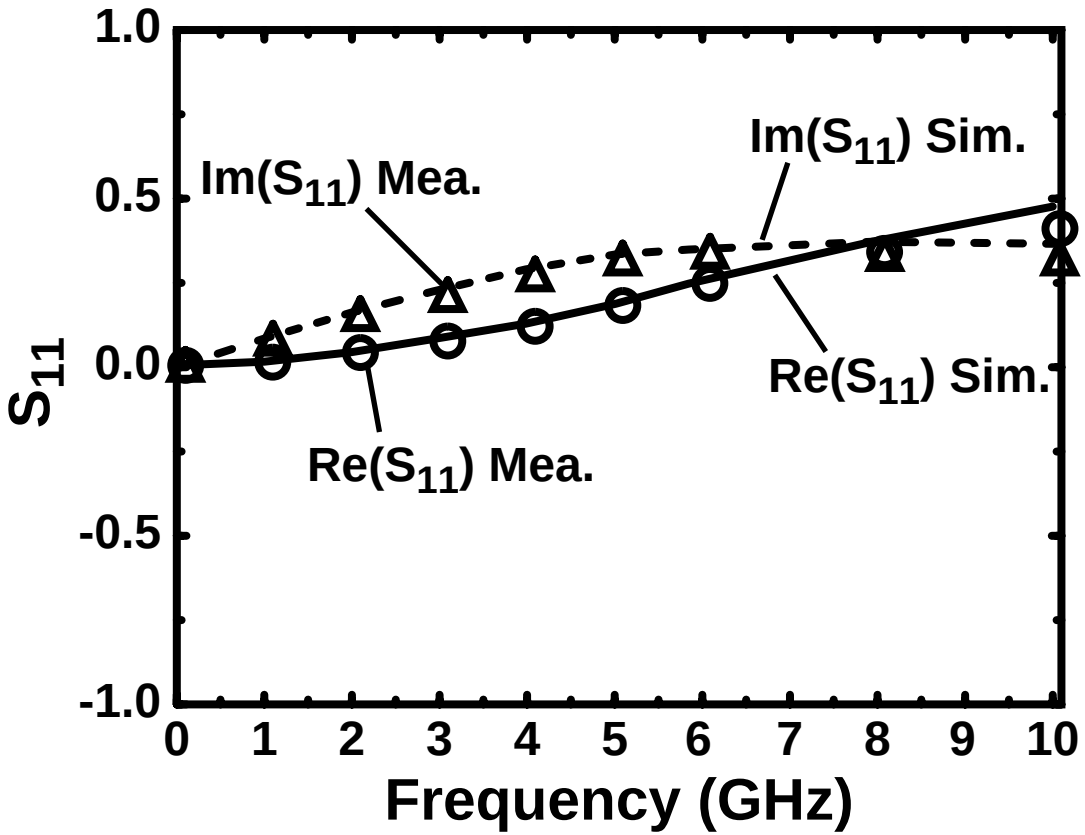
Measured and Simulated *S*-Parameters for Straight Wires

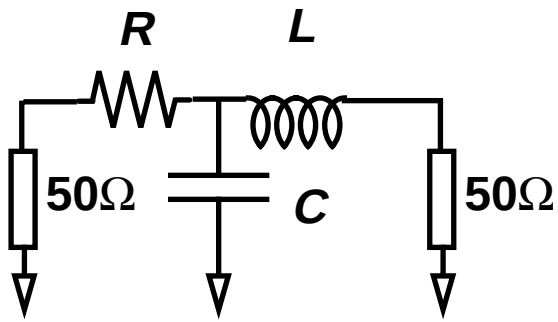




Stra21: two straight lines each of 1mm long *without* capacitance in model

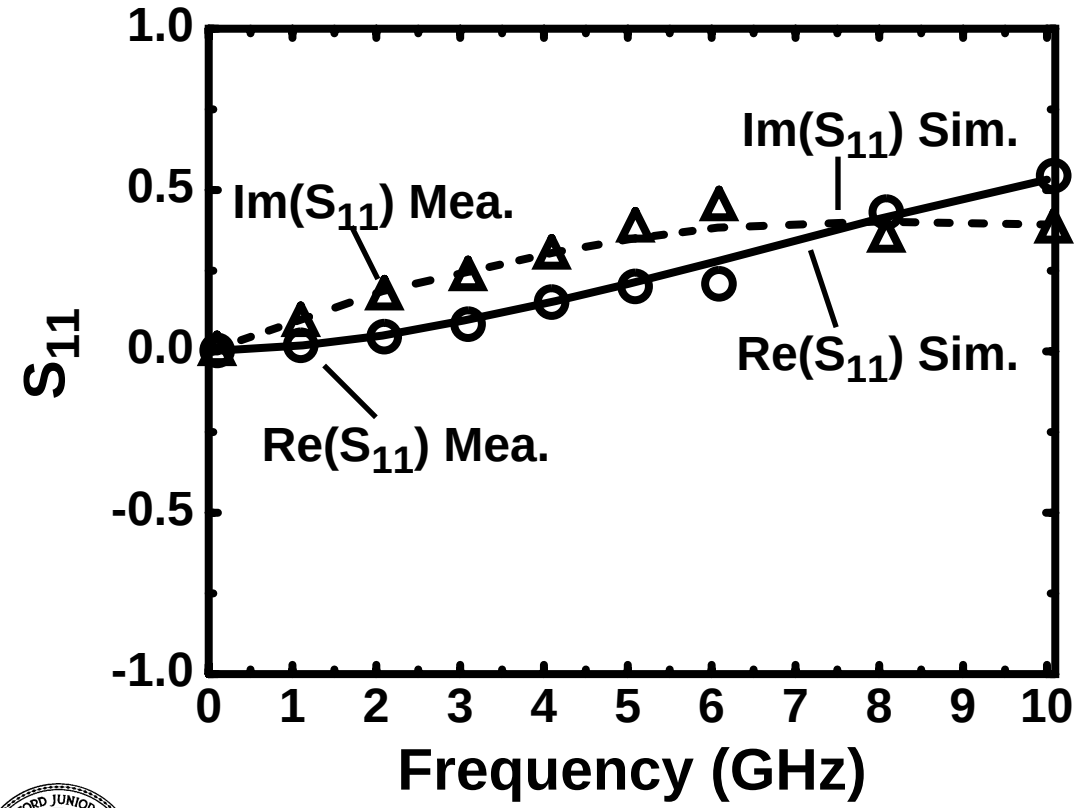
Measured and Simulated *S*-Parameters for Straight Wires



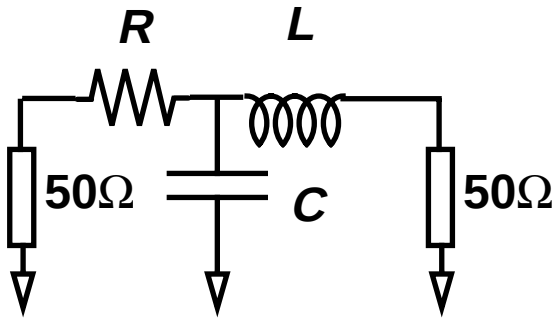


S_{11} of Stra21 *with* capacitance in model

Measured and Simulated *S*-Parameters for Curved Wires (Curv31)

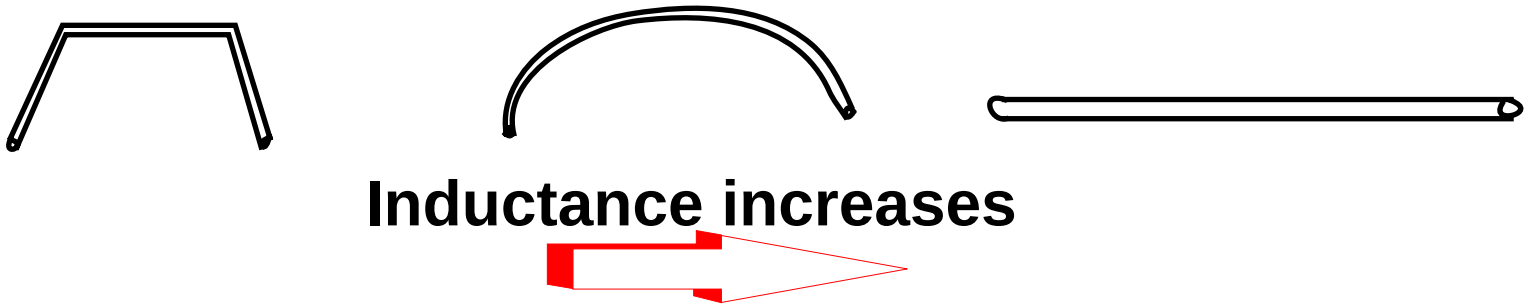


Curvatures are accurately captured.



S_{11} for Curv31 *with* capacitance included

General Shape Dependence of Self and Mutual Inductance



Inductance increases

1.52mm

Self inductance:

1GHz	**0.783nH**	**0.979nH**	**1.160nH**
	(48.15%)	**(18.49%)**	

Mutual inductance: (spacing: 0.3mm)

10GHz	**0.176nH**	**0.305nH**	**0.457nH**
	(159.66%)	**(49.84%)**	

Cancellation due to mutual inductance among segments

Summary

On-Chip VLSI Interconnects

- **The growing impact of inductance of on-chip interconnects in terms of delay and cross talk**
  - ✧ Need close ground returns, co-planar waveguide shielding, ground/power plane or grids (reduce inductance by half).
  - ✧ Good conductivity of the substrate reduces inductance (18% for large signal ground spacing). The three critical factors: spacing, height of signal lines and substrate conductivity.
  - ✧ Geometry generation from layout needs to be integrated into CAD tools for whole chip inductance extraction.

Summary

- **Derived formulae verified by experiments demonstrate accuracy for design and CAD tools.**

Off-Chip Interconnects - Bonding Wires

- **Geometry and shape dependence of inductance are important.**
- **Inductance dominates, but capacitance matters too in frequency above 6 GHz.**

Contributions

- **On-chip inductance modeling**
  - ✧ X. Qi, B. Klevland, Z. Yu, S. Wong, R. Dutton and T. Young, "On-chip Inductance Modeling of VLSI Interconnects", *IEEE International Solid-State Circuits Conference* (ISSCC'00), pp. 172, Feb, 2000.
  - ✧ X. Qi, G. Wang, Z. Yu, R. Dutton, T. Young and N. Chang, "On-chip Inductance Modeling and RLC Extraction of VLSI Interconnects for Circuit Simulations", *IEEE Custom Integrated Circuits Conference* (CICC'00), May, 2000.
- **Bonding wire modeling**
  - ✧ X. Qi, P. Yue, T. Arnborg, H. Soh, Z. Yu, R. Dutton and H. Sakai, "A Fast 3D Modeling Approach and Parasitic Extraction of Bonding Wires for RF Circuits" *IEEE International Electron Devices Meeting*, (IEDM'98), pp. 299, Dec.1998.
  - ✧ X. Qi, P. Yue, T. Arnborg, H. Soh, Z. Yu, R. Dutton and H. Sakai, "A Fast 3D Modeling Approach and Parasitic Extraction of Bonding Wires for RF Circuits" *IEEE Transactions on Advanced Packaging*. Aug. 2000.

Contributions (cont.)

- **On-chip capacitance modeling**
  - X. Qi, S. Shen, Z. Hsiau, Z. Yu, and R. Dutton, "Layout-Based 3D Solid Modeling of IC Structures and Interconnects Including Electrical Parameter Extraction", *IEEE International Conference on Simulation of Semiconductor Processes and Devices* (SISPAD'98) pp. 61-64, Sept., 1998.
- **Others:**
  - G. Wang, X. Qi, Z. Yu, R. Dutton and C. Rafferty, "Large Signal Analysis of On-Chip Interconnects Using Transport Based Approach", *The Fifth International Symposium on Antennas, Propagation, and EM Theory* (ISAPE 2000), Aug. 2000.
  - O. Tornblad, J. Jang, X. Qi, T. Arnborg, Q. Chen, Z. Yu and R. Dutton, "Compact Electrothermal Modeling of RF Power LDMOS", *Proceedings of the Workshop on Synthesis and System Integration of Mixed Technologies* (SASIMI 2000), pp.146, April, 2000.
  - B. Kleveland, X. Qi, L. Madden, R. Dutton and S. Wong, "Line Inductance Extraction and Modeling in a Real Chip with Power Grid", *Tech. Digest of IEEE International Electron Devices Meeting* (IEDM'99), pp. 901, Dec, 1999.