High-Frequency Characterization of On-Chip Digital Interconnects

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***Abstract*—On-chip inductance is becoming increasingly important as technology continues to scale. This paper describes a way to characterize inductive effects in interconnects. It uses realistic test structures that study the effect of mutual couplings to local interconnects, to random lines connected to on-chip drivers, and to typical power and ground grids. The use of S parameters to characterize the inductance allows a large number of lines to be extracted while requiring only a small overhead measurement of dummy open pads to remove measurement parasitics. It also enables direct extraction of the frequency-dependent R, L, G, C parameters. The results are summarized with curve-fitted formulas of inductance and resistance over a wide range of line spacings and line widths. The significance of the frequency dependence is illustrated with transient analysis of a typical repeater circuit in a 0.25-μm technology. A model that captures the frequency dependency of the extracted parameters accurately predicts the performance of a new inductance-sensitive ring oscillator.**

***Index Terms*—High-speed integrated circuits, inductance measurement, integrated circuit interconnections, integrated circuit modeling, scattering parameters measurement, skin effect.**

I. Introduction

THE CONTINUING trend toward higher levels of integration is partially driven by the fact that on-chip interconnects are faster, denser, and more reliable than off-chip ones. Over the past decades, this integration has enabled a tremendous improvement in the density and speed of electronic systems. As the signal switching speeds exceed 1 GHz and chip densities exceed tens of millions of transistors, the *RC* delays due to on-chip metal interconnects are becoming significant. The conventional aluminum–silicon dioxide interconnect scheme has been considered a serious limitation to further scaling [1]. This has prompted an industry-wide shift from aluminum to copper interconnects to reduce the resistance, and a relentless search for a reliable low-permittivity dielectric material to reduce the capacitance [2], [3]. However, for wide lines and buses, resistance minimization may not reduce the delays if they are dominated by inductance.

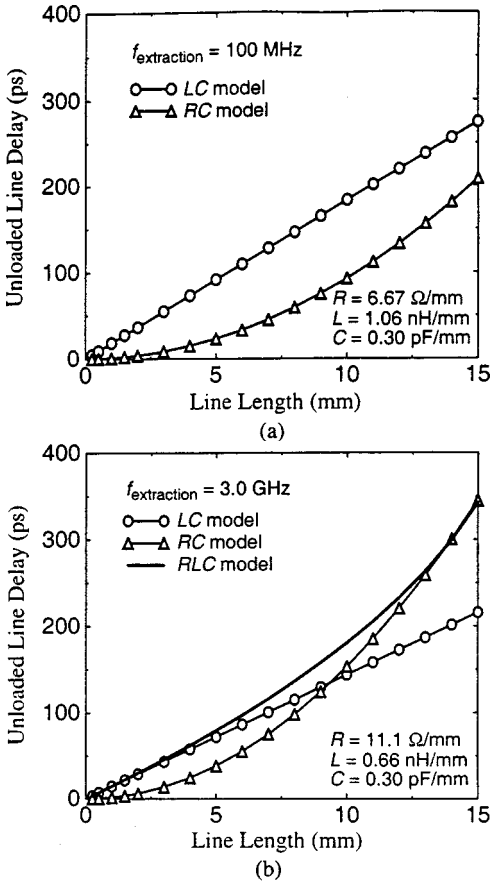

Fig. 1. Simulated unloaded line delay for 5.3-μm-wide line in top-level Al metal (35 mΩ/square). Delay measured from step input to 0.5 V_{dd} at end of line. Model parameters extracted at (a) 100 MHz and (b) 3 GHz from test structures to be described in this paper. Five *RC* and RLC segments are used in the simulations.

The delay of a line is a complicated question, because it depends on both the drive transistor and wire parameters. The importance of inductance is most easily shown if we initially ignore the effect of the driving transistors and assume that a wide wire is driven by a voltage source. Fig. 1 shows delay versus line length for this situation. In Fig. 1(a), the wire parameters are extracted at 100 MHz which is close to those extracted at dc. As expected, the *RC* model predicts a square dependence on line length while the ideal lossless *LC* model predicts a linear dependence on line length. The delays for these lines are dominated by lossless *LC* propagation. Hence, the simple *RC* approximation underestimates the delays for lines as long as 15 mm.

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As will be discussed in a later section, the inductance is lower and the resistance is higher at a frequency of 3 GHz [Fig. 1(b)]. While the resulting delay is not as dominated by the inductance, it still has a significant effect on the delay. These plots clearly show that inductance can be important, and correct modeling of wires needs to include the fact that the inductance and resistance of a wire is frequency dependent.

This figure greatly overstates the effect of inductance in short wires, as it ignores the effect of the driving gate. The effective output resistance of the driving gate adds to the line resistance, resulting in negligible inductance effects for short lines [4]. However, as the driver delay continues to scale down, the break point where inductance becomes an issue progressively becomes shorter [5], [6].

Over the past decade, the study of parasitic on-chip inductance in a digital chip has progressed tremendously, from the simulations and measurements by Priore [7] and Deutsch [8] demonstrating the significance of on-chip inductance to delay optimization for repeaters with *RLC* lines by Ismail [9]. Although there is an agreement that on-chip inductance is important, existing estimation and measurement techniques as well as the resulting guidelines differ vastly. Restle [10] reports on the use of inductance in the optimization of a clock distribution network and uses an accurate time-domain model for on-chip interconnects [11]. Soumyanath [12] and Morton [13] use on-chip sampling to measure driver and receiver waveforms. Singer [14] and Rusu [15] refer to on-chip inductance guidelines, while Gieseke [16] and Benschneider [17] use reference planes to suppress inductance and crosstalk. Deutsch uses time-domain technique to study a wide range of structures in [18]–[20], and gives an overview of various time and frequency-domain techniques in [21].

This paper shows how wire parameters can be extracted using S parameters. This technique is then used to extract wire parameters for a test chip, and simple curve-fitting models are given for how the wire parameters vary with some design parameters. The frequency dependence of the extracted R, L, G, C parameters is presented, and the implications of the frequency-dependent line inductance and resistance are illustrated with SPICE transient simulations. The paper also describes a new ring oscillator that confirms the accuracy of the extracted line parameters. One limitation of this work is that it does not deal with modeling of inductive noise coupling, which is one of the most significant effects of inductance [6], [11], [12], [20].

II. Frequency-Domain S-Parameter Characterization

Direct time-domain approaches are currently preferred in the analysis of on-chip interconnects [8], [10], [12], [13], [21]. Williams [22] gives a brief discussion of some of the time-domain versus frequency-domain characterization tradeoffs. Based on its potential practical and technical advantages as well as our experience with a network analyzer in the characterization and design of high-speed analog interconnects [23] and circuits [24], S-parameter characterization is used in this study.

Frequency-domain S-parameter characterization is carried out by launching waves from both ends of a signal line and measuring the reflected (S_{11}) and transmitted (S_{21}) network parameters. The probes are calibrated to better than 0.1 dB over the whole frequency range (0.1–20 GHz) by using a separate open, short and load calibration substrate. Only one pair of dummy open structures is required for de-embedding the pad parasitics, thereby minimizing the area overhead as well as the test time and measurement uncertainty. It also provides a straightforward extraction of the frequency-dependent loss and impedance, as well as the R, L, G, C parameters, as shown by Eisenstadt [26], Yue [27], and Shih [28]. The time-domain representation is also available with an inverse Fourier transform of the measured S parameters. Adjustment of windowing and time gating is supported on the HP8510c network analyzer to filter out unwanted reflections and improve the dynamic range of the converted time-domain measurements. Translation of the S parameters to the time domain is used extensively by Beyne [29] to measure package parasitics. S_{11} provides the time-domain reflection data (TDR), while S_{21} provides the transmission data (TDT).

III. Test Structure Design

In many circuits, the resistance R and capacitance C of a line are sufficient to characterize an interconnect. The R and C can be extracted from layout based on line width, thickness, and spacing to adjacent lines and layers. However, as the processor frequencies continue to scale, the inductive coupling and return resistance may become significant, as studied by Deutsch [21]. Restle [10] measures signal propagation on a large microprocessor. In this study, a reference test structure will be compared to a new test structure that closely mimics the environment of a real chip to facilitate quantitative calibrations.

Isolated reference test structures are designed as shown in Fig. 2(a). The interconnect process provides five layers of AlCu. Orthogonal ground lines are inserted in M4 in order to achieve a controlled capacitance to the signal lines in M5. The ground lines are connected to the substrate through substrate taps along the whole length of the line as shown in the cross section. The signal line widths and spacings are varied over a wide range of values in order to observe the effect of coupling through the silicon substrate.

The overall philosophy of our realistic test structure was to mimic as closely as possible a real chip with active drivers driving random lines, a regular power grid in the topmost metal layers, and local power/routing at the lower metal layers. Instead of making separate test structures, a typical power grid in M5 is connected to an orthogonal power grid in M4 [5] for a 4×4 mm^2 chip. This is continued down to local power grids in M1/M2 that is only continuous within 300×300 μm^2 regions of the chip to simultaneously mimic separate units on a chip and to test if the presence of the noncontinuous grid affects the inductance of global lines in M4 and M5. In a real chip, there is a large decoupling capacitance between V_{dd} and Gnd, making them both effectively ac ground. This is exploited in this test chip design by only routing Gnd and studying the effect of spacing to Gnd. Signal lines are implemented in both M5 and M4 with the same widths and spacings to the adjacent power lines as the reference test structures. The line capacitance is

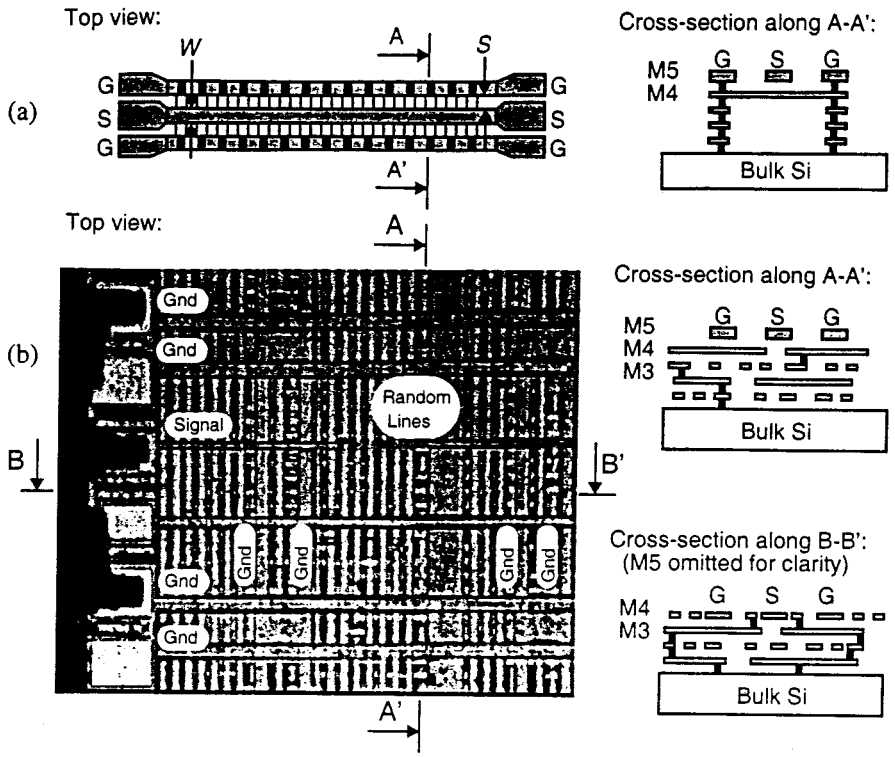

Fig. 2. Test structures implemented in a five-layer 0.25-μm CMOS technology. (a) Reference test structure. (b) New structure that mimics a real chip environment. A coplanar G-S-G probe used for characterization is visible in the die micrograph.

similar to that of the reference test structure, but the coupling is mostly to the orthogonal random lines in M3 and M4.

A real chip typically exploits all metal layers for routing. This has been approximated in our test chip by inserting pseudo-random signal lines in M4 and M3, as illustrated in the die micrograph and cross sections in Fig. 2(b). No random lines are left floating. There are random vias connecting M4 to M3 and random vias connecting M3 to the drains of bias transistors through local interconnects in M1 and M2. The source of each bias transistor is connected to the power grid and to a nearby substrate tap. The transistors can be biased on or off to emulate a real chip where the return paths may change depending on the logic state. Although the pad parasitics are de-embedded, the capacitance is minimized by using small pads, 43×67 μm^2, in the top metal layer only surrounded by ground shields. To be able to observe the inductive effects at high frequencies, intermediate length lines of 4 mm are used.

IV. Characterization Results

The telegrapher's equation $RLGC$ parameters were extracted from S parameters using well-established techniques reported by Eisenstadt [26], Yue [27], and Shih [28]. In the following sections, the extracted line inductance, line resistance, and shunt conductance will be described in detail.

A. On-Chip Inductance

The inductance versus line spacing is shown in Fig. 3. FASTHENRY field solver simulations [31] of the reference structure adequately predicts the inductance. The inductance increases for increasing spacing because more flux is enclosed

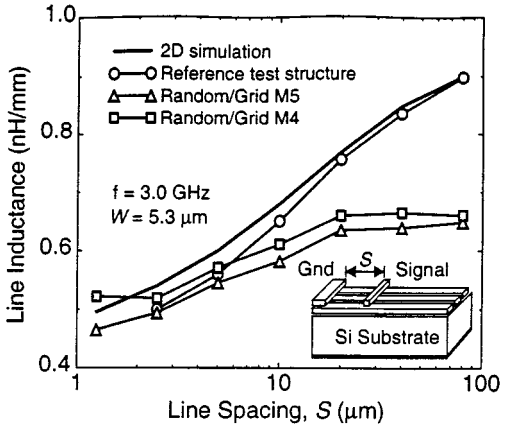

Fig. 3. Inductance versus line spacing for 5.3-μm-wide lines at 3 GHz. Reference test structure compared with FASTHENRY simulations.

between the signal line and the return ground. The inductance increases by about $2\times$ when the line spacing increases from 2.5 to 80 μm. The dependence on line spacing is much weaker for the test structure with a power grid and random lines. The increase is only about 25% for both M5 and M4 lines.

For large spacings, the inductance in the grid is lower than that of the reference structure. The effective return path must therefore be closer than that predicted by the spacing to the adjacent ground line. This inductance reduction can be explained by the presence of parallel random lines and local routing between the signal and the adjacent ground lines. For M5 signals, the parallel random lines are in M3 and M1. Some of the random lines run in parallel directly underneath the signal lines. For M4 signals, the parallel random lines are in M4 and M2. The M4 and M5 signal

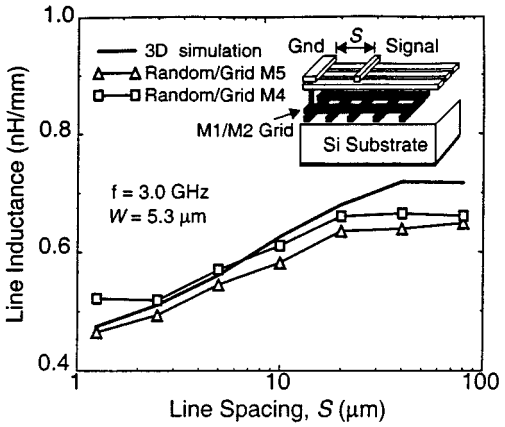

Fig. 4. Inductance versus line spacing of random/grid structure at 3 GHz. Comparison with 3-D FASTHENRY simulations incorporating local M1/M2 power grids, but not M3/M4 random lines.

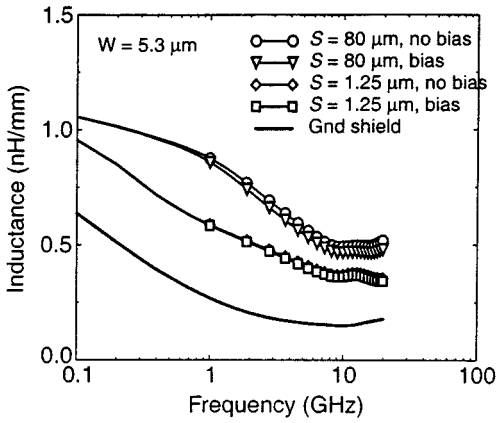

Fig. 5. Line inductance versus frequency for a 5.3-μm-wide line with large (80 μm) and small (1.25 μm) spacing to adjacent ground line for new realistic test structure. A bias on the gate drivers of the random lines has minor effect. Measured signal line with ground shield underneath showed for reference. There are 201 datapoints for each set of data. Not all symbols are shown in order to highlight the slight differences. Lowest frequency point is 99.5 MHz (not shown on this graph).

lines can couple inductively to the parallel random lines which effectively reduces the line inductance. They can also couple capacitively to orthogonal random lines that in turn connect or couple to parallel random lines. The presence of local routing in M1 and M2 could also affect the inductance.

It is difficult to model the complete chip with all the random signal and power lines. However, the presence of the regular local power grid in M1 and M2 with line widths of 1 μm and a pitch of 15 μm$\times$15 μm was expected to have a significant effect, especially for large spacings. Similarly to what was observed by studying the effect of a high- and a low-resistivity substrate in [5] and [6], the grid changes the electromagnetic field configuration, and the time-varying magnetic field induces eddy current that would tend to reduce the effective signal inductance. The effect of the M1/M2 power grid should be more pronounced due to the lower metal resistivity. This regular local power grid in M1 and M2 could also be readily modeled with a FASTHENRY three-dimensional (3-D) simulator. This is compared with the random/grid measurements in Fig. 4. The presence of the grid is indeed significant. However, it does not completely explain the reduction of the inductance for the very large spacings. The discrepancy is believed to be due to the coupling to the parallel random signal lines.

The extracted inductance versus frequency for the random/grid structure is shown in Fig. 5. The inductance reduces significantly with increasing frequencies for both a large (80 μm) and small (1.25 μm) spacing. As shown in [5], this trend is more significant than that of the reference structures, supporting the explanation of a combination of capacitive and inductive coupling to the grid and random lines. Applying a bias to the transistors that terminate the random lines results in a lower return impedance and hence a slight reduction in the signal inductance for the large spacing (drivers ON in Fig. 5). This confirms that the coupling to the random lines does have an effect on the signal inductance. The difference between bias on and off is barely noticeable for the small spacing due to the smaller return path. For reference, the inductance of a line with a blanket metal shield underneath is also shown in Fig. 5. This microstrip line has a significantly lower inductance due to the continuous return path underneath the line. The usage of power planes in between signal layers as suggested by Gieseke [16] and Benschneider [17] thus reduces the inductance significantly beyond that due to random lines and power grids. There is an increase in the inductance below 1 GHz for the microstrip line. This is due to the spreading of the current in the 0.5-μm-thick ground shield to minimize the impedance which is dominated by resistance at low frequencies. Notice that this trend is the case also for the small spacing without the ground plane.

It is important to note that the use of spacings to power and ground exceeding 10–40 μm is seldom the case in a digital chip, since smaller spaces reduce inductive noise coupling. Furthermore, a large portion of the topmost metal layers is usually dedicated to power and ground to create low power-supply impedance. Thus, it may be possible to simultaneously reduce inductance and crosstalk while achieving low-resistance power distribution at minimal overhead. However, the study of a wide range was useful to see the trend of inductance versus spacing. Knowing this dependence may also be helpful in exploring completely new designs, as demonstrated by Woods [32], who uses both large signal spacing (60 μm) and line widths (60 μm) in the design of a multigigahertz clock.

To illustrate the critical parameters in a real chip environment, the extracted inductance was fitted to a simple formula, as follows:

$$L = 0.6 + 0.03 \cdot \ln(S) - 0.15 \cdot \ln(W) + 0.13 \cdot \ln\left(\frac{7.0}{f}\right). \quad (1)$$

Notice that the inductance (L in nanohenry per millimeter) is mainly a function of line width (W in micrometers) and frequency (f in gigahertz between 0.1–7 GHz). The dependence on the spacing to the adjacent ground line (S in micrometers) is so small that it can almost be ignored. At frequencies between 7–20 GHz, the frequency dependence is even weaker and (1) reduces to

$$L = 0.6 + 0.03 \cdot \ln(S) - 0.15 \cdot \ln(W). \quad (2)$$

It is important to note that this formula is a fit to our specific test chip and process. As the technology scales to more layers

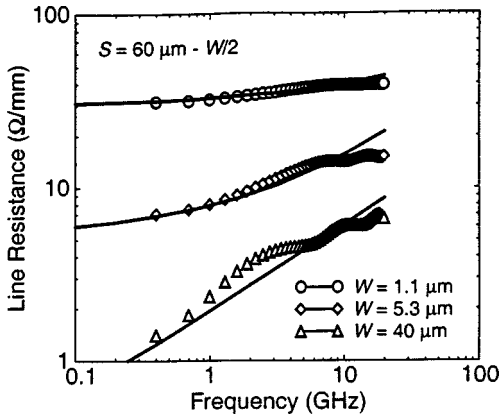

Fig. 6. Comparison of (5) and experimental data of line resistance for new random/grid test structure.

of metal, the inductance dependence on spacing is expected to reduce. In addition to spacing, this curve-fitted formula also captures the effective inductance of a wide bus (e.g., 32 bits) using the effective width of all the 32 lines switching in the same direction. There are several cases of many-to-one capacitive and inductive crosstalk that are clearly not captured by this simple formula. As shown in [5], S parameters can be successfully used to measure the inductive crosstalk. A more detailed study of these important effects are presented by Qi [6], Restle [11], Soumyanath [12], and Deutsch [20]. In addition to inductance, other parameters also need to be considered, as illustrated in the following section.

B. Frequency-Dependent Resistance and Loss

The extracted series line resistance is shown for three different line widths in Fig. 6. For the 1.1-μm-wide line, the resistance varies from 31 Ω at 100 MHz to 40 Ω at 20 GHz (29% increase). For the 5.3-μm-wide line, the resistance varies from 6.7 to 15 Ω (124%), while for the 40-μm-wide line it varies from 1.1 to 6.5 Ω (490%). This frequency dependence is more significant than that reported by Deutsch [19] and Krauter [33] using 2-D and 3-D extraction. One important reason for the discrepancy with earlier published data is the use of much larger spacing and widths resulting in a higher impedance return path.

A comparison with the ideal skin effect calculations for aluminum reveals an unexpected discrepancy. Equation (3) relates the aluminum skin depth, δ_{Al} (μm) versus frequency, f (GHz) for AlCu with a resistivity of $\rho = 35$ m$\Omega \cdot \mu$m [25]:

$$\delta_{\mathrm{Al}} = \frac{3}{\sqrt{f}}. \tag{3}$$

Yue [27] derives the resistance (Ω) for an aluminum line with width W (μm), length l (μm) and thickness T_{Al} (μm) as

$$R = \frac{\rho \cdot l}{W \cdot \delta_{\mathrm{Al}} \cdot \left(1 - e^{-T_{\mathrm{Al}}/\delta_{\mathrm{Al}}}\right)}. \tag{4}$$

For a 1-μm-thick M5 line, (4) predicts an 83% increase in line resistance from 100 MHz to 20 GHz. This overestimates the observed variation for the 1.1-μm-wide line (29%) and significantly underestimates the variation for the 40-μm-wide line (490%). Equation (4) also predicts a smaller frequency dependence for the 0.5-μm-thick M4 line (38%) while the observed dependence is similar to that of M5.

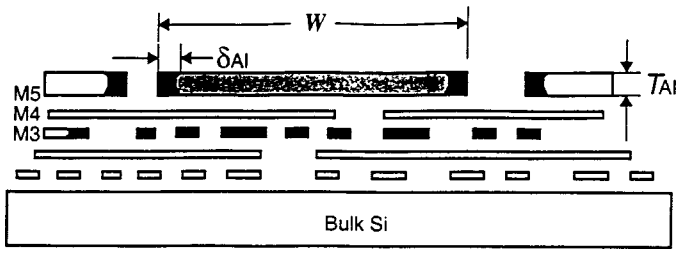

Fig. 7. Cross section illustration of lateral skin effect for wide lines.

The simple skin-effect formula clearly does not capture all the physical mechanisms that cause the resistance to increase with frequency in this real chip environment. According to the measurement, the return current flows mainly in the parallel lines underneath or next to the signal line, even though the capacitive coupling is mainly vertical (down to the orthogonal lines). A cross section of a signal line in the power grid with random lines is illustrated in Fig. 7. The shaded line is the signal and all the other lines are either ground or random lines. A possible current distribution is illustrated in black. The current in the signal line crowds toward the two edges to minimize the return path in the adjacent signal or ground lines. However, there is also a return path contribution from the parallel lines and substrate directly underneath a wide line. By adding a linear term that is proportional to the line width to a lateral skin effect model yields (5). A comparison to the experimental data for the new test structures is shown in Fig. 6. An excellent curve fit is observed in the range of 0.1 to 10 GHz.

$$R = \frac{\rho \cdot l}{T_{\mathrm{Al}} \cdot 2 \cdot \delta_{\mathrm{Al}} \cdot \left(1 + \frac{W}{20}\right) \cdot \left(1 - e^{-W/(2 \cdot \delta_{\mathrm{Al}})}\right)}. \tag{5}$$

The environment in a digital chip—with a power grid, random lines, and a low-resistivity substrate—does not lend itself to a simple analytical prediction. The exact form of (5) will therefore depend on the process technology as well as the distribution of neighboring signal and power lines. Nevertheless, the general form of (5) is instructive in the sense that the lateral skin effect adequately explains the frequency behavior for relatively narrow lines which constitute the largest percentage of interconnects in digital circuits. The spacing to the adjacent ground line is not included in (5). For the 5.3-μm-wide line and a small spacing of 1.25 μm, the resistance increases by 50% from 0.1 to 20 GHz versus 124% for the similar width line in Fig. 6 width a spacing of 57.4 μm. This reduced increase versus frequency is due to better ground return resistance and reduced coupling to the M1/M2 grid and the substrate. More data points would be required (especially small S for large W) to curve fit an equation to both W and S.

The line loss versus frequency is shown in Fig. 8(a). Although the 40-μm-wide line has the lowest loss at 100 MHz, it has the highest loss above 4 GHz. The series resistance of the 40-μm-wide line is still the lowest up to 20 GHz. The dominant loss mechanism of the wide line must therefore be related to the shunt admittance. It is clear from the extracted shunt conductance in Fig. 8(b) that it cannot be ignored for wide lines and

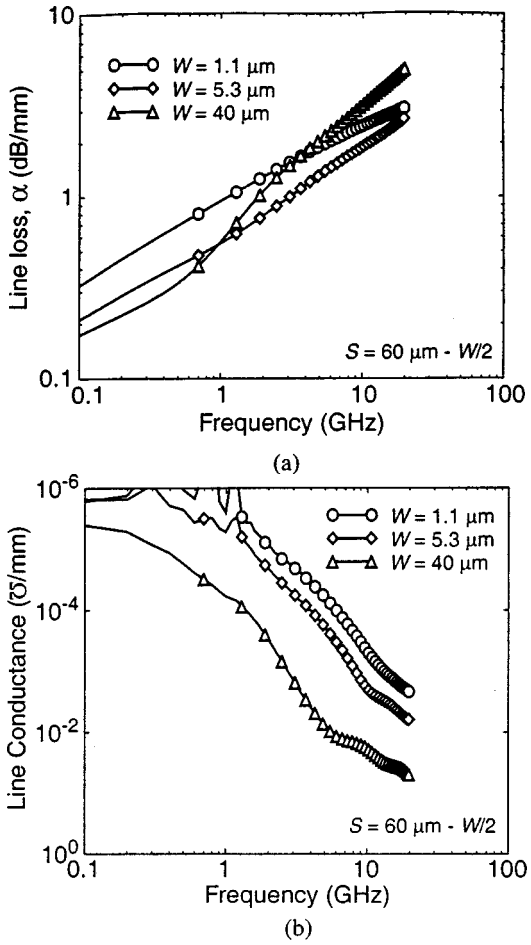

Fig. 8. Frequency dependency of (a) line loss and (b) shunt conductance for new random/grid test structure.

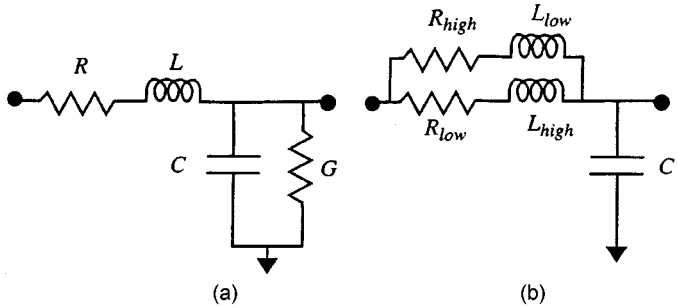

Fig. 9. (a) Telegrapher's equation $RLGC$ model. (b) Proposed *RLC* model.

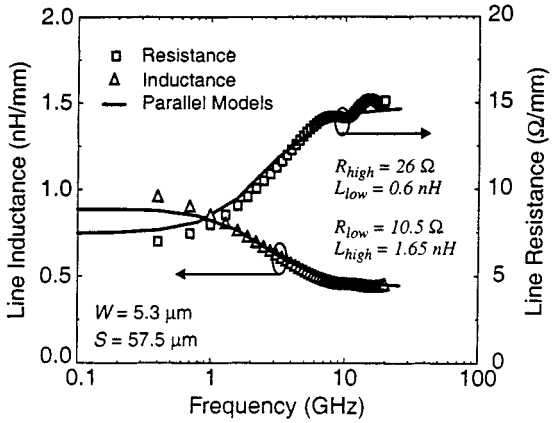

Fig. 10. Comparison of parallel *RLC* model as shown in Fig. 9(b) with experimental data from Figs. 5 and 6.

buses. Again, the apparent disagreement with [19] (reporting a small shunt conductance below 10 GHz) is due to the extremely wide lines studied in our work. The SiO_2 dielectric loss at these frequencies is relatively small and can clearly not explain a shunt G of 1/(100 Ω) per millimeter for the 40-μm-wide line. As explained in [23], the frequency-dependent increase of a shunt conductance can be explained by a capacitance in series with a resistor: at low frequencies, the circuit looks like an ideal capacitor, while at high frequencies the series resistance makes the capacitance look lossy. Thus, even a constant ground return resistance in series with the line capacitance will result in a shunt conductance that appears to increase with frequencies in the extracted telegrapher's equation. This apparent shunt loss is therefore consistent with earlier studies of the ground return resistance [11], [21]. In addition, the induced eddy currents in local interconnect loops and eddy currents in the silicon substrate that reduces the inductance for large spacings in Fig. 4 will also contribute to the effective shunt loss at high frequencies. Separate test structures would be required to quantify the contribution of these different loss mechanisms.

V. Transient Analysis With Extracted Parameters

In the previous sections, we studied the unloaded line characteristics. For many global lines and buses, the unloaded line capacitance is a good approximation to the actual circuit due to the small receivers typically used for on-chip interconnects. However, the added gate and local routing capacitance can affect some heavily loaded interconnect circuits. Ideally, the frequency-dependent parameters of the general $RLGC$ model in Fig. 9(a) should be used in the simulations. However, frequency-dependent parameters are currently not supported in many transient circuit simulators such as SPICE. To incorporate the effects, the more general solution is to modify the simulator as proposed by Chang [27]. The frequency-dependent effects can also be approximated with an equivalent model as shown by Deutsch [21], Krauter [33], Yue [34], and Zheng [35]. An *RC* network to model the frequency-dependent shunt component was used in [23]. The shunt conductance was found to have an insignificant effect on the relatively narrow 5.3-μm-wide line in this circuit and was therefore not used. A parallel *RLC* model that approximates the dominant frequency-dependent behavior of an interconnect is shown in Fig. 9(b). At low frequencies, the current flows mostly in the low-resistance high-inductance path ($R_{\text{low}} - R_{\text{high}}$), while at high frequencies, it flows mostly in the high-resistance low-inductance path ($R_{\text{high}} - R_{\text{low}}$). By minimizing the normalized error of both the resistive and inductive components, this model yields an excellent fit to the experimental data in the frequency range of 100 MHz to 20 GHz, as illustrated in Fig. 10.

Different interconnect models are compared using transient simulations of a clock line in Fig. 11. A 4-mm-long line is simulated with a gate load at the end of the line and the output of the receiver unloaded. The frequency-dependent model is compared

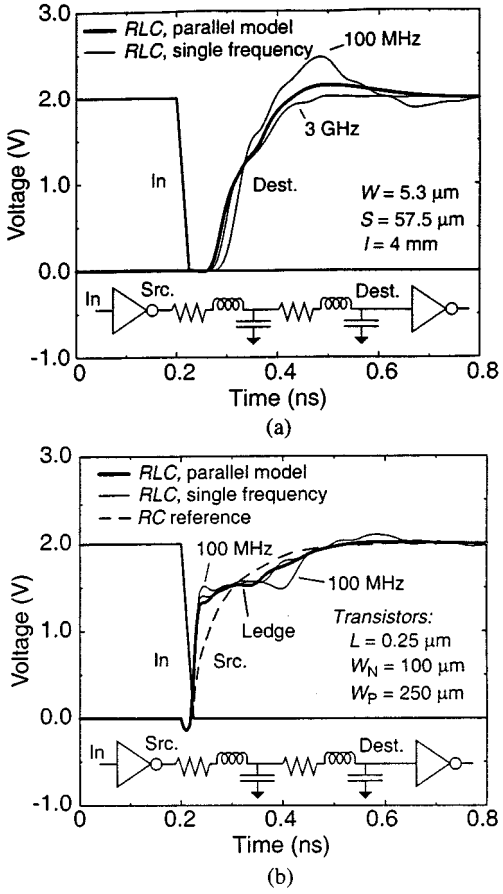

Fig. 11. Distributed *RLC* SPICE simulations with parallel *RLC* model and fixed-frequency *RLC* model extracted at 100 MHz and 3 GHz. Five *RLC* segments are used in the simulations (only two are illustrated). (a) destination waveforms and (b) source waveforms.

with fixed-frequency models extracted at two different frequencies (100 MHz and 3 GHz) at the source and the destination of the line.

In Fig. 11(a), the destination waveforms are compared. The frequency-dependent model predicts a smaller initial delay below 1 V. This is due to the lower inductance for frequencies *above* 3 GHz. The delay to $V_{dd}/2$ is 84 ps. This is close to that predicted with the *RLC* model extracted at 3 GHz (85 ps). The frequency-dependent model predicts significantly less overshoot and ringing than the 100-MHz model. This is due to the higher inductance and lower series resistance extracted at 100 MHz (close to dc). However, the 3-GHz model predicts no overshoot, while the frequency-dependent model does have a small overshoot. The higher inductance and lower resistance at the lower frequencies therefore cannot be ignored.

In Fig. 11(b), the source waveforms are compared. There are only slight differences between the *RLC* models. The initial ledge voltage is lowest for the frequency-dependent model, indicating again that the frequency components above 3 GHz are significant: the lower inductance at these frequencies result in a lower characteristic impedance. The initial ledge voltage is highest for the model extracted at 100 MHz due to the high inductance. The low-frequency model also has the longest ledge due to the longer line delay.

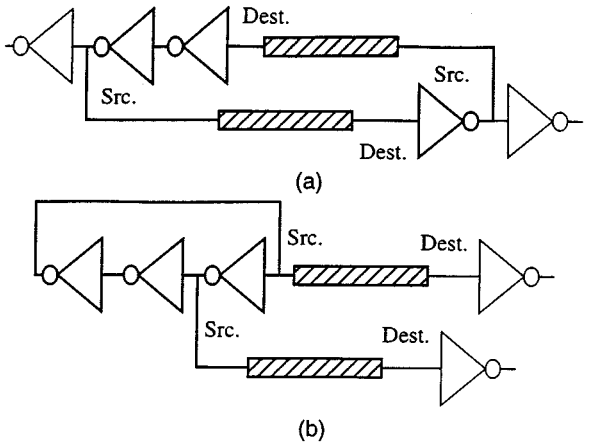

Fig. 12. Ring oscillators with connections at (a) destination and (b) source.

The simple *RC* model extracted at dc is also shown for comparison in Fig. 11(b). The *RC* waveform does not have a distinct ledge voltage. The delay from the input to the source and the source rise time are much *longer* than for the *RLC* models. The simple *RC* model overestimates the line capacitance initially seen by the driver. The presence of the inductance in the *RLC* model effectively limits the line capacitance that is initially seen by the driver, resulting in a short delay to the source. The line *RC* delay from the source to the destination is is still much shorter (40 ps versus 85 ps for the *RLC* model), consistent with the results shown in Fig. 1.

VI. Inductance-Sensitive Ring Oscillator

It is clear that a simple *RC* model can underestimate the line delay significantly. The more accurate *RLC* model predicts a longer delay but also a faster transition time. However, the delay through the receiver at the destination is related to the transition time. An increased delay due to a higher line inductance may be offset by a reduced receiver delay. Hence, a ring oscillator incorporating a line in between the stages would not be sensitive to the details of the interconnect model [Fig. 12(a)]. Morton [13] uses this destination-connected ring oscillator to measure a wide range of interconnect structures. An excellent match with simulations is observed, but the oscillation frequencies vary by only $\pm 10\%$. It may be difficult to extract detailed interconnect parameters with such a small difference in oscillation frequency amongst variations in power supply and device characteristics across the wafer. In Fig. 12(b), the capacitive loading on the ring oscillator is similar to that of Fig. 12(a), but the inverters are connected at the source ends of the lines. This structure studies the details of the waveform at the source. If the inverters in Fig. 12(b) have a low impedance compared to the interconnect characteristic impedance, the ledge voltage at the source [as illustrated in Fig. 11(b)] could be sufficient to trip the next inverter in the ring. This would result in a substantial increase in the oscillation frequency compared to the destination-connected ring oscillator. This increase in oscillation frequency will be a clear evidence of the significance of inductance.

Several three-stage ring oscillators were implemented in a 0.25-μm five-metal layer CMOS process. A reference ring os-

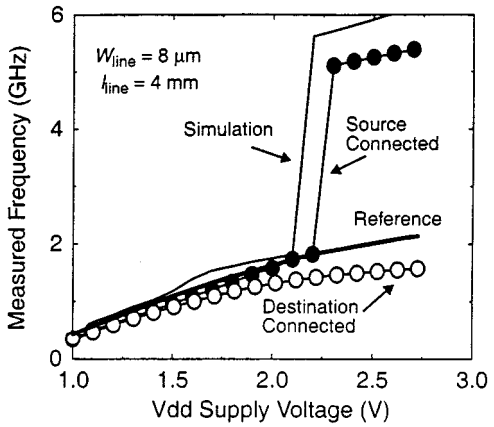

Fig. 13. Measured and simulated ring oscillators characteristics. The simulations used the model of Fig. 9(b).

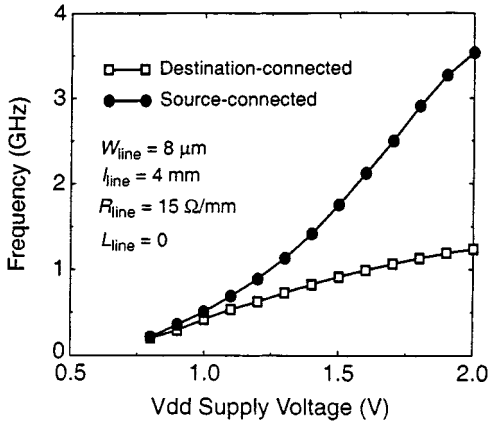

Fig. 14. Simulated characteristics of *RC*-dominated ring oscillators.

cillator was designed to have the same capacitive load but negligible inductive load. The oscillators were placed in a power grid with short-channel on-chip decoupling capacitors to provide a stable power supply and provide ac ground return in V_{dd} lines in addition to the V_{ss} lines. The output impedance and the gate delay of the inverters are a function of the supply voltage (V_{dd}). The ring oscillator frequency variation with V_{dd} is shown in Fig. 13. The reference ring oscillator has a slightly higher frequency than the destination connected oscillator. This difference becomes more pronounced for large V_{dd} when the gate delay is reduced in comparison with the interconnect delay. However, it is difficult to extract the detailed interconnect characteristics from this set of measurements. The source-connected ring oscillator behavior confirms that at a critical V_{dd}, the ledge voltage at the source becomes sufficient to trigger the next stage. This causes the oscillator frequency to increase rapidly. Simulations using the model in Fig. 9(b) adequately predict the line delay, the line characteristic impedance, and the transition to a higher oscillating frequency at sufficiently high V_{dd}.

The source-connected ring oscillator is expected to have an increase in the frequency with V_{dd} even with the line modeled as *RC*. A simulation was therefore carried out with the same ring oscillator model but with zero line inductance and an increased series resistance ($R = 15\,\Omega/\text{mm}$). Fig. 14 confirms that a sizeable increase in frequency with V_{dd} is indeed observed for the source-connected ring oscillator. However, the frequency increase is gradual with V_{dd}. This characteristic is distinctly different from the sudden change in frequency observed when the inductance effect is considered, reflecting the difference in the source waveforms illustrated in Fig. 11(b).

If the transition is fast, the characteristic impedance $\{Z_0 = \text{sqrt}(L/C)\}$ will match the driver strength close to the transition voltage. By knowing the line capacitance and the driver strength at this bias from E-test characterization and by using matched driver pull-up and pull-down strengths as well as receiver trip points at $V_{dd}/2$, the effective line inductance can be extracted. Different line lengths and gate loads as well as comparison with simulations can further improve the accuracy of extracted inductance and line delay. If combined with on-chip dividers, the ring oscillator test structures enable the characterization of on-chip interconnects without the need for high-frequency probes. The essential information would be contained in the frequency versus V_{dd} characteristics. The transition to a high-frequency oscillation in Fig. 13 occurs at a voltage below the normal operating voltage ($V_{dd} = 2.5$ V in this process). This indicates that the driver has a lower impedance than the on-chip interconnect. This impedance mismatch will result in overshoot and ringing.

VII. Conclusion

Several test methods and test structures for high-speed on-chip interconnects were investigated. The S-parameter characterization enabled extraction of frequency-dependent line resistance, inductance, and conductance with a test structure that mimics a real chip environment. The use of a network analyzer further enabled a low area and testing overhead of a pair of open pads for parasitic de-embedding. Combined with the use of lines in both x and y direction of the test chip, it allowed a vast range of line spacings and widths to be studied. The inductance dependence on line spacing is weaker than that predicted with reference test structures due to coupling to random lines and local power grids. This is good news for digital designs that often try to suppress the inductive effects, particularly since this coupling is expected to continue to increase as CMOS processes scale to more interconnect layers. Further inductive reduction as well as reduced crosstalk can be achieved with the conventional method of suppressing the inductance by reducing the spacing to the adjacent ground line.

On-chip inductance can cause an increase in the delay for fast clock lines, severe ringing, and noise for wide bus lines and power-supply ringing for V_{dd}/V_{ss} lines. To illustrate the significance of these effects, the parameters extracted in the frequency domain were analyzed in the time domain with transient simulations of a parallel *RLC* model. The complete model is required to accurately capture the interconnect behavior due to variations of inductance and resistance versus frequency. The extracted parameters are used to accurately predict the characteristics of an inductance-sensitive ring oscillator fabricated in a five-layer metal 0.25-μm CMOS technology.

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