Impact of On-chip Inductance on Power Distribution Network Design for Nanometer Scale Integrated Circuits

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Abstract

This work presents a compact methodology for power distribution network design in a nanometer scale VLSI chip using a noise-area tradeoff analysis which considers on-chip inductance effects. This methodology is used to quantitatively demonstrate the importance of considering on-chip power grid inductance, and how its impact scales with technology. While increasing power supply noise levels (which become worse with on-chip inductance) are expected to adversely impact the chip's power supply grid design, this work demonstrates that a power grid optimized with on-chip inductance considerations can lead to significant improvement in the wiring resource utilization.

1. INTRODUCTION

Efficient power distribution network design is a key factor in the performance of modern VLSI circuits [1]. As we move into sub-100nm technologies, device packing densities, power consumption levels and switching speeds place tremendous demands on the chip power distribution network. The parasitic elements in the wires from off-chip power supply sources to the terminals of each transistor cause voltage drops which reduce the effective supply voltage seen at the terminals of the devices and degrade circuit performance. This transient shift of supply voltage levels is called power supply noise. Excessive power supply noise may lead to effects like increased signal delay and delay uncertainty [2], on-chip clock jitter [3] and reduced noise margins [1].

Conventional computer aided design flows for chip power distribution networks start at a very early stage of the physical design process when little is known about the specific current requirements in different parts of the circuitry. The coarse assumption of uniform power supply requirements across the chip makes it easy for an early conservative allocation of wiring resources for the power supply. In later design stages this coarse design is refined as more information about current requirements of local logic circuitry becomes available. Later, for circuit analysis, equivalent RLC circuit representations of the whole power network are used in a layout-based verification step. Problems detected in the power supply grid at this late stage, when the physical design is near completion, are extremely expensive to redesign. On the other hand, interconnect limited technologies [4] of the sub-130 nm era make an overly conservative power distribution network too expensive as it uses up valuable wiring resources. Hence it is necessary to have an accurate and simple method to design a cost-effective and robust power supply grid early in the design cycle.

Role of On-Chip Inductance:

The two major contributors to power supply noise are resistive *IR* voltage drop [5] and inductive *L(di/dt)* voltage drop [6]. Inductance on the power supply network appears mainly in the bonds connecting power supply pins on the chip to the off-chip wires in the case of wire-bond-packaging technology. In nanometer scale VLSI, on-chip inductance that appears in wires forming the chip's power supply grid has become a matter of growing concern. This is due to the trend of decreasing rise time of transient currents on the power supply network coupled with the introduction of low-inductance packaging technologies like ball-grid array or flip-chip bonding [7]. However, the state of the art presents two gaps in addressing this aspect of power distribution network design. Firstly, there is a lack of concrete evidence to justify the inclusion of on-chip inductance considerations in early power grid design. Secondly, there is a need for a compact framework that embodies our understanding of on-chip inductance and can be easily integrated in the computer aided design flow. Our paper attempts to fill these gaps.

Scope of this Work:

This paper presents a simple mathematical formulation of the tradeoff analysis between power supply noise and power grid area. The critical aspects of package inductance, interconnect resistance, on-chip interconnect inductance and the presence of on-chip decoupling capacitors [8] that are typically used to mitigate excessive power supply noise are taken into account. The model is used to optimize the design of a regular power grid that supplies power to a small block of logic circuitry for a nanometer scale VLSI chip. We show that considering on-chip inductance not only gives a more realistic estimate of power supply noise but also leads to smaller widths for wires constituting the power grid. The intent of this study is not to predict power supply noise with high accuracy, but to frame an early power grid design methodology and to determine the impact of on-chip inductance on power grid design for current and future technology generations. It is shown that although power supply noise levels are increasing and on-chip inductance adds to that problem, the inclusion of on-chip inductance considerations interestingly leads to significant improvement in wiring resource utilization.

2. PREVIOUS WORK

Larsson [9] has discussed the scaling trends of various components of noise in the power distribution network. The trend of increasing power supply noise as VLSI technology progresses into the deep sub-micron regime has been demonstrated with regard to resistive and inductive noise in wire-bonded ICs [7], package level inductance [9] and more recently based on ITRS [10] predicted technology scaling in [11]. The inductive voltage drop seen on the power network has been a matter of growing concern with the rising *di/dt* and overall faster switching of VLSI circuit components, which in turn leads to higher frequency transient currents on the chip's power/ground network. The advent of novel packaging techniques like ball-grid arrays have done well to reduce package inductance [1, 7], but on-chip inductance is now emerging as another significant contributor to noise on the power distribution grid [12].

Research on the characterization, extraction and modeling of inductance in signal wires and VLSI interconnects in general

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has been prolific [13-16]. The performance impact of on-chip inductance is an important aspect of interconnect design [17]. [18, 19] address modeling and analysis of power-grid inductance. On the other hand, inductance of on-chip power/ground wires with regard to designing a power grid in particular has received less attention. Some works that address this aspect of power distribution network design are discussed below.

The effect of layout considerations (like using narrower inter-digitated nets instead of using wide nets and placing power and ground lines in close proximity to each other) on power/ground network inductance and therefore on power supply noise has been presented in [20]. The work in [21] provides a comprehensive analysis of the variation of grid inductance for different power grid designs. They again point to the efficacy of using "paired" grids. Figure 1 depicts typical power grid designs based on the different topologies suggested in these works. [21] also provides an insight into the trade-offs that exist between resistance, inductance and area of the grid.

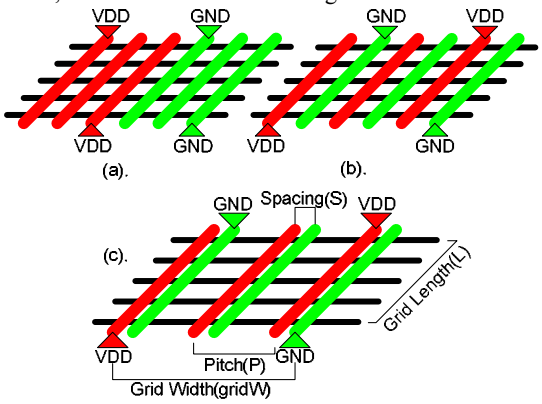

Figure 1: Power/Ground grid structures: (a). a non-interdigitated grid, (b). an interdigitated grid and (c). a paired grid (minimum inductance design).

Although these works present qualitative guidelines for designing a better power distribution network, they fall short of evolving a complete methodology that would guide a designer to choose appropriate parameters, like wire widths, for such designs. They also do not quantify the cost/benefit a designer would incur/earn by considering on-chip power grid inductance at such an early stage of the design.

The work presented here is novel because it develops a compact methodology to guide the early design of a power distribution network including on-chip inductance considerations, shows (quantitatively) at what costs these considerations may be excluded or included, and how these costs change with the scaling of VLSI technology.

3. COST FACTORS FOR POWER DISTRIBUTION GRID DESIGN

The objectives of a power distribution network design are to achieve low impedance (resistance and inductance), occupy small area (from the available wiring resources), and low current densities (for improved reliability against issues like electromigration). The choices regarding wire width or area allocation that cater to one of these objectives may very well be in conflict with another requirement. For example, a wider wire would occupy more area but is desirable because it has lower resistance. Hence, it is very important for the designer to have yardsticks with which to weigh one design objective against others.

The two major factors that are of concern to the designer are power supply noise and the amount of wiring area used by the power grid. Other factors such as increased delay, lower drive capability of devices, lower noise margins are side-effects of the supply noise. Consideration of power supply noise also tends to indirectly alleviate secondary problems such as electromigration reliability of the grid as these stem from high current densities and ringing voltages on the grid. Metal area ratio of the grid on the other hand translates into a direct cost as it off-sets the available routing area for logic and signaling circuitry. In the rest of this section we derive relations for the various contributors to cost associated with a power grid. These expressions are then used to develop the methodology to perform a tradeoff analysis of these costs.

The use of an approximate formula for power supply noise, assumed frequency independence of resistance and inductance and neglecting the effect of neighborhood switching wires on the grid inductance help us evolve a fairly simple optimization methodology for power grid design. However, at present-day frequency levels and within reasonable wire widths our analysis provides a close upper bound to the noise estimation. It must be kept in mind that the intent of this study is not to predict power supply noise with high accuracy, but to formulate an easy to use power grid optimization methodology and establish the trends of on-chip inductance impact on power supply grid design in current and future technology generations.

Power Grid Inductance

The paired grid topology (Figure 1c) is the design of choice when considering power grid inductance. Due to the proximity of the power and ground wires that constitute each power-ground pair the inductive coupling between them is large, whereas these wires are weakly coupled to the wires of an adjacent pair due to the relatively larger distance. The paired grid provides a nearby return path for transient current flowing through any power/ground wire, which means that the current loop area, and hence grid inductance, is small [14]. This topology exhibits not only minimum grid inductance but also the variation in inductance with grid width and length is linear [21]. The following simple formula can thus be used to get a fairly accurate estimate of the grid inductance [21, 22]:

$$L_{grid} = 0.004l\left[\ln\left(\frac{S}{W+t}\right)+1.5\right]\frac{P}{W_g}\ \mu\text{H} \qquad (1)$$

Here 'S' is the spacing between two power and ground wires that form a pair, 'P' is the interval (pitch) between two adjacent pairs, 'W' is the width of each wire, 't' is the thickness of the metal layer, 'l' is the length of the grid in cm, and 'W_g' is the grid width. Figure 2 shows a comparison of inductance calculated by Equation 1 to FastHenry [15] extracted inductance values for a power grid.

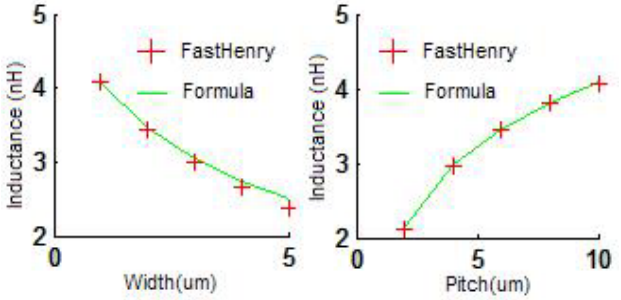

Figure 2: Comparison between approx grid inductance calculated by Equation (1) and that extracted using FastHenry [15] at 20 GHz, *S*=6µm, *t*=1µm, *l*=1mm.

The introduction of flip-chip technology with solder bumps for packaging chips leads to a significantly lower package inductance as compared to previous technologies like wire bonding. For the purpose of the analysis here, a constant package inductance of 1nH [7] associated with the package connecting the off-chip power supply to the on-chip power grid is assumed.

Inductive voltage drop is proportional to the rate of change of current on the power grid. The contribution of inductance to the cost of a power grid is thus evaluated as the worst case inductive noise shown in Equation 2.

$$N_L = \left(\left[L(di/dt)_{peak}\right]_{grid} + \left[L(di/dt)_{peak}\right]_{package}\right)/V_{dd} \quad (2)$$

In order to estimate the peak *di/dt*, a triangular switching current waveform is assumed (Figure 3) with current rising from zero to its peak value ($di=I_{peak}$) in time *dt*. Furthermore, the current rise/fall transition time in the package (dt_{pkg}) is assumed to be an order of magnitude longer than on the chip itself due to the presence of numerous transistor capacitances as well as decoupling capacitors on the chip [10].

Power Grid Resistance

The resistance of the grid can be directly calculated from the metal resistivity properties and dimensions of the grid, as shown in Equation 3, where ρ denotes the resistivity of copper, '*l*' is the length of the grid, '*W*' is the width of each wire that forms the grid, '*t*' is the thickness of the metal layer, '*n*' is the number of power/ground pairs, 'W_g' is the grid width and *'P'* is the interval (pitch) between two adjacent pairs of power-ground wires. The resistance is factored by 2 as each pair of power and ground wires (ref. Figure 1(c).) gives rise to a series resistance, and there are '*n*' such pairs in parallel.

$$R = \rho \frac{l}{W \times t} \cdot 2 \cdot \frac{1}{n} \; ; \; n = \frac{W_g}{P} \quad (3)$$

Resistive voltage drop is proportional to the current drawn from the power grid. The contribution of resistance to the cost of the grid is evaluated as the worst case resistive noise (IR drop) shown in Equation 4, where I_{peak} is as depicted in Figure 3.

$$N_R = I_{peak} R / V_{dd} \quad (4)$$

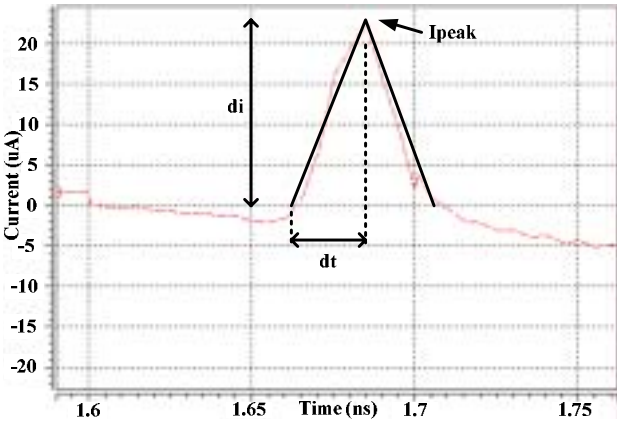

Figure 3: Triangular current waveform on the power supply grid showing peak current and *di/dt* when the circuit underlying the grid switches.

Power Distribution Grid Area Ratio

The area ratio of the power distribution network is the ratio of the metallization area occupied by power/ground wires to the total area available for metallization. Since power/ground wires use up valuable routing resources which could otherwise have been used for wiring the logic circuitry, the intent is to keep the area ratio as low as possible. Considering a metal layer where signal wires are laid out with spacing equal to the wire widths, then the total area available for metallization is $l_g W_g/2$ (W_g=grid width, l_g=grid length). The metallization area occupied by power/ground wires is $2Wl_gW_g/P$, where each power/ground line has width *W*. Hence, the area ratio (*A*) of the power grid is given by:

$$A = \frac{4W}{P} \quad (5)$$

Power supply noise (inductive and resistive) and area ratio of the grid contribute to the total cost associated with a power grid design. Design constraints, the intended usage of the chip and such factors would typically lead to guidelines about the relative importance of power supply noise (PSN) as against area used by the power distribution grid. Any power grid design would thus have a total cost expressed as a weighted sum of the PSN cost ($N=N_L+N_R$) and area cost (*A*). The designer's intent would always be to minimize the total cost by adjusting relative proportions of noise cost and area cost. The following section describes the methodology to design an optimal power grid by trading-off these cost factors.

4. TRADEOFF ANALYSIS FOR POWER DISTRIBUTION GRID DESIGN

Starting from an initial grid designed with typical physical dimensions, a general strategy would be to perturb the design by varying one of the variable parameters (say wire width) and find the effect on the total cost. The design solution moves in the direction in which the effect of such a perturbation is to reduce the 'total cost', to obtain new values of the design parameters. Such perturbations are made in the direction of cost improvement until either a). cost cannot be improved further, or b). a limit imposed by some design requirement is reached. The solution space for the power distribution network can be explored by using the following 'Incremental Cost', shown here as the Incremental Cost for wire width '*IC(W)*' (power supply noise is denoted as *N* and area ratio is denoted as *A*):

$$\frac{\Delta N}{N} = \frac{\Delta W\left(\frac{dN}{dW}\right)}{N} \; ; \; \frac{\Delta A}{A} = \frac{\Delta W\left(\frac{dA}{dW}\right)}{A}$$

$$IC(W) = \frac{\Delta N}{N} \times r + \frac{\Delta A}{A} = \Delta W\left[\frac{dN/dW}{N} \times r + \frac{dA/dW}{A}\right] \quad (6)$$

'*IC(W)*' is the increase in the cost when wire width increases by an amount *'ΔW'*. '*r*' denotes the relative importance of PSN with respect to area ratio as a contributor to the total cost of the network. For a particular design, if *'IC(W)'* is negative, it means the total cost will decrease if wire width is increased by an amount ΔW, and vice versa.

The foregoing analysis yields a simple expression that combines PSN and area ratio, and can be used to perform the trade-off analysis to obtain a better power distribution network design. The expression appearing in square brackets in Equation 6 is referred to as the Incremental Cost Function (ICF) (for Width) in the subsequent analysis.

$$ICF(W) = \left[\frac{dN/dW}{N} \times r + \frac{dA/dW}{A}\right] \quad (7)$$

The differential terms used in the incremental cost function expression can be easily evaluated by differentiating Equations 3-5:

$$\frac{\frac{dN}{dW}}{N} = \frac{-\left[\frac{2\rho lP}{W^2 t} + \frac{0.004lP}{dt(W+t)} \times 10^{-6}\right]}{\left[\frac{2\rho lP}{Wt} + \frac{w_g L_{pkg}}{dt_{pkg}} \times 10^{-9} + \frac{0.004lP}{dt}\left\{\ln\left(\frac{S}{W+t}\right) + 1.5\right\} \times 10^{-6}\right]}$$

$$\frac{\frac{dA}{dW}}{A} = \frac{1}{W} \quad (8)$$

Similar relations can be derived for the effect of other design parameters (like pitch) on total cost of the power grid. Simulations show, however, that wire width variation leads to the largest variations in total cost and potentially better solutions, whereas variation in pitch does not lead to much improvement. This is because the relative change in grid resistance or inductance due to a certain change in pitch is equal and opposite to that in grid area ratio. Hence this paper presents the analysis for wire width variations only.

In order to arrive at a reasonable value for 'r', the relative influence of PSN and area ratio on the total cost can be estimated in the following way. Starting with a power grid design whose physical parameters are known, PSN and area ratio are calculated using Equations 3-5. Since the number of grid lines is a measure of the cost of the grid, this number is then increased and the fractional changes in PSN and area ratio as a result of this increase are evaluated. The ratio of the fractional increase in area ratio to that in PSN gives a measure of 'r'. For example, a power grid at the 90 nm node with 13 power-ground wire pairs shows a 7.7% rise in area ratio and 1.83% fall in power supply noise when the number of power-ground wire pairs is increased to 14. Hence 'r' in this situation is a ratio of the two percentages (7.7/1.83 = 4.2). If the design places very stringent constraints on power supply noise levels while allowing the expense of a slightly larger area ratio, then the parameter 'r' can be assigned a correspondingly higher value, or vice versa.

The steps involved in the evaluation of an optimal wire width for a power distribution grid using ICF(W) are summarized in Figure 4. The implications of applying this methodology to power grid designs at different technology nodes are presented in the next section.

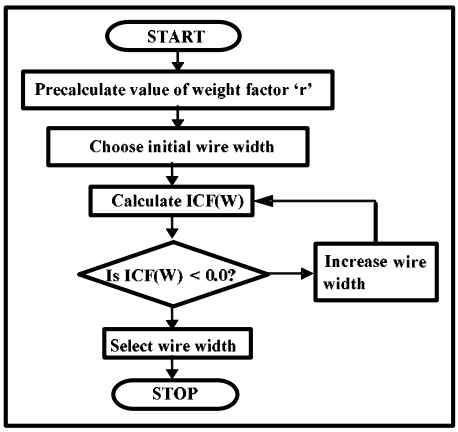

Figure 4: Flowchart showing methodology for evaluating optimal power grid wire width.

5. RESULTS AND DISCUSSIONS

Table 1 shows relevant numbers pertaining to nanometer scale high performance microprocessor designs as prescribed by the ITRS. In general, half of the external pins on a chip are used to connect the power supply. Accordingly, the entire chip area is divided into a number of small locally regular grids (Figure 1(c).), each fed at its four corners by a set of C4 bumps which connect them to the off-chip power supply. This simple design does not cause any loss of generality, as each individual grid can be designed as per local requirements while still maintaining a locally regular grid-like structure.

Table 1: ITRS (2003) prescribed technology requirements used for the power distribution network design.

Tech Node	90 nm	65 nm	45 nm
Pins per chip	3000	4000	4009
Chip Size (mm^2)	310	310	310
Local P/G Grid Area (mm^2)	.413	.310	.309
Square P/G Grid Size (µm)	640	560	560
NAND nominal gate delay (ps)	24	16	9.8

The wire width optimization methodology described above is applied to the design of a power grid at different technology nodes to demonstrate the effect of including on-chip grid inductance in the optimization methodology. For each grid a constant P (pitch between successive pairs of power/ground wires) of 25 µm and S (spacing between wires forming a power-ground pair) of 2µm is assumed, in order to preserve the "paired grid" topology (Figure 1(c)). The other grid dimensions are derived from the technology dependent figures shown in Table 1. The current rise/fall transition time (*dt*) for on-chip inductive noise is assumed to be half the nominal gate delay at each technology node (later in this section this assumption regarding *dt* is removed). The actual value of I_{peak} does not reflect anywhere in the results presented as the ratios cancel out that value (Equation 8). In addition to evaluating the weight factor 'r' as outlined in Section 4, it is scaled up by a factor of 2 to demonstrate the case where an increase in PSN is considered twice as expensive as a corresponding increase in area ratio.

Figure 5 plots ICF(W) against wire width (W) at different technology nodes. The intersection of these curves with the X-axis marks the point where there is no further improvement in total cost and the optimal wire width is found. The curves show the significant difference in optimal wire width when grid inductance is ignored in the power supply noise expression (Equation 2). Note that for the case *without* on-chip grid inductance, Equations 6 need to be re-evaluated by including only the package inductance. It is observed that with the inclusion of on-chip inductance, the optimal wire width decreases with technology scaling. This is expected because as switching time decreases with technology scaling, the contribution of inductance to power supply noise becomes greater.

It is observed that the optimal wire width is smaller than that obtained by ignoring on-chip inductance. At a smaller wire width the resistive voltage drop will be higher. However there are a few points to note here. Firstly, the wire width obtained by ignoring on-chip grid inductance is not a true optimal as the noise levels estimated using only grid resistance and package inductance are significantly lower. In nanometer scale technologies, the on-chip power grid inductance becomes a significant contributor to PSN and grid resistance does not remain the sole factor determining the optimal wire width. Also, the worst power supply noise occurs when the underlying circuit is switching and the power supply grid is subject to high levels of current as well as high frequencies. The significant frequency

[23] on the power supply grid is several tens of GHz in nanometer designs. At these high frequencies it is important to consider the ac resistance of the power grid along with the dc resistance.

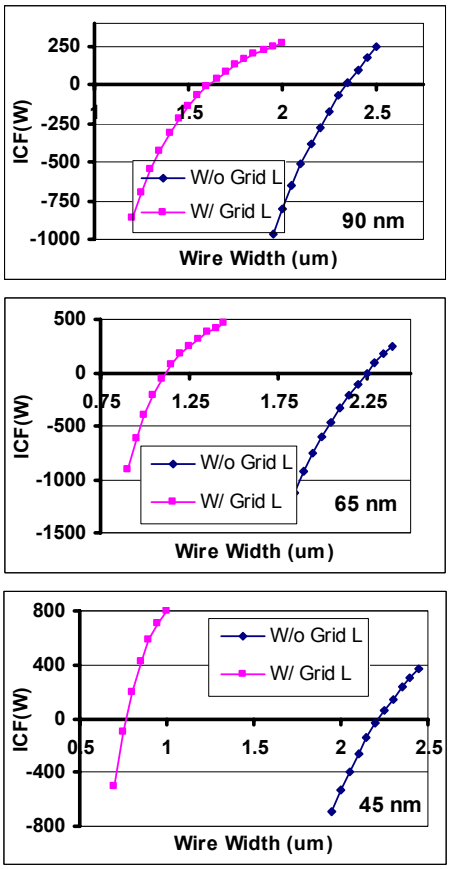

Figure 5: ICF(W) variation with wire width for illustrative power grid wire width optimization with and without on-chip grid inductance at different technology nodes.

Table 2 shows the resulting change in area ratio, resistance, on-chip grid inductance and worst case PSN with the wire width optimization methodology when on-chip grid inductance is included as compared to the case where it is ignored. Since we assigned higher weight to PSN (scaled up the factor 'r' by 2), the change in PSN is significantly lower than the reduction in area ratio. This is in spite of the fact that resistance increases because grid inductance is also a significant contributor to PSN. It is also observed that the increase in ac resistance (taking high frequency effects into account) as obtained by the field solver FastImp [24] (at the significant frequency corresponding to the rise/fall transition time at each technology node) is significantly lower than that in dc resistance.

In practical designs, on-chip decoupling capacitances (decaps) [8] are used to reduce the high frequency switching currents. Current rise/fall transition times (*dt*) would be larger depending upon the specific placement of decaps and the switching activity in the circuit underlying the grid. Figure 6 shows the optimal wire width (the case ignoring on-chip grid inductance is shown for comparison) when *dt* is varied to demonstrate the effect of decaps, for different technology nodes. As the transition time increases (or transient frequency decreases) power supply noise due to inductance decreases accordingly and the optimal wire width is obtained at a higher value. As expected, these results also show that the difference in optimal wire width when on-chip grid inductance is included becomes larger as technology scales and frequencies increase (transition time decreases).

Table 2: Variation in critical parameters of the power grid: area ratio (A), d.c. resistance (Rdc), a.c. resistance (Rac), inductance (L) and worst case power supply noise (PSN). Values shown are percentage increase in these parameters when wire width is optimized considering on-chip power grid inductance as compared to the case when wire width is optimized ignoring on-chip power grid inductance. Rac and L obtained from FastImp [24].

Tech Node	A (% change)	Rdc (% change)	Rac (% change)	L (% change)	PSN (% change)
90 nm	-30%	42%	25%	8%	11%
65 nm	-50%	100%	49%	15%	20%
45 nm	-64%	181%	84%	21%	31%

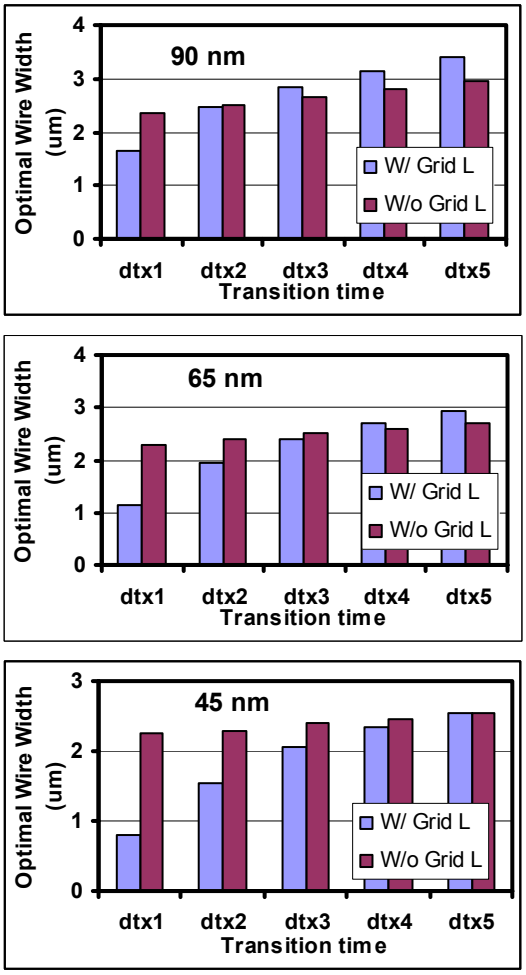

Figure 6: Optimal power grid wire width (with and without on-chip grid inductance) for switching current rise/fall transition time different multiples (1, 2, 3, 4 and 5) of half the nominal gate switching delay (*dt*=gate-delay/2) at different technology nodes.

6. SUMMARY

A compact methodology has been described for the early power distribution network design for nanometer scale integrated circuits. Using this methodology, the cost associated with

a chip's power distribution network has been evaluated from a consideration of the resistive and inductive voltage drops on the grid and the fraction of the metallization area it occupies. This analysis has been used to present quantitative measures for the importance of considering on-chip grid inductance while designing the power distribution network on a chip. The inclusion of on-chip power grid inductive noise in designing an illustrative power supply grid is shown to reduce the fraction of metallization area it occupies by 30% at the 90 nm technology node and by 64% at the 45 nm technology node. This result stems from the fact that including on-chip inductance leads to an optimal grid design at a lower wire width as compared to a design that ignores on-chip inductance. With the increasing switching frequencies of on-chip devices as technology scales, it is shown that including on-chip power grid inductance in the early power grid design process not only provides more accurate noise estimation but also leads to larger improvements in wiring resource utilization of nanometer scale VLSI circuits.

Acknowledgements

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