Simulation of Interconnect Inductive Impact in the Presence of Process Variations in 90 nm and Beyond

Xiaoning Qi, *Senior Member, IEEE*, Alex Gyure, Yansheng Luo, Sam C. Lo, Mahmoud Shahram, *Senior Member, IEEE*, and Kishore Singhal, *Fellow, IEEE*

***Abstract*—The on-chip inductive impact on signal integrity has been a problem for designs in deep-submicrometer technologies. The inductive impact increases the clock skew, max timing, and noise of bus signals. In this letter, circuit simulations using silicon-validated macromodels show that there is a significant inductive impact on the signal max timing ($\sim$ 10% pushout versus RC delay) and noise ($\sim 2 \times RC$ noise). In nanometer technologies, process variations have become a concern. Results show that device and interconnect process variations add $\sim$ 3% to the *RLC* max-timing impact. However, their impact on the *RLC* signal noise is not appreciable. Finally, inductive impact in 65- and 45-nm technologies is investigated, which indicates that the inductance impact will not diminish as technology scales.**

***Index Terms*—Inductance, interconnections, very-high-frequency (VHF) integrated circuits.**

I. Introduction

THE INDUCTIVE impact on timing and noise of ultrahigh-frequency designs has been a challenge for technologies below 0.25 μm [1]–[7]. The inductance impact increases the clock skew, max timing of signals, and noise injection on the signals and power/ground grids. In nanometer technologies, interconnects become more resistive due to smaller wire width and more coupling capacitive due to smaller wire spaces, which may potentially alleviate the inductance effects. On the other hand, faster signal rise-and-fall times inevitably increase di/dt and inductive effects. Evaluation of the inductive impact in the 90-nm technology and beyond is necessary for proper understanding of signal integrity for high-performance circuits. In addition, process variations become a major issue for nanometer technologies [8]–[10]. Intra-/inter die device and interconnect variations add another dimension to signal-timing uncertainties, and it is worth investigating the inductive impact on the signal integrity in the presence of process variations. In this letter, circuit simulations using silicon-validated *RLC* extraction and circuit macromodels show that the inductive impact on signal timing is not alleviated relative to the 130-nm technology, and that the impact on the noise becomes larger. Inductance-impact analysis with process variations reveals that inductive impact is larger than the process-variation impact. Finally, the inductive impact in 65- and 45-nm technologies was studied based on the 2004 International Technology Roadmap for Semiconductors (ITRS) [11]. Results predict that the inductance impact continues to be significant as technology scales.

Manuscript recieved April 20, 2006. The review of this letter was arranged by Editor S. Kawamura.

The authors are with the Direct Silicon Access Laboratory, Synopsys Inc., Mountain View, CA 94043 USA (e-mail: xiaoning.qi@synopsys.com; xqi@stanfordalumni.org).

Digital Object Identifier 10.1109/LED.2006.879039

II. Simulation for Inductive Impacts and Process Variations

To have an accurate simulation of the inductive impact, a test chip was designed and manufactured in a 90-nm process technology to calibrate *RLC* extraction circuit models [12], [13]. The circuit *RLC* parameters were extracted using RAPHAEL. Multiple π models are used to model long wires, which include resistance, capacitance, coupling capacitance, and self- and mutual inductances between all wires. To model proximity effects, simulation windows are bounded by four power bays in the same metal layer and above/below metal layers. HSPICE simulation results show that simulated S-parameters and measured S-parameters match very well up to 20 GHz (errors $< 5\%$) [13], which validates the circuit macromodels and extraction methodology. These accurate models make it possible to analyze the inductive impact on timing and noise for interconnects in the 90-nm technology.

To simulate the inductive max timing and noise impact, consider two parallel 15-bit buses, one in M6 and one in M4, in a 90-nm technology. Every three signal wires share two power/ground wires (Fig. 1). Such bus structures are typical in high-performance CPU designs. HSPICE is used in all circuit simulations to include any nonlinear effect from the driver/load devices. To simulate the worst case inductive impact on the max-timing stage delay, the two nearest signals next to the victim (in M6) switch against the victim to maximize the Miller effect of the wire capacitance, while the rest of the signals switch with the victim to maximize inductive impact. This scenario will maximize the stage delay due to the inductive impact against the worst case RC simulation. In terms of noise simulation, the victim wire is kept quiet, and all other switching activities are the same as in the delay simulation. All delay and noise measurements are taken at the far end (FE) of the victim wire. The circuit is simulated both with inductance (*RLC*) and

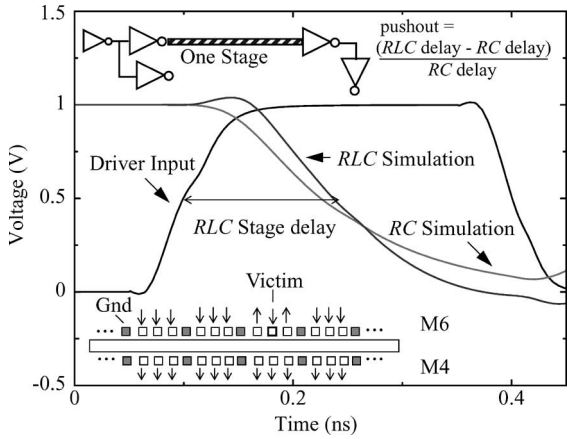

Fig. 1. All wires are 1500-μm long and modeled by six π models. Drivers are prebuffered and sized to be 20X in M6 and 16X in M4 in order to have a rise/fall time of $\sim$ 50 ps at the driver inputs and $\sim$ 100 ps at the receiver inputs (20%–80% VDD). The wire pitch is 0.6 μm, and the metal thickness is 0.33 μm. The resistance, coupling capacitance, and ground capacitance of the victim wire are 0.25 Ω/μm, 0.07 fF/μm, and 0.1 fF/μm, respectively. The *RLC* stage delay is 137 ps while the *RC* stage delay is 125 ps — an inductive pushout of 9.6%. The pushouts in multiple stages converge to 8% due to the signal overshoots from the *RLC* wires.

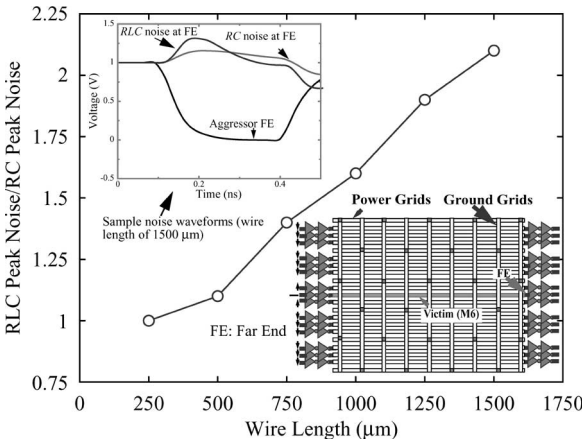

Fig. 2. Ratio of *RLC* peak noise over RC peak noise is greater than one for wires longer than 500 μm in a 90-nm technology. Ignoring inductance in the noise simulation underestimates the signal noise. The bus structure consists of two 15-bit buses in M6 and M4, and the victim is in M6. For clarity, only signal lines in M6 with power grid in M7–M8 are plotted. The wire pitch is 0.6 μm, and the metal thickness is 0.33 μm. The resistance, coupling capacitance, and ground capacitance of the victim wire are 0.25 Ω/μm, 0.07 fF/μm, and 0.1 fF/μm, respectively. The input rise time is 48 ps (20%–80% VDD).

without inductance (RC). Results show that *RLC* 50%-delay has 9.6% pushout compared to RC 50%-delay (Fig. 1). Due to inductive impact, the victim signal starts to fall later than it does in RC, but has relatively faster fall time. To have accurate max-timing estimation, this inductive pushout must be taken into account in timing analysis. Noise simulations show that *RLC* noise is 2.1$\times$ RC-noise simulation. The larger glitch and ringing on the signal may cause a circuit functional failure, especially in dynamic circuits. In addition, inductive noise is a function of the wire length. Any wires longer than 500 μm have significant *RLC* noise (Fig. 2). In order to avoid the inductive impact, analysis should be done in the early stages of design to create inductance-aware wire classes or to factor their impact into the design.

Process variations become increasingly important in the 90-nm technology and beyond. Table I shows the impacts from device and interconnect variations on stage delay and noise. Inductance is a weak function of geometry as can be seen from the approximate formulas for wire self- and mutual inductances

$$L_{\text{self}} = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{(w+t)} + \frac{1}{2}\right] \quad M = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{d} - 1\right]$$

where l, w, t, and d are the wire length, width, thickness, and wire center-to-center distance, respectively. μ_0 is the permeability. For a 1000-μm-long wire with width and thickness equal to 1 μm ($L_{\text{self}} = 1.5$ nH), the inductance variation is 0.1 nH for a 1-μm-width (2X) variation [14]. If there is a wire and a ground return in parallel with the lengths of a 1000-μm (width and thickness of 1 μm), the wire-loop inductance varies 0.2 nH per 1-μm-width change. However, the inductance impact can become larger or alleviated by process variations (Table I). It is worth pointing out that the increased current driving force (larger di/dt) from shorter channels does not make the inductive effect more severe, because capacitive effects dominate the max-timing stage delay under this switching condition (Miller effect). Similarly, interconnect thickness variations do not change the inductance impact much, and process variations do not add more to *RLC* noise.

III. Inductive Impacts in Future Technologies

Having followed a similar methodology to that used in [3], which predicted the inductive effect down to the 130-nm-technology node, simulations were performed for sub-130-nm technologies. Fig. 3(a) shows the RC and LC delay estimation of a coplanar clock wire in M8 for the 90-nm node. For wire lengths from 2.5 (Len1) to 9.5 mm (Len2), it illustrates that RC delay estimation is faster than the speed of light, which is not physical. It simply means that inductance needs to be included in the wire model, otherwise, the wire delay will be underestimated. For wire lengths smaller than 2.5 mm, gate delay dominates. But inductance is needed for bus-noise analysis for any wire length longer than 500 μm. Based on ITRS'04, *RLC* extractions were performed to calculate Len1 and Len2 for sub-130-nm technologies. Fig. 3(b) plots Len1 and Len2, which predict the wire range where inductance effect is important. The ranges for future technologies indicate that inductive impact for practical circuits will not diminish as technology scales.

IV. Conclusion

In this letter, circuit simulations, using silicon-validated circuit models, reveal significant inductive impact on clock, bus signal max timing ($\sim$ 10% pushout) and noise ($\sim 2 \times RC$ noise). Collective impact of inductance and process variations is about 6% to 13% for max timing, but does not show much noise difference compared to *RLC* simulations. The analysis based on the ITRS'04 shows that inductive impact on

TABLE I
IMPACTS FROM PROCESS VARIATIONS AND INDUCTANCE IMPACT IN THE PRESENCE OF PROCESS VARIATIONS*

	Device Variations		Interconnect Variations
Worst case delay and noise vs. RC Nominal	Channel Length (-10% to +10%) Nominal: 0.1 µm	Threshold Voltage (-10% to +10%) Nominal VTH0: 0.2v	Metal Thickness (-10% to +10%) Nominal M6 Thickness: 0.33 µm
RC Delay Pushout	-6.0% to 4.8%	-2.9% to 3.4%	1.6% to 0.8%
RC Noise	1.1x to 1x	1x	0.93x to 1.1x
RLC Delay Pushout	5.6% to 12.0%	6.4% to 12.8%	11.2% to 8.8%
RLC Noise	2.3x - 2x	2.1x	1.93x - 2.2x

*The circuit setup is the same as that in Fig. 2. The *RLC* pushout without process variations is 9.6%.

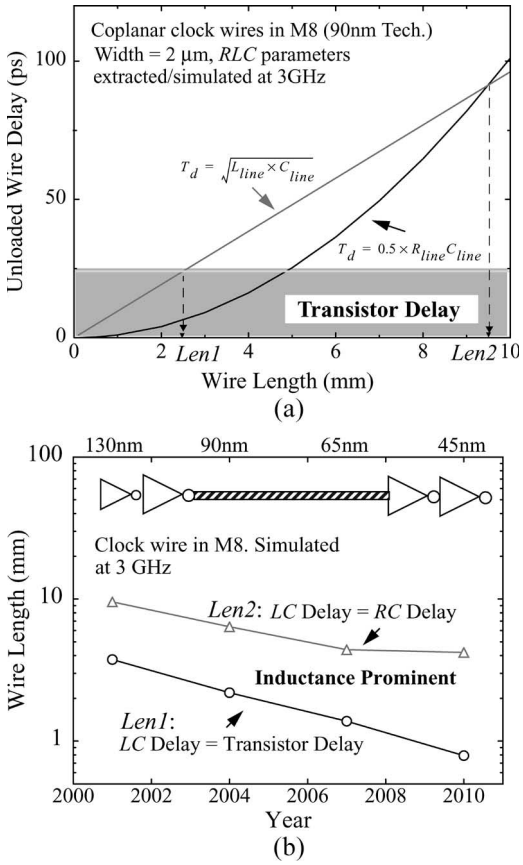

Fig. 3. (a) For the 90-nm technology in the range of 2.5- to 9.5-mm wire length, *RC* delay estimations underestimate the wire delays. The wire width and spacing are 2 μm. The metal thickness is 0.8 μm. (b) For each technology node, any coplanar clock wire of length below the Len2 line and above the Len1 line will see the inductance impact on delays (i.e., delay is underestimated if the inductance is not included in the timing analysis). The wire pitches and widths are 2 μm. The gate switching time is based on the ITRS'04 (e.g., 16.23 ps in 65-nm technology).

interconnect delay will not be alleviated in the 65- and 45-nm technologies. High-performance designs need to take measures to minimize the impact effectively [5], [15].

REFERENCES

[1] A. Deutsch, P. W. Coteus, G. V. Kopcsay, H. H. Smith, C. W. Surovic, B. L. Krauter, D. C. Edelstein, and P. J. Restle, "On-chip wiring design challenges for gigahertz operation," *Proc. IEEE*, vol. 89, no. 4, pp. 529–555, Apr. 2001.

[2] P. J. Restle, "High speed interconnects: A designers perspective," in *ICCAD Tutorial: Interconnect High Speed Des.: Problems, Methodologies and Tools*, Nov. 1998.

[3] X. Qi, B. Kleveland, Z. Yu, S. S. Wong, R. W. Dutton, and T. Young, "On-chip inductance modeling of VLSI interconnects," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2000, p. 172.

[4] B. Krauter, S. Mehrotra, and V. Chandranmouli, "Including inductive effects in Interconnect timing analysis," in *Proc. IEEE Custom Integr. Circuits Conf.*, 1999, pp. 445–452.

[5] B. Kleveland, X. Qi, L. Madden, T. Furusawa, R. W. Dutton, M. A. Horowitz, and S. S. Wong, "High-frequency characterization of on-chip digital interconnects," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 716–725, Jun. 2002.

[6] Y. Massoud, J. Kawa, D. MacMillen, and J. White, "Modeling and analysis of differential signaling for minimizing inductive cross-talk," in *Proc. Des. Autom. Conf.*, Jun. 2001, pp. 804–809.

[7] P. Mahoney, E. Fetzer, B. Doyle, and S. Naffziger, "Clock distribution on a dual-core, multi-threaded Itanium-family process," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2005, pp. 292–293.

[8] K. Bowman, S. Duvall, and J. Meindl, "Impact of die-to-die and within-die parameter fluctuations on the maximum clock frequency distribution for gigascale integration," *IEEE J. Solid-State Circuits*, vol. 37, no. 2, pp. 183–190, Feb. 2002.

[9] P. Zuchowski, P. Habitz, J. Hayes, and J. Oppold, "Process and environmental variation impacts on ASIC timing," in *Proc. ICCAD Tech. Dig.*, Nov. 2004, pp. 336–342.

[10] S. Samaan, "The impact of device parameter variations on the frequency and performance of VLSI chips," in *Proc. ICCAD Tech. Dig.*, Nov. 2004, pp. 343–346.

[11] Semiconductor Industry Association, *International Technology Roadmap for Semiconductors 2004 (ITRS'04)*. [Online]. Available: http://public.itrs.net

[12] H. H. Skilling, *Fundamentals of Electric Waves*. New York: Wiley, 1948.

[13] X. Qi, A. Gyure, Y. Luo, S. Lo, M. Shahram, and K. Singhal, "Measurement and simulation of interconnect inductance in 90 nm and beyond," in *Proc. IEEE Int. Conf. Simul. Semicond. Process. Devices*, Sep. 2005, pp. 111–114.

[14] X. Qi, S. C. Lo, Y. Luo, A. Gyure, M. Shahram, and K. Singhal, "Simulation and analysis of inductive impact on VLSI interconnects in the presence of process variations," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2005, pp. 309–312.

[15] B. J. Benschneider, S. Park, R. Allmon, W. Anderson, M. Arneborn, J. Cho, C. Choi, J. Clouser, S. Han, R. Hokinson, G. Hwang, J. Kim, J. Krause, J. Kwack, S. Meier, S. Thierauf, and C. Zhou, "A 1- GHz alpha microprocessor," in *Proc. IEEE ISSCC Tech. Dig.*, 2000, pp. 86–87.