Line Inductance Extraction and Modeling in a Real Chip With Power Grid

Bendik Kleveland, Xiaoning Qi, Liam Madden[1], Robert W. Dutton, and S. Simon Wong

Center for Integrated Systems, Stanford University, Stanford, CA 94305, USA

[1]MIPS Technologies Inc., Mountain View, CA 94043, USA

Abstract

A realistic power grid and pseudo-random signal lines connected to on-chip drivers are included for accurate extraction of the parasitic inductance in a 5-metal layer 0.25–µm CMOS technology. A new ring oscillator for the extraction of signal delay and characteristic impedance is demonstrated. The increase of signal delay due to mutual inductance of clock lines is measured directly with *S*-parameter characterization techniques.

Introduction

The effects of on-chip parasitic line inductance have recently been observed in high-speed microprocessors [1]. Several time-domain techniques have been used to characterize long interconnects and excellent match with simulations has been reported [2]-[3]. Due to the continuous scaling of the gate delay and therefore faster signal rise and fall times, it will be necessary to incorporate the inductance in the modeling of progressively shorter lines. In this paper, various test structures for accurate extraction of line inductance are described.

Methodology

Conventional, isolated inductance test structures are illustrated in Fig. 1. Underneath the signal line, other lines are included to mimic the environment on a chip. These lines are usually either grounded (Fig. 1(a)) or left floating (Fig. 1(b)). Fig. 2 shows a section of the proposed test structure fabricated in a 0.25–µm CMOS technology with five metal layers. In metal levels M4 and M5 there are several test lines in an orthogonal power grid. In addition, a pseudo-random set of signal lines are inserted in M3 and M4. M1 and M2 are used for connecting the random lines to on-chip drivers [3].

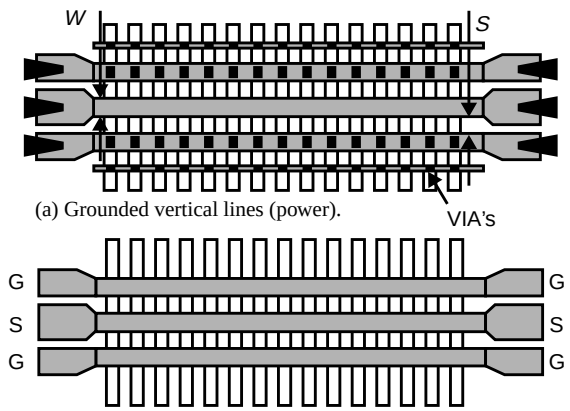


Fig. 1. Conventional inductance test structures.

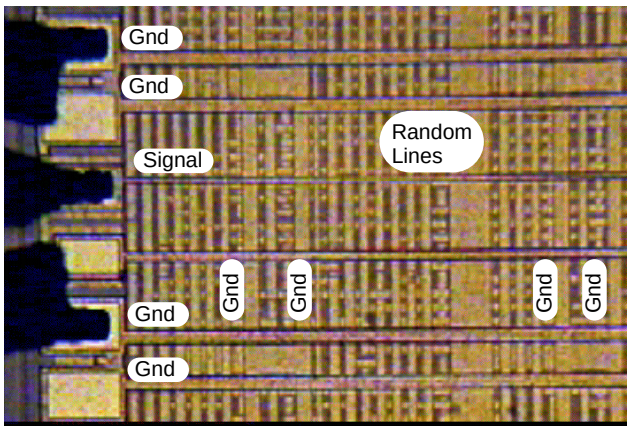


Fig. 2. Section of proposed real chip test structures.

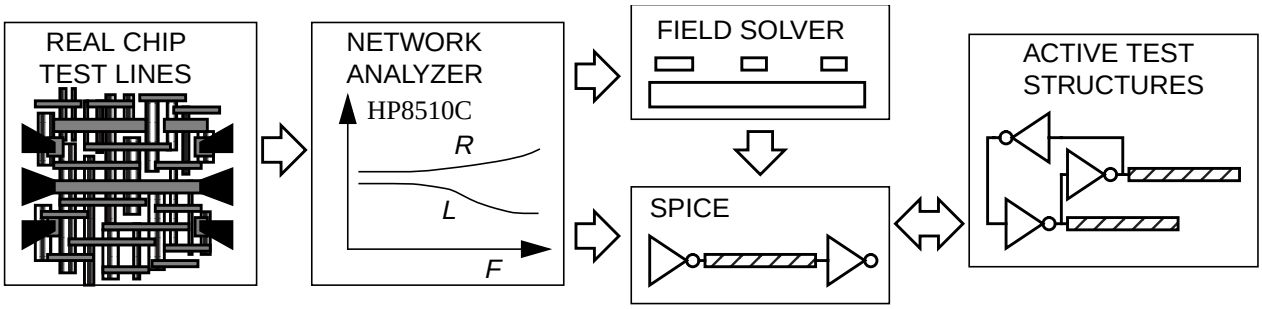


Fig. 3. Inductance characterization, modeling and simulation flow chart.

0-7803-5413-3/99/$10.00 (c) 1999 IEEE

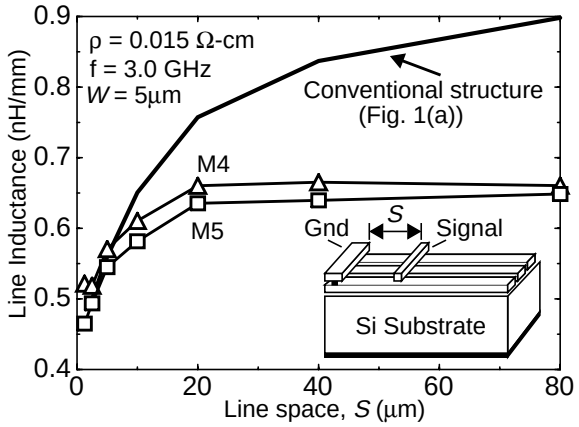


Fig. 4. Inductance vs. space.

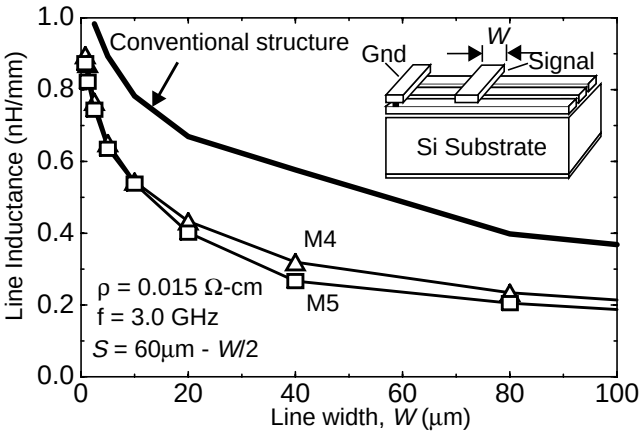


Fig. 5. Inductance vs. line width.

The *R,L,C,G* matrix is extracted from *S*-parameters and compared with field solver solutions (Fig. 3). The SPICE models are used for circuit simulation and correlation with measurements.

Grid Test Structures

The inductance of 4-mm long wires versus spacing to the power grid is shown in Fig. 4. The conventional test structure significantly overestimates the inductance for large spacing due to the absence of coupling to the random lines. However, for small spacing, it actually underestimates the inductance since all the current is forced to return in the neighboring power line. In Fig. 5, the inductance is shown for a wide range of widths to mimic the effect of multiple bus lines that switch in the same direction. The conventional structure overestimates the inductance due to the absence of random lines. Although the various test structures have similar inductance at low frequencies, the high frequency characteristics are different (Fig. 6). The coupling to a conductive substrate (0.015 Ω-cm) is shown to cause some of the frequency dependence (i.e. substrate skin effect). The majority of the discrepancy is due to the coupling to the random lines. Whether the drivers of the random lines are ON or OFF does not significantly affect the inductance because the capacitive couplings to the power grid and signal lines dominate. Assuming an effective characteristic transient frequency of 3 GHz, a simple analytical formula can be used to predict the inductance of lines in a power grid without the parallel random lines (Fig. 7).

Ring Oscillator Test Structures

Figs. 8 and 9 show SPICE simulations of an on-chip interconnect. When the inductance of a low-resistive line is ignored (Fig. 8), the full capacitive load is seen at the driver. The source and destination waveforms are therefore similar. When the inductance is included (Fig. 9), the inductance isolates a large portion of the line and load capacitance from the driver. Hence, the source waveform rises faster, but stays at a ledge while the wave travels to the destination and is reflected back. Notice that the destination waveforms are similar whether the inductance is included or not. Hence, a ring oscillator incorporating the delay line (Fig. 10 (a)) in between the stages would not be sensitive to the inductance. In Fig.

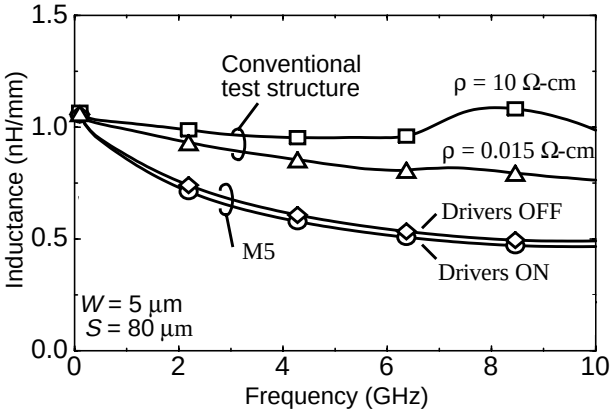


Fig. 6. Dependence of inductance on frequency.

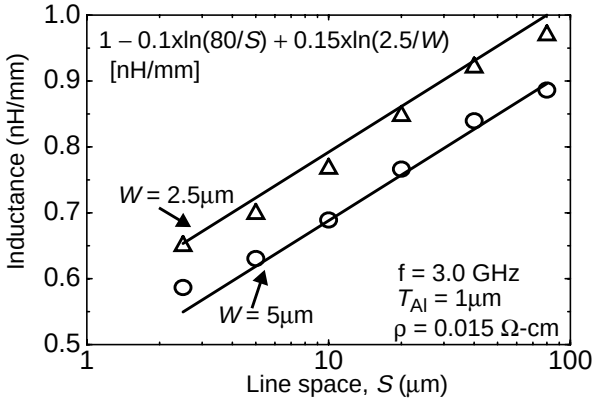


Fig. 7. Analytical model for inductance in power grid.

0-7803-5413-3/99/$10.00 (c) 1999 IEEE

10(b), the capacitive loading on the ring oscillator is similar to that of Fig. 10(a) but the inverters are connected to the source ends of the lines. The ledge voltage (Fig. 9), if sufficiently high, could trigger the next stage and cause a significant increase in the oscillation frequency.

Several three-stage ring oscillators were implemented. A reference ring oscillator was designed to have the same capacitive load but negligible inductive load. The oscillators were placed in a power grid. The frequency variation with Vdd shows that the reference ring oscillator has a slightly higher frequency which becomes more pronounced for larger Vdd when the gate delay is a smaller proportion of the cycle (Fig. 11 (a)). However, it is difficult to extract the inductance-induced delay from this set of measurements.

The frequency versus Vdd measurements as shown in Fig. 11 (b) confirm that at a critical Vdd, the ledge voltage at the source becomes sufficient to trigger the next stage causing the oscillator frequency to increase rapidly. Simulations adequately predict the line delay, the line impedance, and the transition to a higher oscillating frequency at sufficiently high Vdd. By combining the information from the two types of ring oscillators and the device characteristics, the line delay as well as the characteristic impedance can be

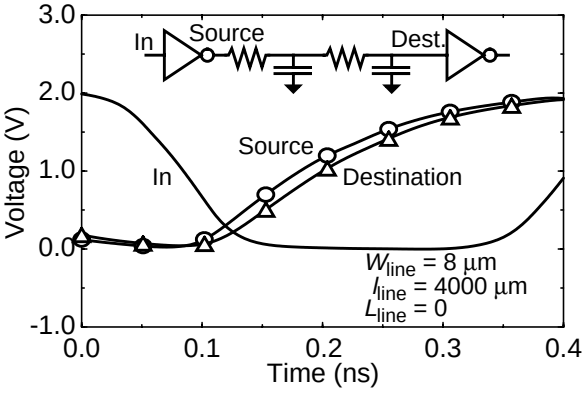


Fig. 8. Simulations of *RC* delay line.

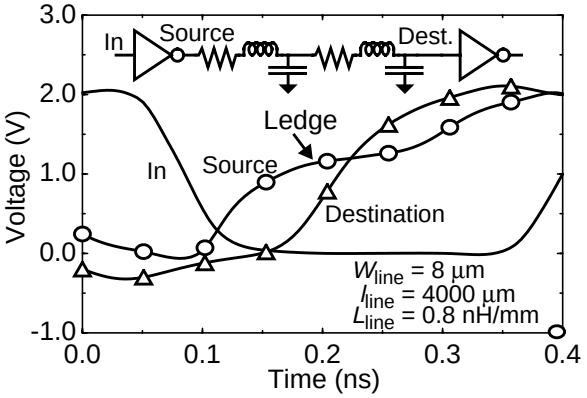


Fig. 9. Simulations of *RLC* delay line.

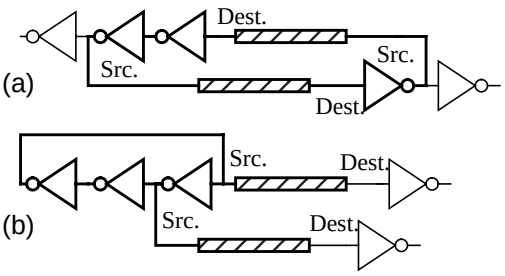
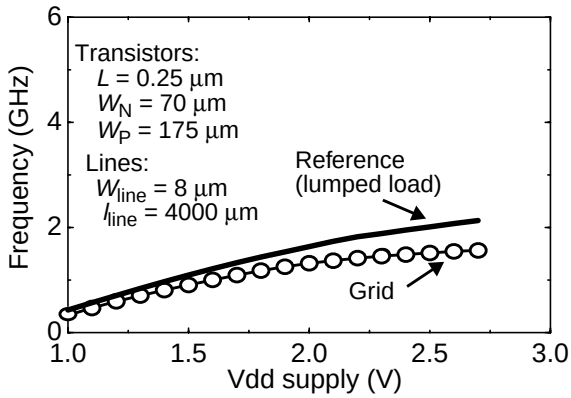
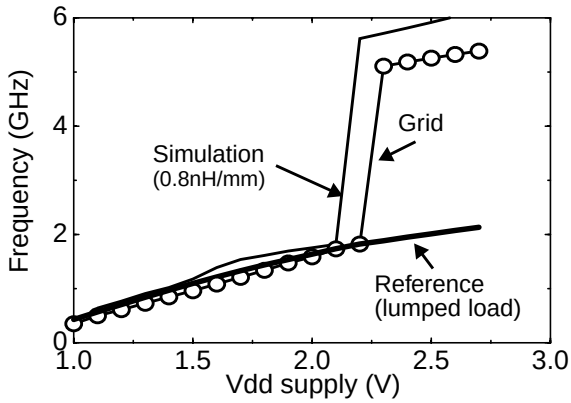


Fig. 10. Ring oscillators with connections at (a) destination and (b) source end of line.



(a) Connections at destination end of line



(b) Connections at source end of line

Fig. 11. Characteristics of ring oscillators.

extracted. The source connected ring oscillators also reveal that if this 4-mm interconnect is used for clock distribution, the ledge at approximately Vdd/2 can cause clock skew in excess of 100ps. Moreover, the existence of the transition to a high-frequency oscillation indicates that the driver has a lower impedance than the on-chip interconnect. This impedance mismatch will result in overshoot and ringing. If combined with on-chip dividers, the ring oscillator test structures enable the characterization of on-chip interconnects without the need of high-frequency probes. All the information is contained in the frequency vs. Vdd characteristics.

0-7803-5413-3/99/$10.00 (c) 1999 IEEE

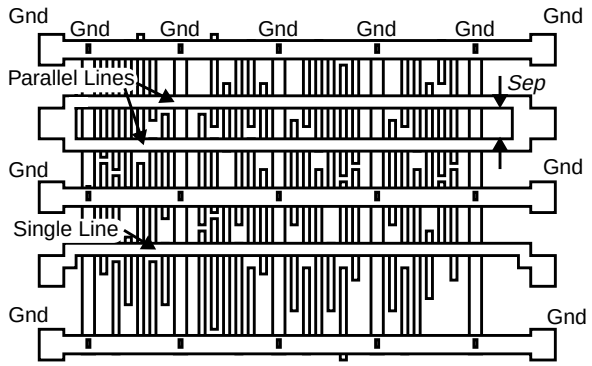


Fig. 12. Mutual inductance test structures.

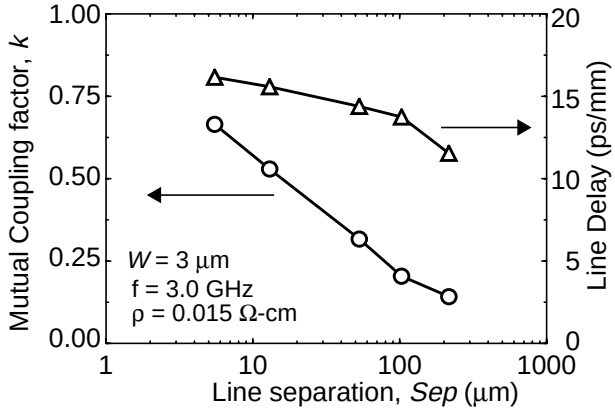


Fig. 13. Mutual line coupling results.

Clock Test Structures

In clock distribution, not only self inductance but also mutual inductance is a concern. The measurements are usually performed with a common ground terminal which is difficult for extracting low inductances [4]. Fig. 12 shows that by comparing the inductance measured on two lines driven in parallel with that of a single line, the increase in delay due to mutual coupling can be determined directly and the mutual inductance can be extracted (Fig. 13).

Fig. 13 shows that inductive coupling can not be ignored, even for large line separations. Clock shields should therefore be used. The importance of a low-impedance shield is illustrated by the three schemes in Fig. 14. The shield of CLK A is well connected to the power grid. The shield of CLK B is only connected at one end and that of CLK C is left floating to mimic neigboring tristate buses. A tremendous increase in inductance and loss due to coupling and resonance is observed in CLK B and CLK C, especially at high frequencies (Fig. 15).

Conclusion

The use of a realistic power grid and random lines enabled accurate extraction of parasitic line inductance. A new ring oscillator for extraction of signal delay and interconnect characteristics was demonstrated. *S*-parameter characterization enabled direct characterization of mutual inductance of relatively short lines.

Acknowledgments

We thank MIPS Technologies Inc. and the MARCO Interconnect Focus Center for research funding and National Semiconductors for chip fabrication. We also thank J. W. Prak and I. Young of Intel Corporation, and G. Gorton, V. Subramanian, R. T. Chang, N. Talwalkar, H. Sakai, and S. S. Mohan of Stanford University for discussions and assistance.

References

[1] P. J. Restle et al., "Measurement and modeling of on-chip transmission line effects in a 400 MHz microprocessor," IEEE Journal of solid-state circuits, vol. 33, no. 4, April 1998, pp. 662-665.

[2] A. Deutsch et al., "Functional high-speed characterization and modeling of a six-layer copper wiring structure and performance comparison with aluminum on-chip interconnections," IEDM 98, pp. 295-298.

[3] K. Soumyanath et al., "Accurate on-chip interconnect evaluation: a time domain technique," 1998 Symposium on VLSI circuits, pp. 116-117.

[4] S. S. Mohan et al., "Modeling and characterization of on-chip transformers," IEDM 98, pp. 531-534.

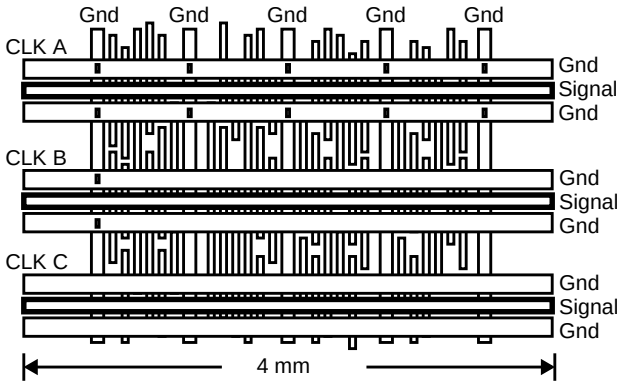


Fig. 14. Three different clock shields.

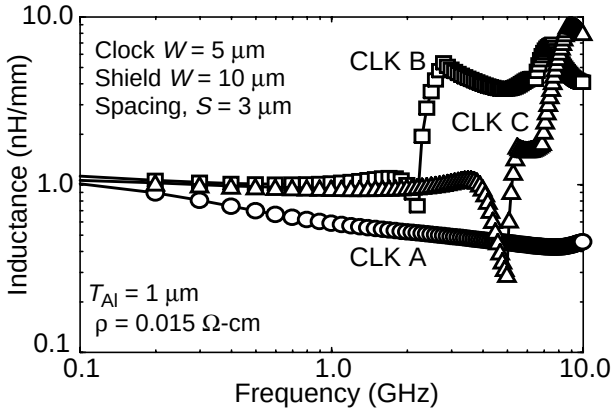


Fig. 15. Inductance vs. frequency for clock shields.

0-7803-5413-3/99/$10.00 (c) 1999 IEEE