Measurement and Characterization of Pattern Dependent Process Variations of Interconnect Resistance, Capacitance and Inductance in Nanometer Technologies

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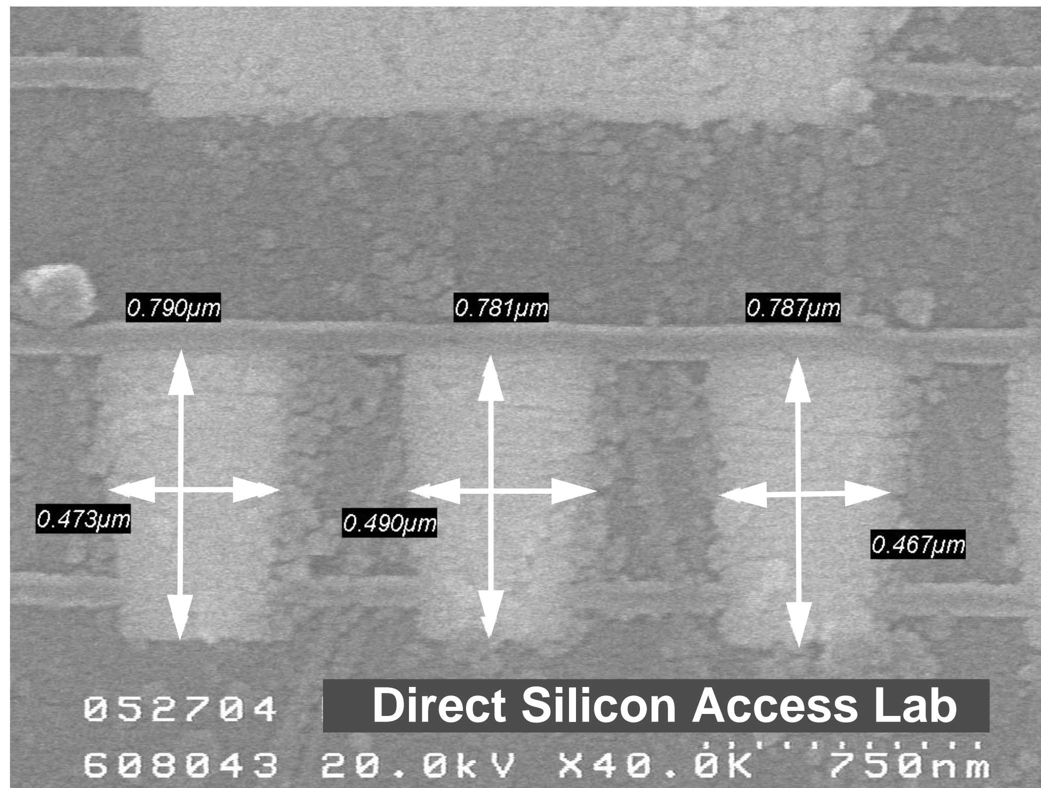
Outline

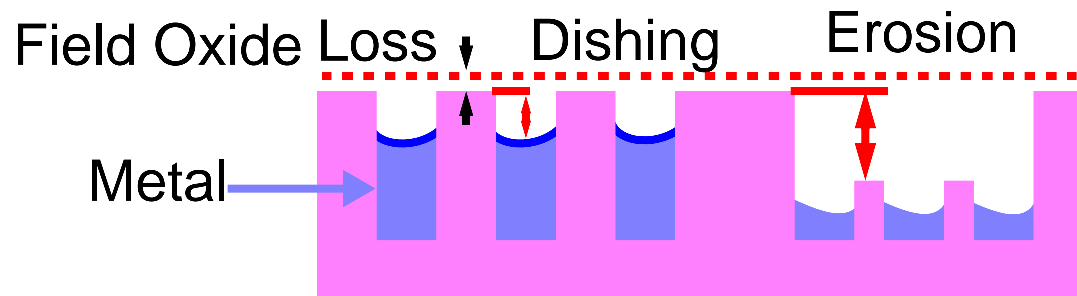
- Background and Motivation
- Pattern Dependent Process Variations - A test chip
- Modeling for Pattern Dependent *RC* Variations - A tech. file
- Summary

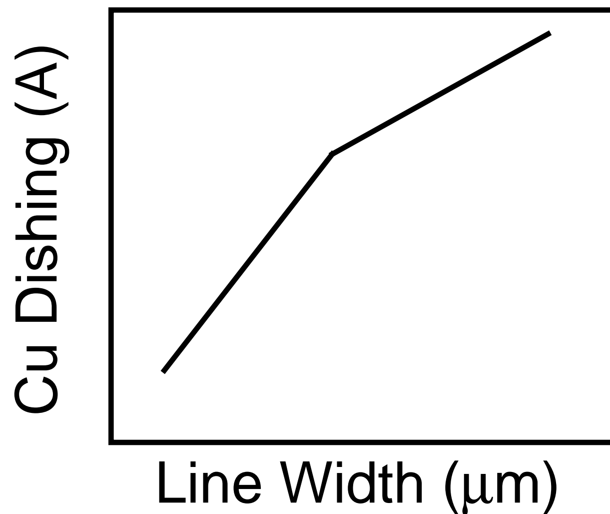
Background and Motivation

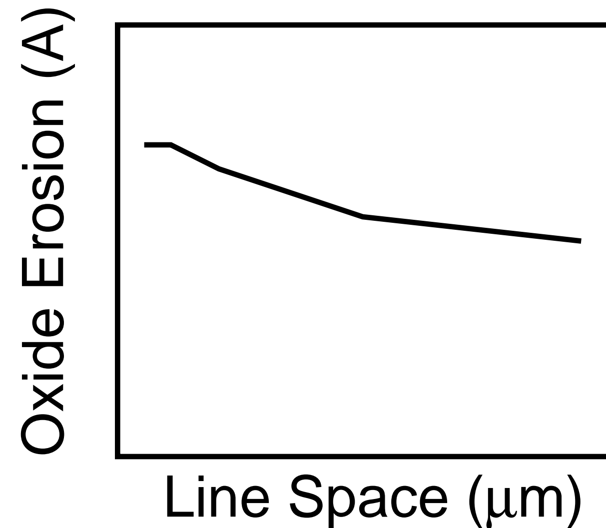
- **Process variations become an issue in 90 nm technology and beyond**



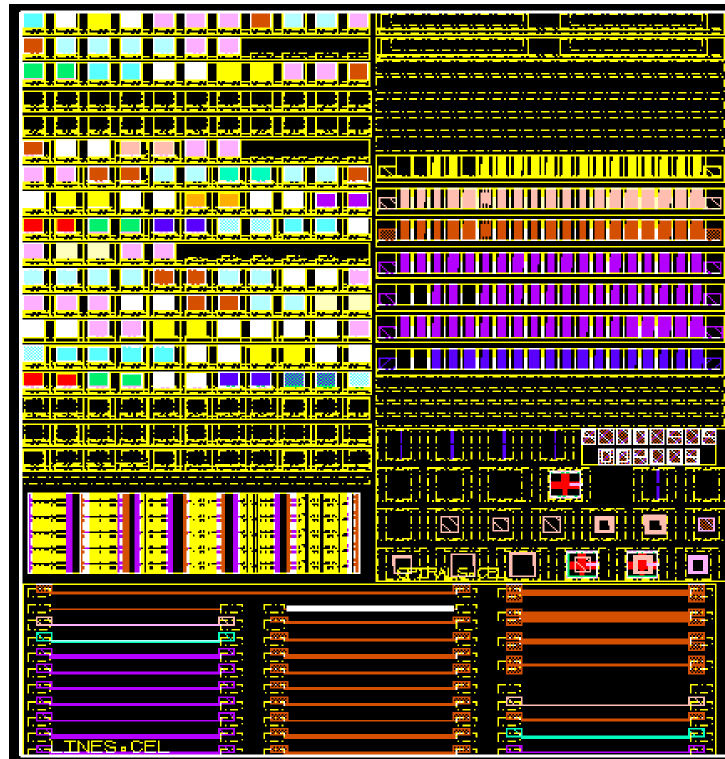
Pattern Dependencies in Cu CMP Processes







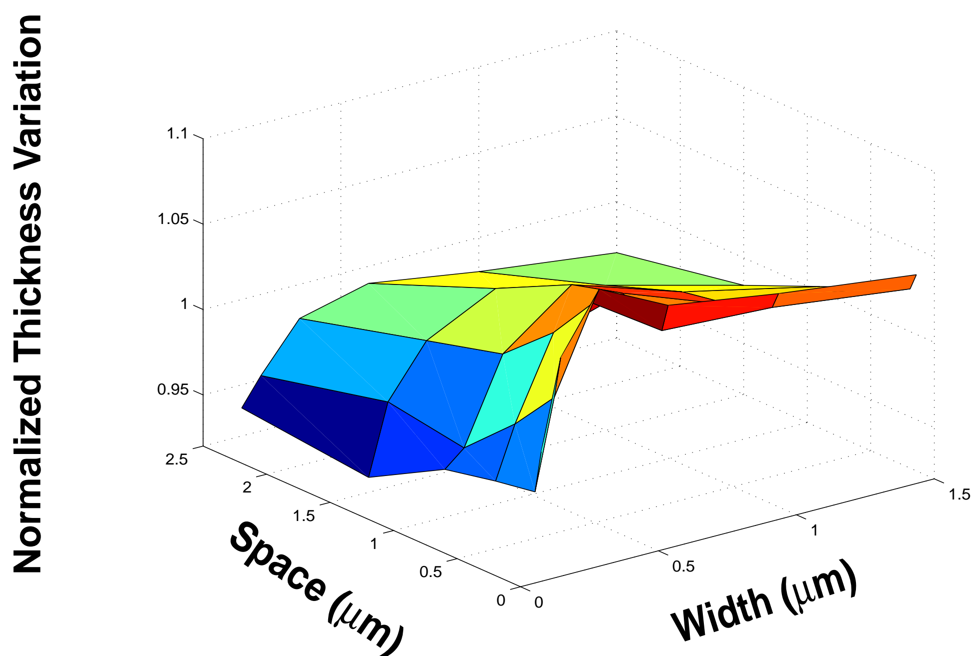
A Test Chip in 90 nm Technology



Measurement Methodology

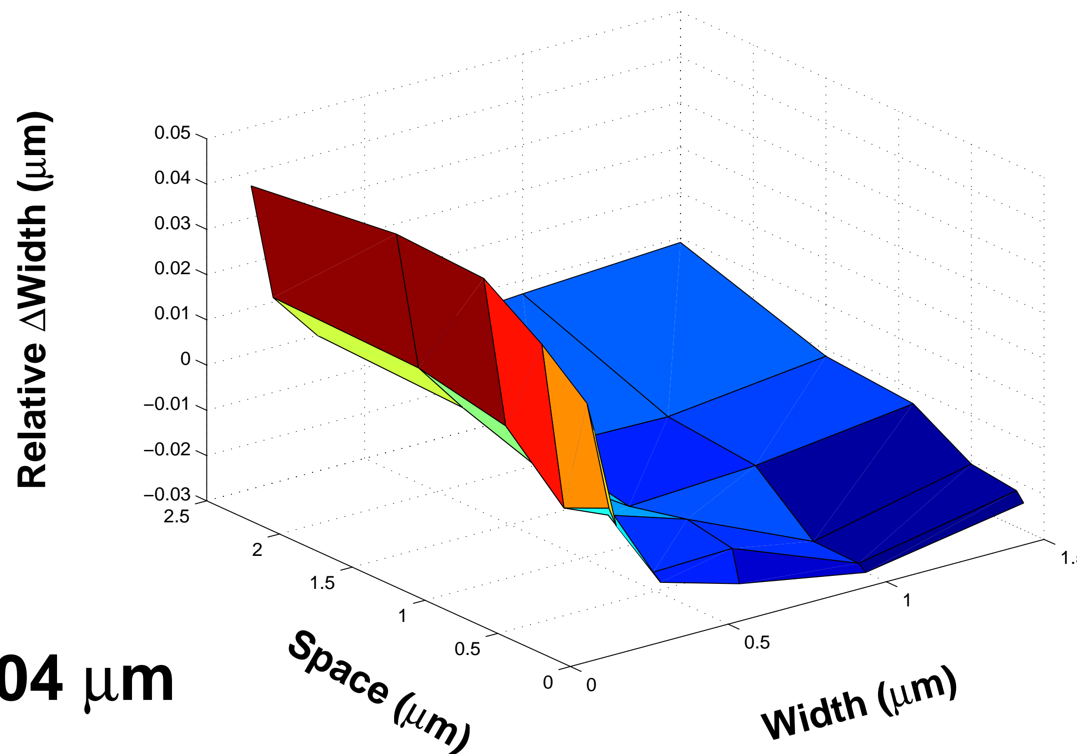
- Electrical characterization: I-V curve measurement and LCR meters.
- Physical characterization: SEM photos.
- Active device/transistors characterization: use on die I-V characteristics to fine tune SPICE models for ring oscillators in the same site.

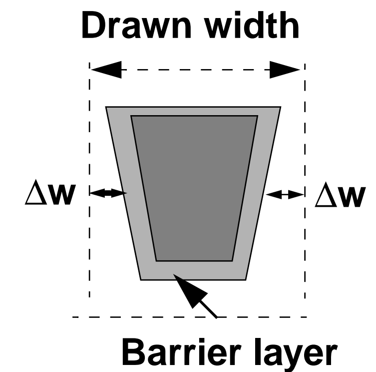
Normalized Average Metal Thickness Variations



Thicknesses are normalized to 50% wire density with about +/- 8% variations.

Width Variation Due to Etching Process

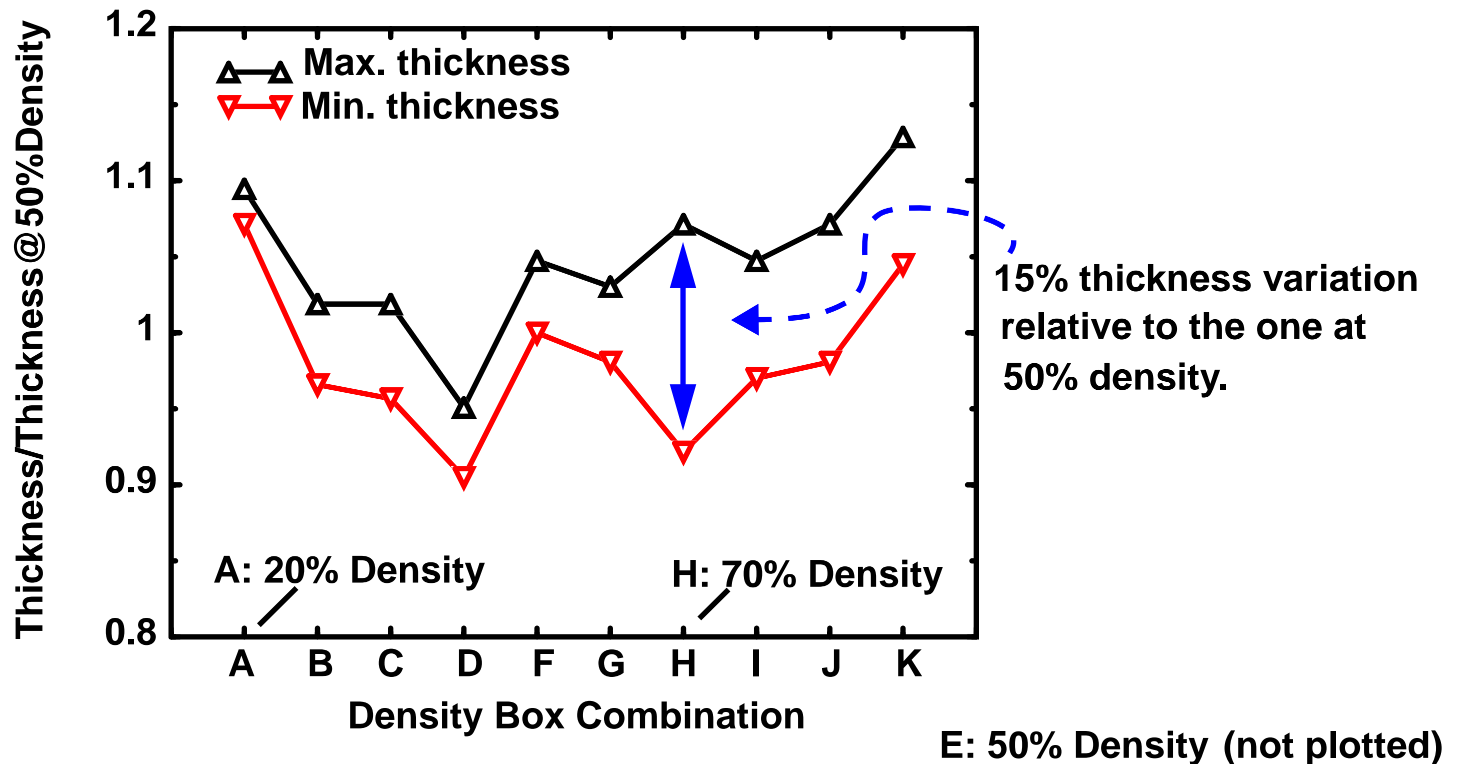




Variation:
-0.03 μm to 0.04 μm

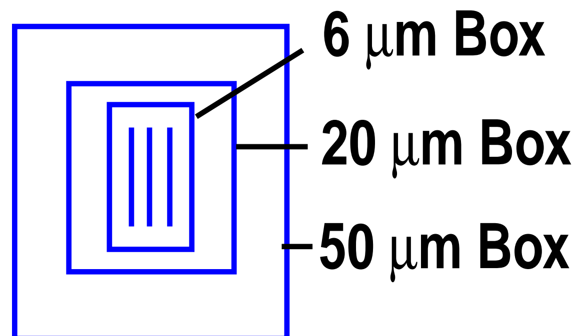
Relative ΔWidth = Δwidth - AVG(Δwidth)

Wire Thickness Variation vs. Wire Density

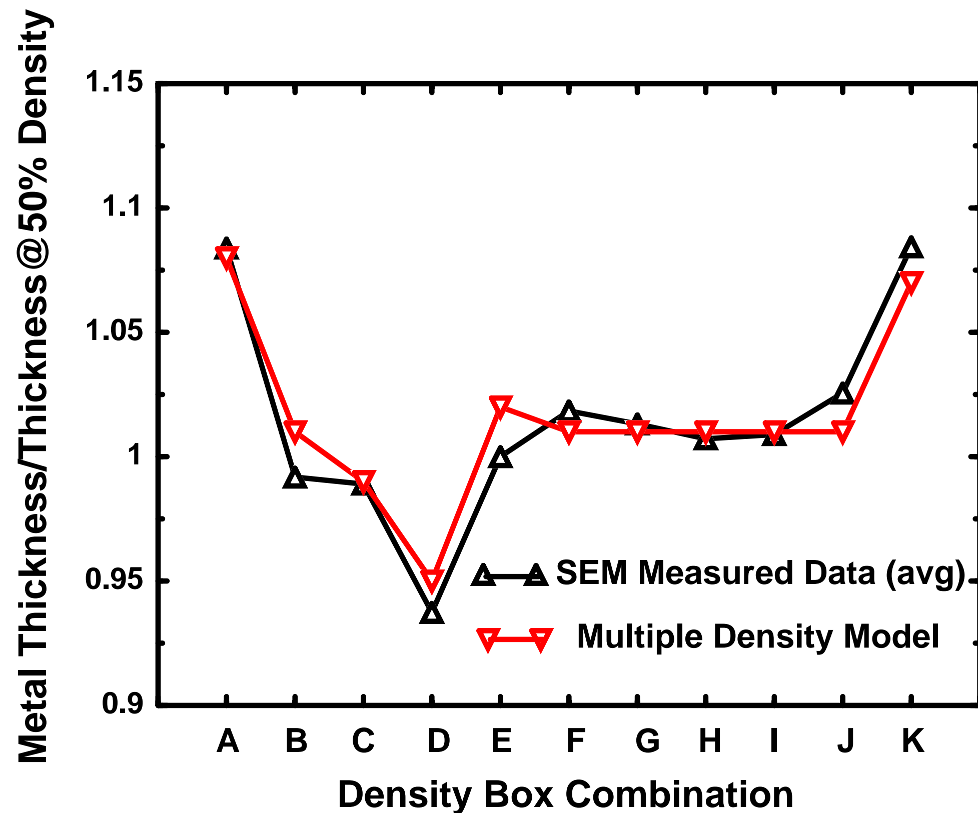


Three-Box Density Definitions

Density Combinations	A	B	C	D	E	F	G	H	I	J	K
6 µm Box Density (Weight Factor: 0.15)	0.2	0.2	0.2	0.2	0.5	0.5	0.5	0.7	0.6	0.7	0.7
20 µm Box Density (Wight Factor: 0.37)	0.2	0.6	0.3	0.7	0.5	0.3	0.7	0.7	0.3	0.7	0.3
50 µm Box Density (Weight Factor: 0.48)	0.2	0.25	0.6	0.7	0.5	0.6	0.3	0.7	0.6	0.3	0.2
Effective Density	0.2	0.37	0.43	0.63	0.5	0.47	0.48	0.7	0.49	0.51	0.31



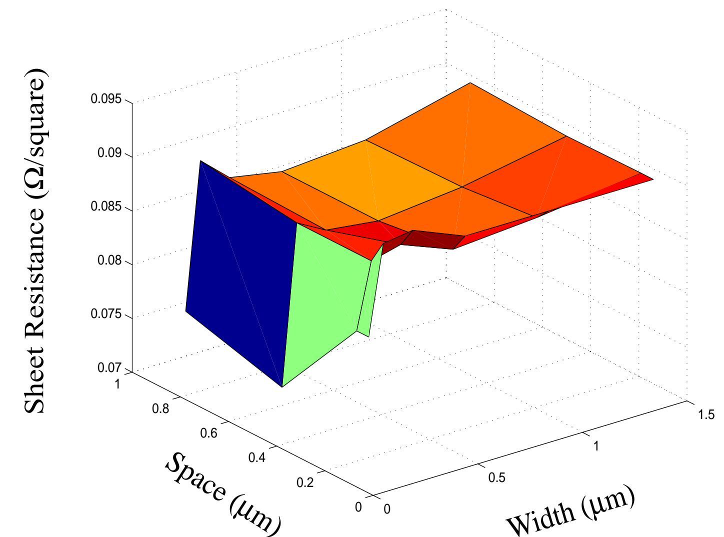
Three-Density Box Validation



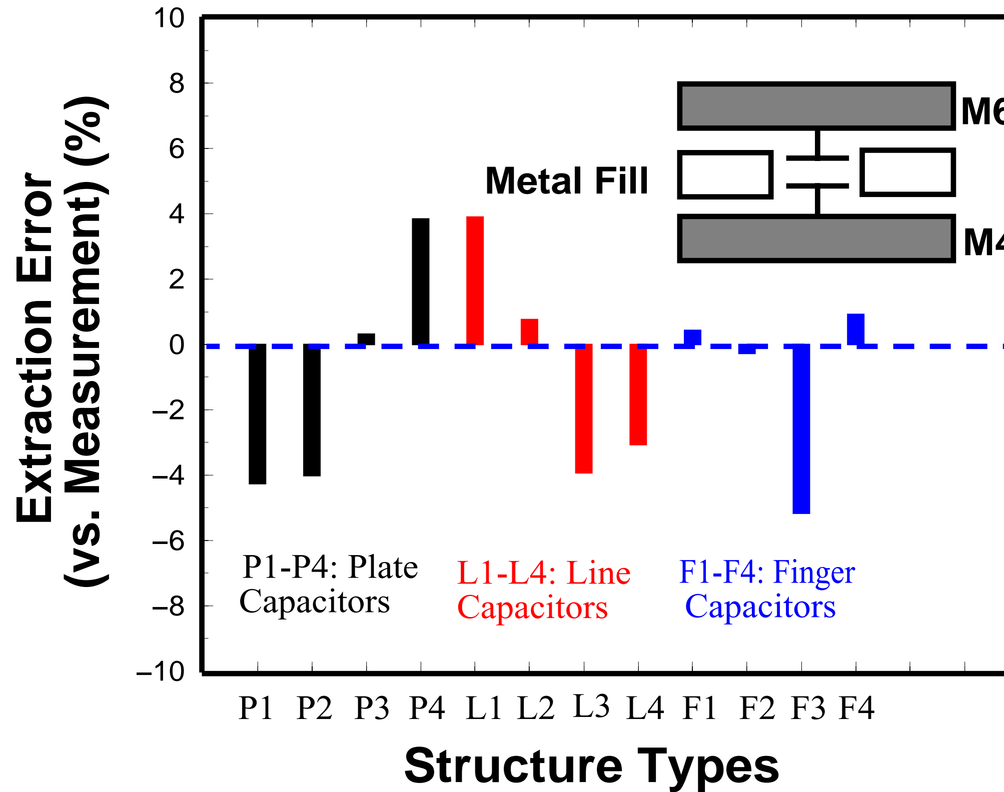
Normalized to 50% density data
Errors are within +/- 2%

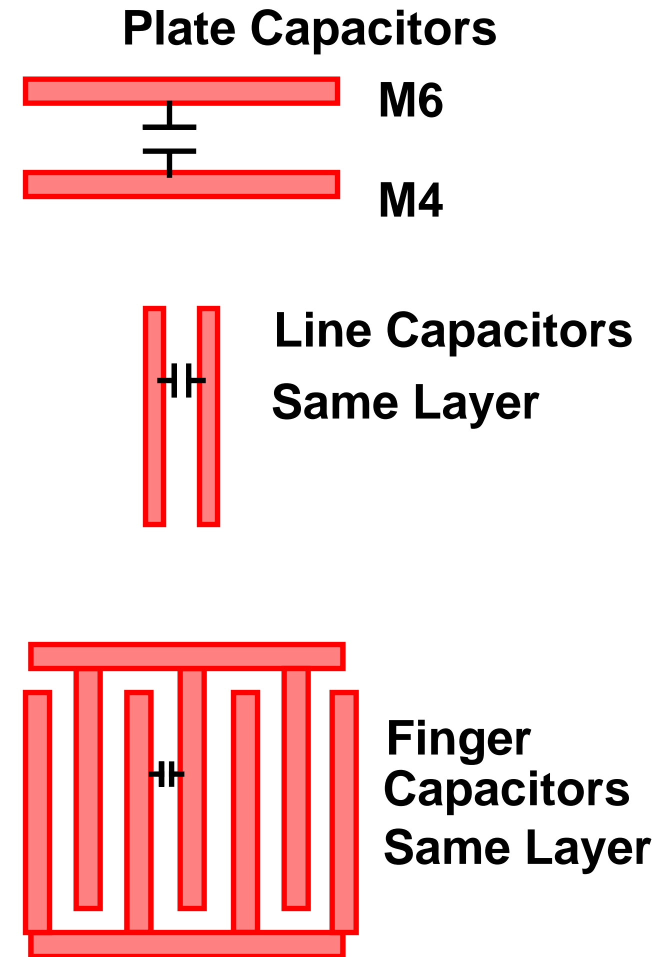
Variation Modeling for RC Extraction

```
...
CONDUCTOR M5 {SIDE_TANGENT = 0.06 THICKNESS = 0.26 WMIN = 0.15 SMIN = 0.15}
RPSQ_VS_WIDTH_AND_SPACING {
SPACINGS {0.15 0.19 0.6 0.9}
WIDTHS {0.15 0.21 0.35 0.6 1.1 1.6}
VALUES {...}}

DENSITY_BOX_WEIGHTING_FACTOR {(6 0.15) (20 0.37) (50 0.48)}

THICKNESS_VS_DENSITY {(0.2 0.058).... (0.8 -0.015)}

THICKNESS_VS_WIDTH_AND_SPACING CAPACITIVE_ONLY {
SPACINGS {0.15 0.19 0.6 0.9 1.5 2.5}
WIDTHS {0.15 0.21 0.35 0.60 1.0 1.5}
VALUES {...}}

ETCH_VS_WIDTH_AND_SPACING CAPACITIVE_ONLY {
SPACINGS {0.15 0.19 0.6 0.9 1.5 2.5}
WIDTHS {0.15 0.21 0.35 0.6 1.0 1.5}
VALUES {...}}
...
```



Capacitance Extraction Accuracy



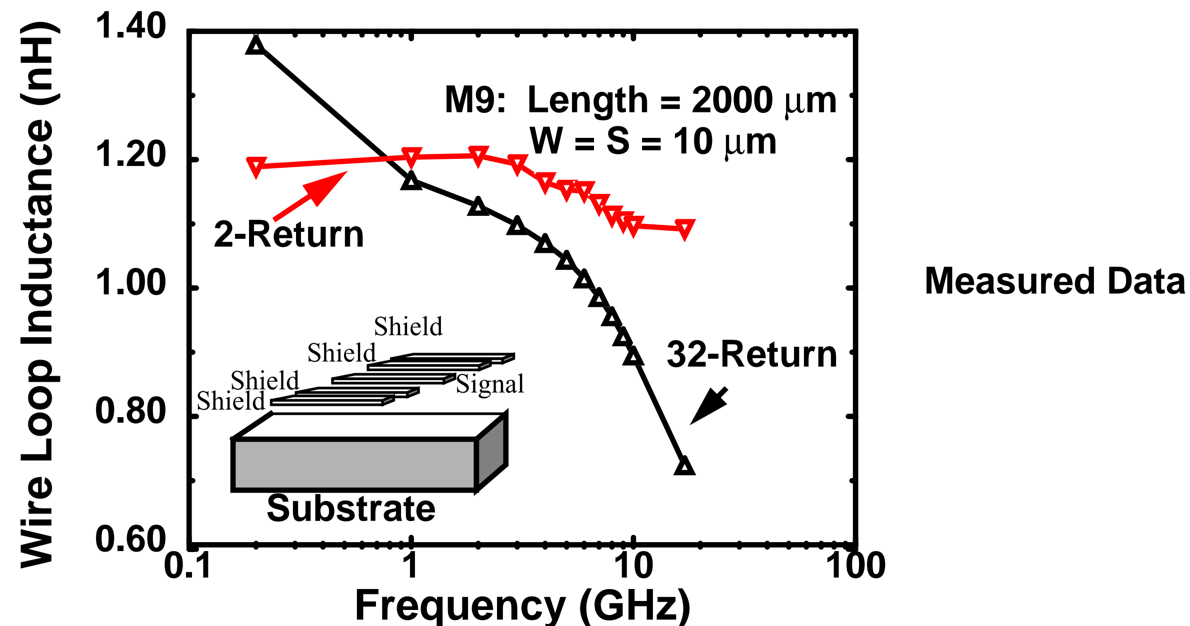


Inductance Variations

- Inductance is a weak function of geometries.

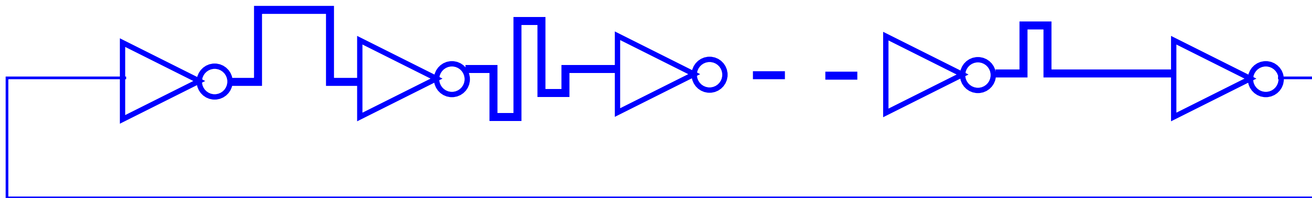
$$L_{self} = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{(w+t)} + \frac{1}{2}\right] \qquad M = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{d} - 1\right]$$

- Return paths may vary due to frequencies.



Measured Data

Ring Oscillators



Load Type	Measured Period (101 Stages)	Simulated Period (101 Stages)	Error
Unloaded	3.09s	3.09s	0
Random wire load (M3)	26.2s	25.7s	-1.9%
Random wire load (M5)	26.4s	27.0s	2.3%

Summary

- The measurements of a 90 nm test chip show strong metal thickness/width variations due to the CMP process in nanometer technologies.
- Simple, yet accurate modeling methods are proposed to extract interconnect *RC* variations as a function of metal density, width and space.
- Results show excellent agreement between on-wafer measurements and extraction.