Measurement and Characterization of Pattern Dependent Process Variations of Interconnect Resistance, Capacitance and Inductance in Nanometer Technologies

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ABSTRACT

Process variations have become a serious concern for nanometer technologies. The interconnect and device variations include inter- and intra-die variations of geometries, as well as process and electrical parameters. In this paper, pattern (i.e. density, width and space) dependent interconnect thickness and width variations are studied based on a well-designed test chip in a 90 nm technology. The parasitic resistance and capacitance variations due to the process variations are investigated, and process-variation-aware extraction techniques are proposed. In the test chip, electrical and physical measurements show strong metal thickness and width variations mainly due to chemical mechanical polishing (CMP) in nanometer technologies. The loop inductance dependence of return patterns is also validated in the test chip. The proposed new characterization methods extract interconnect *RC* variations as a function of metal density, width and space. Simulation results show excellent agreement between on-wafer measurements and extractions of various *RC* structures, including a set of metal loaded/unloaded ring oscillators in a complex wiring environment.

Categories and Subject Descriptors

J.6 **[Computer-aided engineering]**: Computer-aided design

General Terms

Algorithms

Keywords

VLSI Interconnects, Extraction, Measurement, Process Variations

1. INTRODUCTION

As technology scales to the nanometer region, process variations have become a serious concern, which cause significant interconnect and device inter-/intra-die parameter variations. These variations include device geometry change, dopant density change, threshold voltage and circuit timing change, etc. Some of the variations are random and some are systematic. In terms of interconnect geometries, interconnect patterns (i.e., the wire density, wire width and space) have a major impact on wire thickness and width as well as inter-layer dielectric (ILD) thickness. Due to this interconnect pattern dependent process variations of metal (and ILD) thickness and width, wire parasitic resistance, capacitance and inductance vary within a chip and across different dies. The parasitic *RLC* variations further cause circuit performance variations [1]-[5]. Mehrotra [5] shows that clock skew increases from about 15% to 30% of clock cycles due to both random and systematic variations in interconnect and device parameters as technology scales from 180 nm to 50 nm. In other words, *RC* extraction without taking into account process variations can cause inaccuracy in circuit performance simulation, like clock timing estimation, of 15% to 30% error. Capturing and modeling the variations become essential to device and interconnect extraction tools for accurate timing and power analysis. Traditional *RC* extraction is no longer adequate for today's technology. Studies show that most of the interconnect variations are from chemical mechanical polishing (CMP) process, which are based on systematic pattern or spatial effects (metal density, width and space) [6][7]. Accurate modeling of CMP effects become key to interconnect parasitic extraction in nanometer technologies.

In this paper, the design and measurement of a test chip in 90 nm are presented to gain insights into the CMP pattern dependent variations. Firstly, the interconnect CMP pattern dependent thickness and width variations are studied. Secondly, the resistance and capacitance variations due to the pattern dependent geometry changes are investigated, and new modeling techniques are proposed and implemented to accurately extract the wire resistance and capacitance. Finally, results are presented which show excellent agreement between measurements and simulations. In addition, circuits like ring oscillators were designed and measured to validate the proposed resistance and capacitance extraction tool in a complex wiring environment. The extraction tool implemented based on this process variation modeling renders much more accurate extraction results, and thus ensure more accurate timing and noise simulations.

The paper is organized as follows. Section 2 analyzes the pattern dependent interconnect geometry variations which were measured in a 90 nm test chip. Section 3 proposes the effective modeling techniques for resistance and capacitance extractions, and results are validated by measurements. Conclusions are drawn in Section 4.

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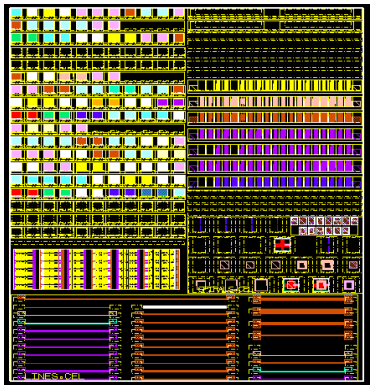

Fig. 1. The 90 nm test chip: structures consist of various density, width and space resistor combinations as well as capacitance and inductance configurations. Some ring oscillators for electrical measurement were also designed.

2. PATTERN DEPENDENT PROCESS VARIATIONS

2.1 Overview of the Test Chip

A 90 nm test chip (see Fig. 1) was designed to study intra-die interconnect variations of metal thickness and cross-section etching/width, and the variation impact on *RLC* parameters. These variations are mostly from the CMP process. Since metal wire density is the major cause of the CMP pattern dependent metal thickness variation, *RLC* test structures were designed to include various metal densities with numerous width and space combinations. Electrical (*RLC*) and physical (from SEM photos) parameters were measured to characterize the intra-die variations, see Fig. 2. These parameter variations were compared with extractions and simulations. For more complicated cases, ring oscillators were designed to further validate extraction methodologies by circuit simulation using HSPICE. The ring oscillators have different metal wire loads which go through various routing environments.

2.2 Metal Thickness and Width Variations due to the CMP

Pattern dependent CMP causes metal wire thickness reduction due to two effects known as dishing and erosion. The metal thickness variation can be modeled as a function of metal pattern density, width and space. Dishing is proportional to metal width, while erosion is inversely proportional to metal space [8][9]. Fig. 3 shows the measurement of metal thickness variation with metal space. Although the relationship depends on both effects of dishing and erosion, higher density results in smaller metal thickness. In Fig. 4, normalized measured metal thickness variations of various width and space show a quite complex non-linear effect. For the same width, a smaller space results in larger metal thickness. In terms of thickness variations, the measured data indicate that higher density results in larger variations. The maximum and minimum metal thicknesses of ten different densities (20% to 70%) are normalized to 50% density thickness. See Fig. 5.

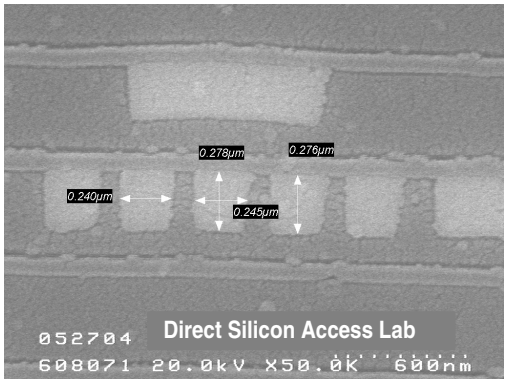

Fig. 2. SEM photos were measured to get physical dimensions of metal thicknesses and widths for physical and electrical correlation and verification.

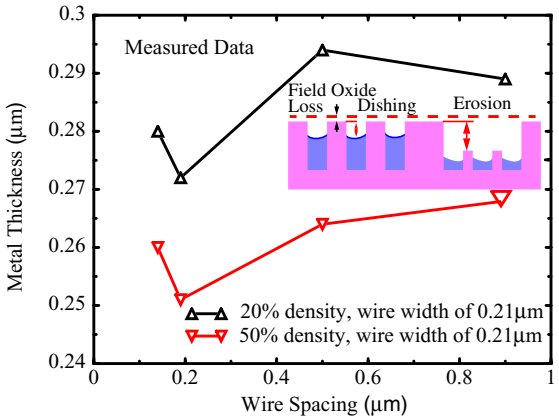

Fig. 3. Metal thickness variation is due to CMP dishing and erosion, which are functions of the polish time. Metal density dominates metal thickness variations.

To model the wire thickness variations as a function of metal density in extraction tools, on-chip metal densities can be modeled using three density boxes at 6 µm, 20 µm and 50 µm away from a target wire. Three weight factors associated with the three box sizes can be determined from an optimization process. In Table 1, the weight factors are used to calculate the effective densities, which are used to find corresponding wire thickness.

$$Density_{effective} = \sum_{i=1to3} Density(X_i) \bullet W(X_i)$$

where X_i is the three boxes, and $W(X_i)$ is the weights. This is par-

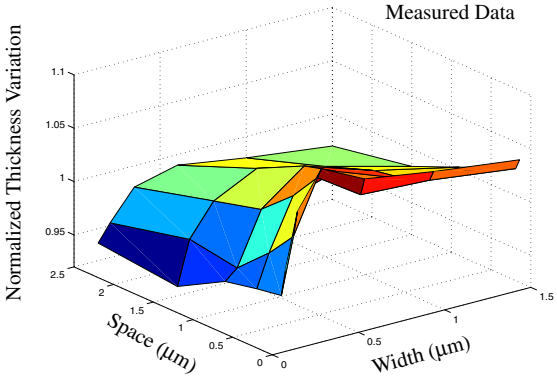

Fig. 4. Normalized average metal thickness variations: Generally speaking, metal thickness is the largest for the smallest space, and decreases as the space increases.

Table 1: DENSITY BOX DEFINITION AND WEIGHT FACTORS FOR EFFECTIVE DENSITY

Density Combinations	A	B	C	D	E	F	G	H	I	J	K
6 µm Box Density (Weight Factor: 0.15)	0.2	0.2	0.2	0.2	0.5	0.5	0.5	0.7	0.6	0.7	0.7
20 µm Box Density (Wight Factor: 0.37)	0.2	0.6	0.3	0.7	0.5	0.3	0.7	0.7	0.3	0.7	0.3
50 µm Box Density (Weight Factor: 0.48)	0.2	0.25	0.6	0.7	0.5	0.6	0.3	0.7	0.6	0.3	0.2
Effective Density	0.2	0.37	0.43	0.63	0.5	0.47	0.48	0.7	0.49	0.51	0.31

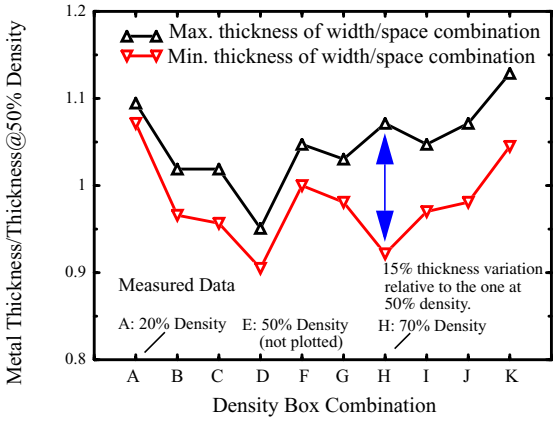

Fig. 5. The highest density (70%) at H shows the largest thickness variation. The max. and min. metal thicknesses at different densities are normalized to the ones at 50% density. Density boxes are defined in Table 1.

ticularly useful to model a complex wiring environment which surrounds a target extraction wire. To determine the final density and the thickness of a wire, the effective density is calculated based on the densities in the three boxes and their respective weights. To validate the accuracy of the three density box model with their weight factors, modelled data are compared with measured thickness data for various effective densities. In Fig. 6, the results show that the model can accurately characterize the thickness variations. The average error for all eleven data points is -0.012%, and all points are within +/- 2% error.

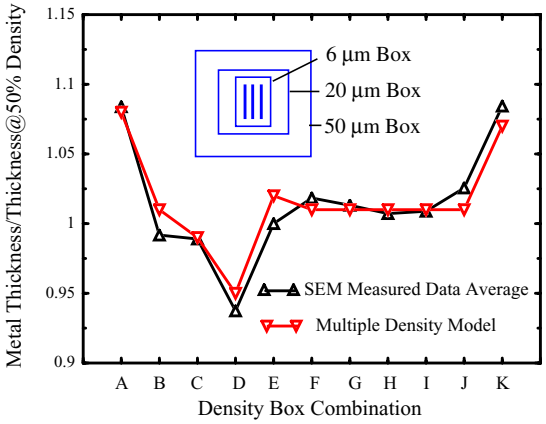

Fig. 6. Normalized average thicknesses (to 50% density data) from SEM photos at different densities match the normalized metal thicknesses calculated from the three density box models.

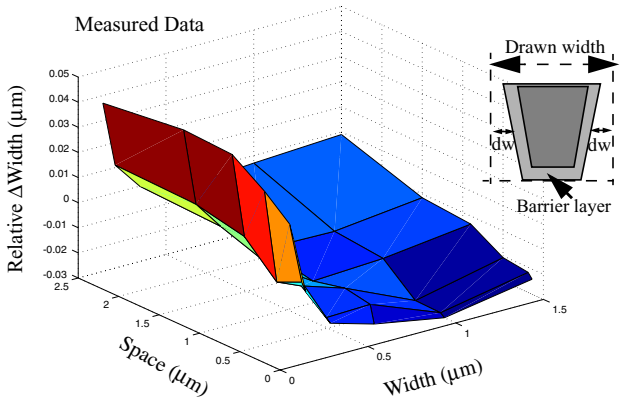

Fig. 7. Width variation is due to the etching process. The Δwidth equals drawn width minus measured trapezoidal mid point width. The relative Δwidth is the Δwidth minus average Δwidth.

Due to the etching process, wire width can change. Basically, the cross-section is trapezoidal with larger edge at the top. The midpoint width of the cross-section has impact on the resistance of wires and the side wall capacitance. To study the process variation on the width, measured etching variations are plotted in Fig. 7. The variation is affected by many factors, namely, photolithographic process, mask preparation including OPC models, etc. The process-variation-aware extraction tools need to model these observed effects accurately.

3. MODELING FOR PATTERN DEPENDENT *RLC* VARIATIONS

Process variations can be modeled using technology files or analytical formulae for process-variation-aware extraction tools. Technology files are process dependent and can be created based on the information provided by foundries. In this section, a technology file is generated based on the data from the test chip measurement, where metal thickness and etch variations vs. density, width and spacing are modeled.

3.1 Resistance Extraction

Once metal thickness and width variations are captured by models (Fig. 8), it facilitates to extract resistance and capacitance accurately due to the CMP process variations. Test structures are used to extract sheet resistance as a function of wire density, width, and space, which can be used to form a technology file for a specific technology. In other words, the sheet resistance dependence of wire width

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...
CONDUCTOR M5 {SIDE_TANGENT=0.06 THICKNESS=0.26
WMIN=0.15 SMIN=0.15}
  RPSQ_VS_WIDTH_AND_SPACING {
   SPACINGS {0.15 0.19 0.6 0.9}
   WIDTHS {0.15 0.21 0.35 0.6 1.1 1.6}
   VALUES {...,
  ...}}

  DENSITY_BOX_WEIGHTING_FACTOR {(6 0.15) (20 0.37) (50
0.48)}

  THICKNESS_VS_DENSITY {(0.2 0.058).... (0.8 -0.015)}

  THICKNESS_VS_WIDTH_AND_SPACING CAPACITIVE_ONLY {
  SPACINGS {0.15 0.19 0.6 0.9 1.5 2.5}
  WIDTHS {0.15 0.21 0.35 0.60 1.0 1.5}
  VALUES {...}}

  ETCH_VS_WIDTH_AND_SPACING CAPACITIVE_ONLY {
   SPACINGS {0.15 0.19 0.6 0.9 1.5 2.5}
   WIDTHS {0.15 0.21 0.35 0.6 1.0 1.5}
   VALUES {...}}
  ...
```

Fig. 8. A technology file describes metal thickness, sheet resistance, and etching variations due to process variations. Only the part related to metal layer 5 is shown.

and space can be modeled together with metal density (and thus thickness) as shown in Fig. 9. Furthermore, etching effects as well as cladding material effects need to be included. The cladding material is a barrier layer to prevent Cu leakage in the Cu interconnect technology. Without modeling the cladding layer, wire resistance extraction error can be as high as 50% in small pitch wires. Effective wire sheet resistance at any width and space combinations are obtained to model the cladding effect. In terms of sheet resistance variation as a function of density, Fig. 10 illustrates metal density dependency of normalized sheet resistance in metal 5. High density sheet resistance shows higher variations. Resistance variation models have been implemented using characterized technology look-up table and analytical formulae. Extraction results based on the proposed models show excellent agreement with the measured data (Fig. 11).

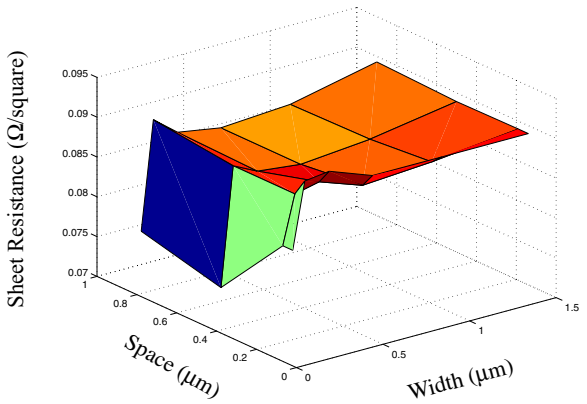

Fig. 9. Sheet resistance for metal density of 50% in M5: Measured resistance of test structures were converted into sheet resistance using drawn resistor dimensions. The cladding layer effect is included.

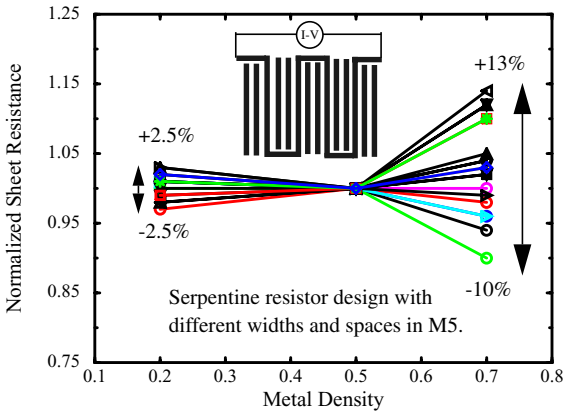

Fig. 10. Sheet resistances are normalized to 50% density for 19 different width and space combinations. The high density sheet resistor shows higher variation.

3.2 Capacitance Extraction

Like resistance model, capacitance variation models are built based on wire thickness and width variations. Capacitance structures are designed to validate models of the variation impact of etching/width, space, dielectric layer and metal thickness on capacitance extraction. The structures include various plate, line and finger capacitors. With a technology file which accurately models these dependencies, capacitance extraction with process variations has good agreement with measured data (e.g., Plate capacitors within 2% errors, and finger capacitors within 5% errors). Moreover, metal fill is essential to nanometer designs in order to reduce process variations. Accurate capacitance modeling with metal fills is highly desirable. In Fig. 12, capacitances in the presence of metal fills are extracted, and compared with measured data. The errors are within +/- 5%.

3.3 Inductance Extraction

Inductance is a weak function of wire metal thickness and width as shown below.

$$L_{self} = \frac{\mu_0 l}{2\pi}\left[\ln\frac{2l}{(w+t)} + \frac{1}{2}\right]$$

where l, w, and t are wire length, width and thickness, respec-

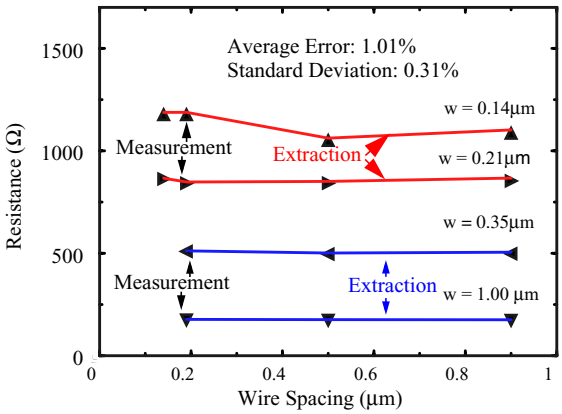

Fig. 11. Resistance extraction of wires with length of 2000 mm in M5 has excellent agreement with measured data. Only data for 50% density are plotted.

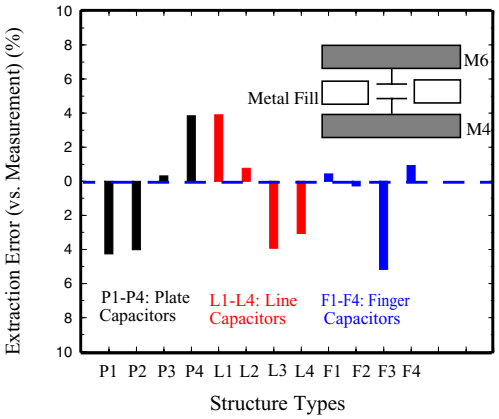

Fig. 12. Capacitance extraction with one floating metal layer: Three sets of capacitance structures include plate capacitors, line capacitors and finger capacitors, all of which have metal fills in them.

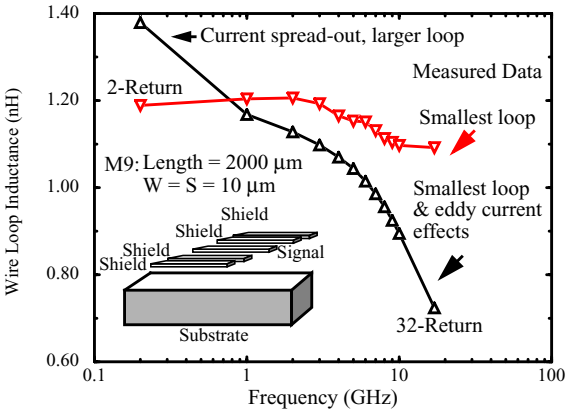

Fig. 13. Loop inductance of 32-returns is larger at low frequencies due to larger loop, but it is smaller than the one of 2-return structure (the smallest loop) at high frequencies, due to eddy current effects.

tively. μ_0 is the permeability. Self and mutual inductance vary little with current scale of process variations [10]. However, wire pattern variations may offer more or fewer return paths for signals, and result in a significant loop inductance variation. Fig. 13 shows loop inductance variations with signal frequency. The 32-return structure has larger loop inductance at low frequencies, but has much smaller inductance at high frequencies due to the eddy effect.

3.4 *RLC* Validation

In order to validate *RLC* extraction in a complex wiring environment, ring oscillators were designed to have various random wire loads in the test chip. Resistance, capacitance, and inductance were extracted based on the proposed methods, and SPICE models and netlist were generated from the same die. Circuit simulations show small timing errors compared to measurements as shown in Table 2, which validate the accuracy of the models and *RC* extractions.

TABLE 2 **RING OSCILATOR MEASUREMENT AND SIMULATION (Units: ns)**

Load Type	Measured Period (101 Stages)	Simulated Period (101 Stages)	Error
Unloaded	3.09	3.09	0
Random wire load (M3)	26.2	25.7	-1.9%
Random wire load (M5)	26.4	27.0	2.3%

4. CONCLUSIONS

As IC technologies advance to the nanometer era, process variations are a serious concern. The design-for-yield (DFY) and design-for-manufacture (DFM) have become essential to high performance integrated circuit designs. In this paper, electrical and physical measurements of a 90 nm test chip show strong metal thickness and width variations due to the CMP process in nanometer technologies. New characterization and modeling methods are proposed to extract interconnect *RC* variations as a function of metal density, width and space. Results show excellent agreement between on-wafer measurements and values from the extraction and simulation tools.

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