

On-chip Inductance Modeling and RLC Extraction of VLSI Interconnects for Circuit Simulation

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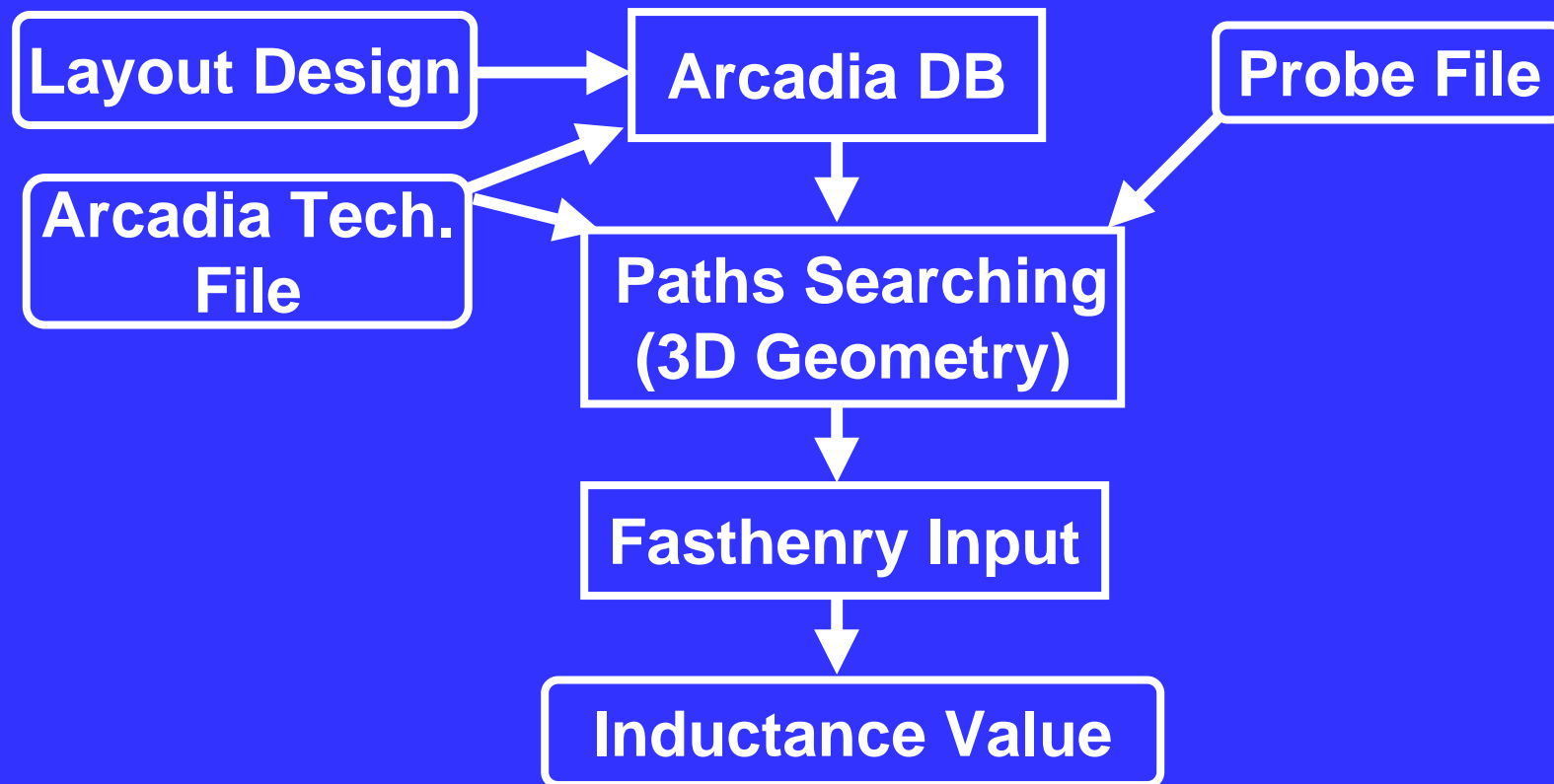
Outline

- **Background and motivation**
- **3D geometry modeling and inductance extraction using field solvers**
- **Analytical formulae for inductance estimation**
- **Applications in circuit simulation**
- **Summary**

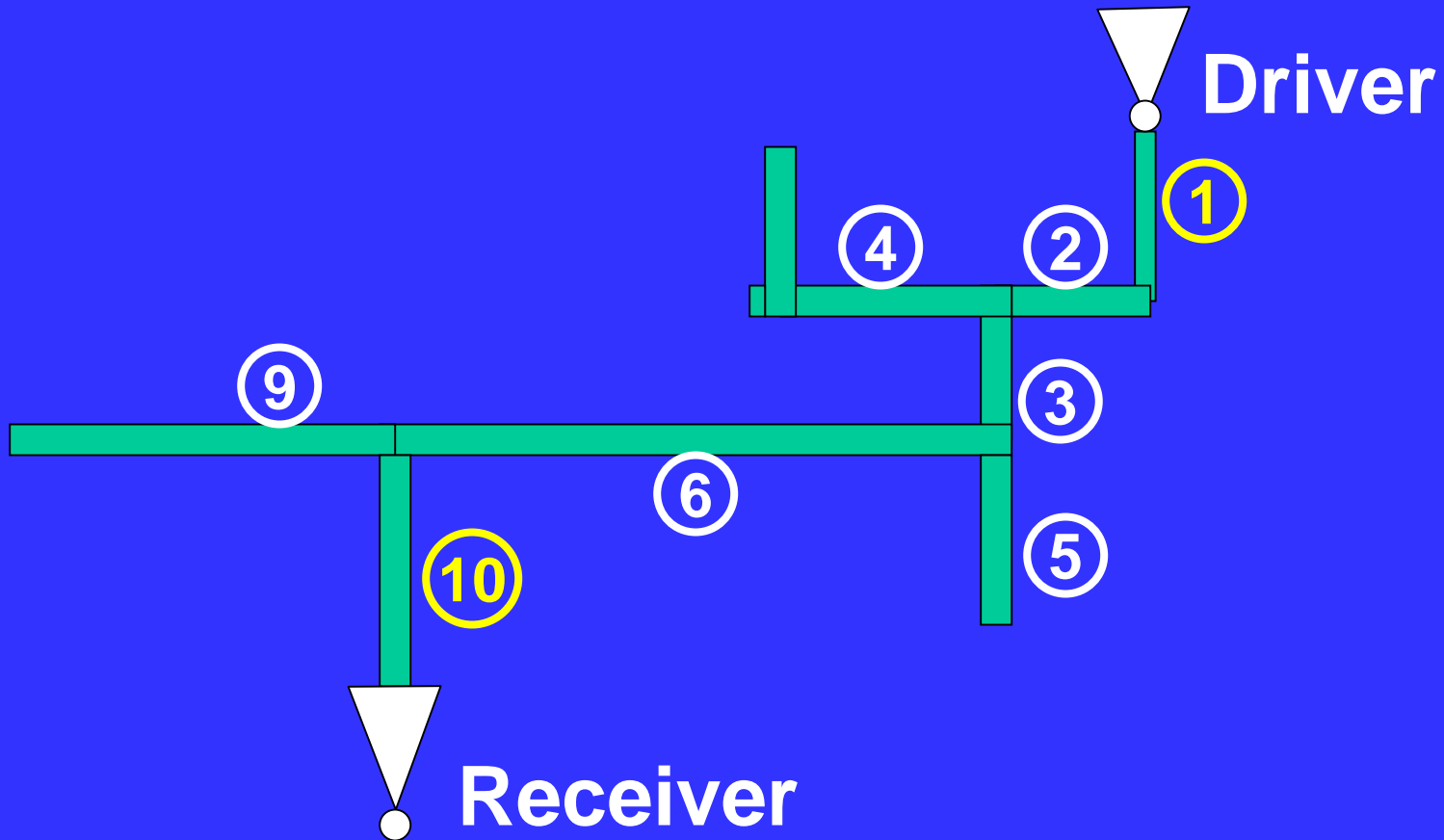
Background and Motivation

- Long wires exhibit transmission line effects with faster transistor rise/fall time.
- Inductance component becomes comparable to resistance component.
- Signal ringing and inductive cross talk are observed. Ground bounce becomes worse.

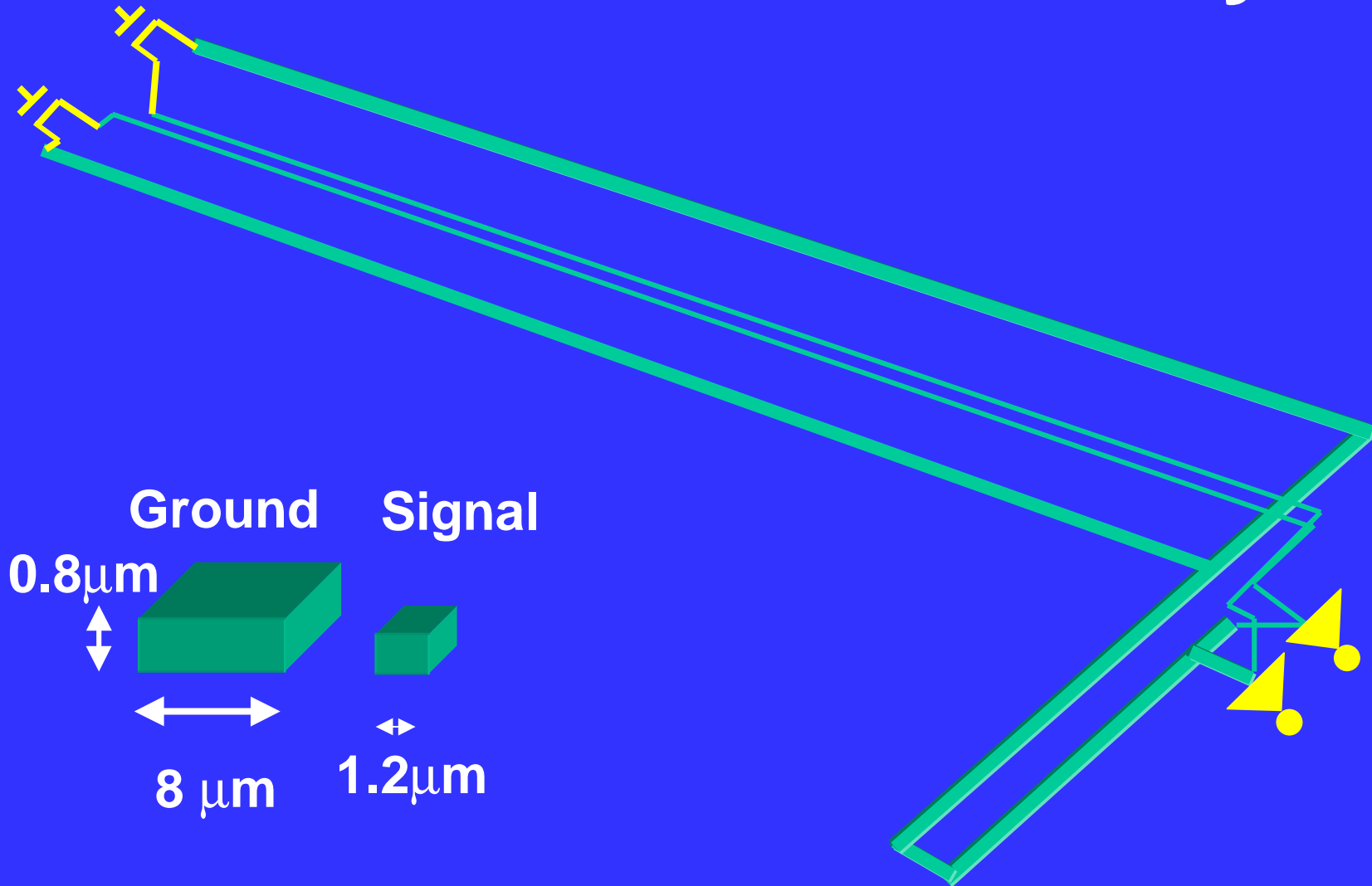
3D Geometry Modeling for Field Solver



Path Searching in 3D Geometry Modeling

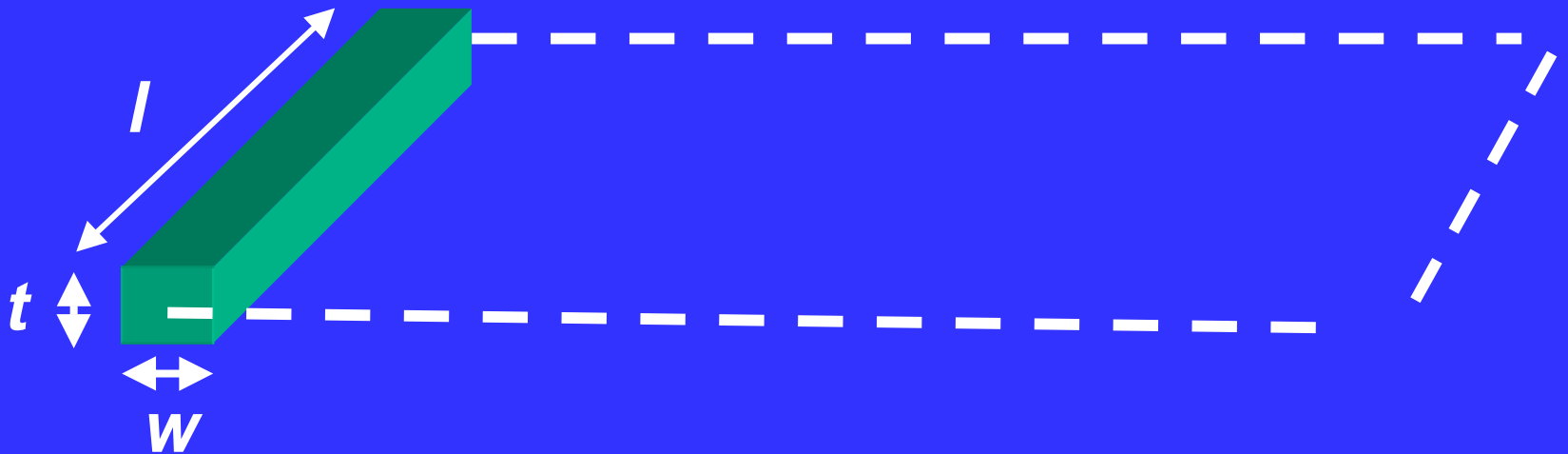


Extracted 3D Geometry



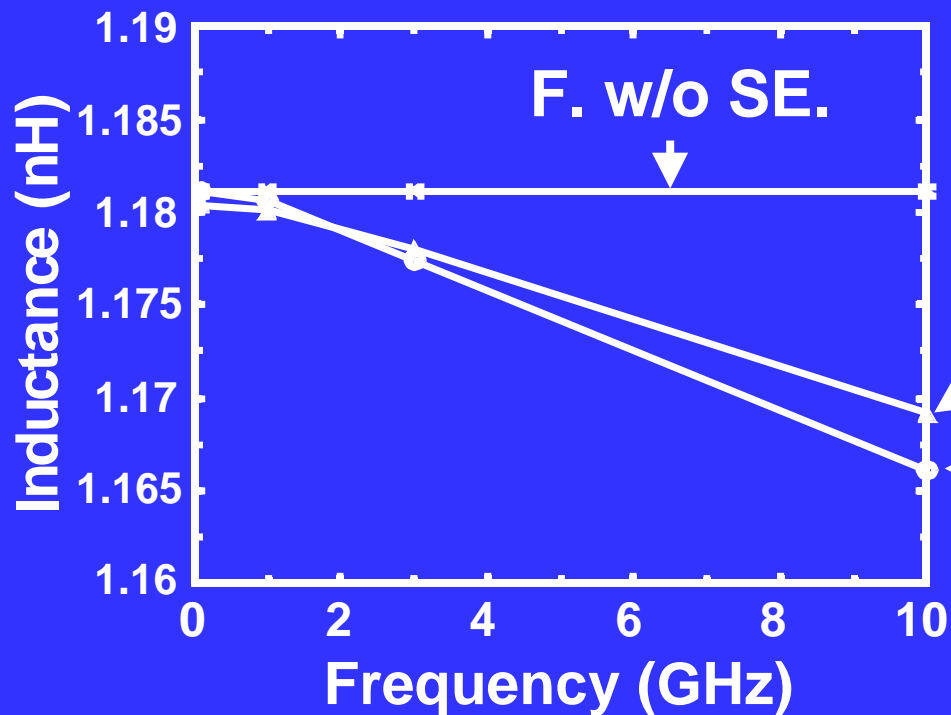
Self-inductance Formula

$$L_{self} = \frac{\mu_0 l}{2\pi} \left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.447(w+t)}{2l} \right]$$



Self-inductance With Skin Effect

$$L_{self} = \frac{\mu_0 l}{2\pi} \left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.2235(w+t)}{l} - \mu_r(0.25 - X) \right]$$

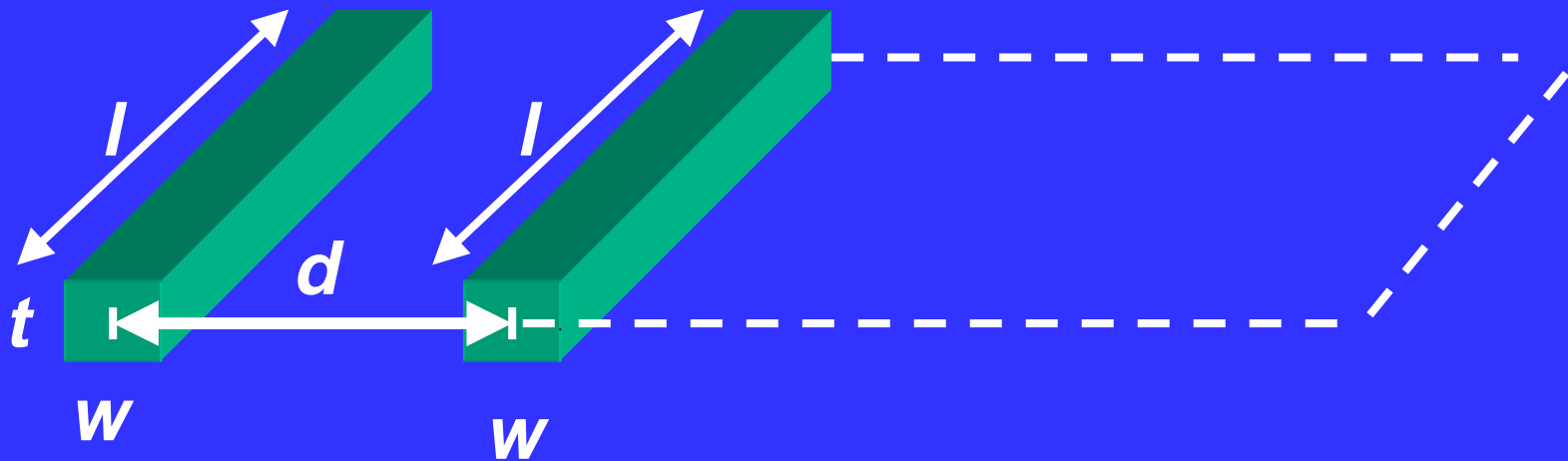


$$X = f(\delta)$$

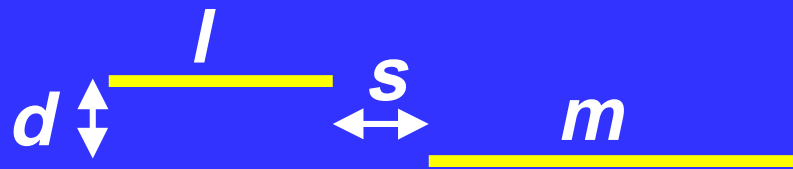
$$W = 8 \mu\text{m} \quad t = 1 \mu\text{m} \\ l = 1 \text{ mm}$$

Mutual Inductance

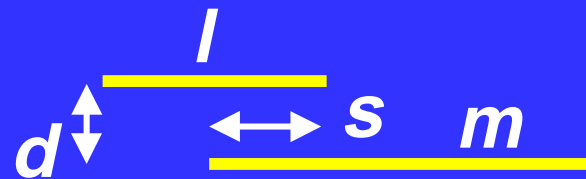
$$M = \frac{\mu_0 l}{2\pi} \left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l} \right]$$



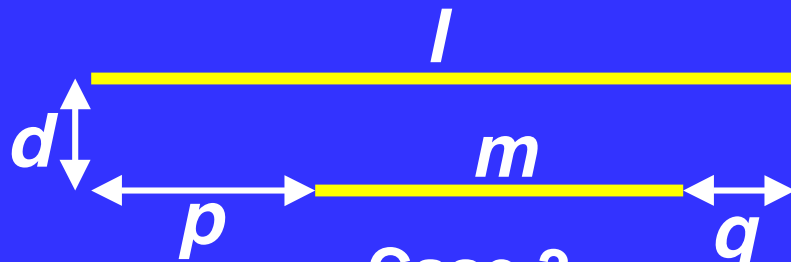
Six Different Positions



Case 1



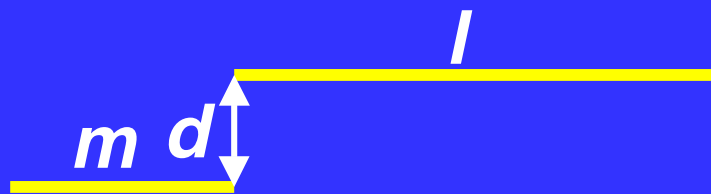
Case 2



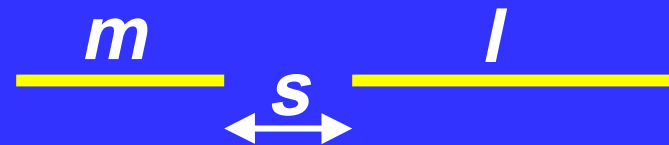
Case 3



Case 4

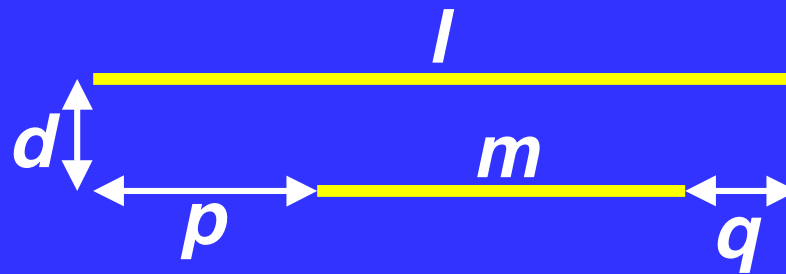


Case 5



Case 6

Calculating Mutual Inductance

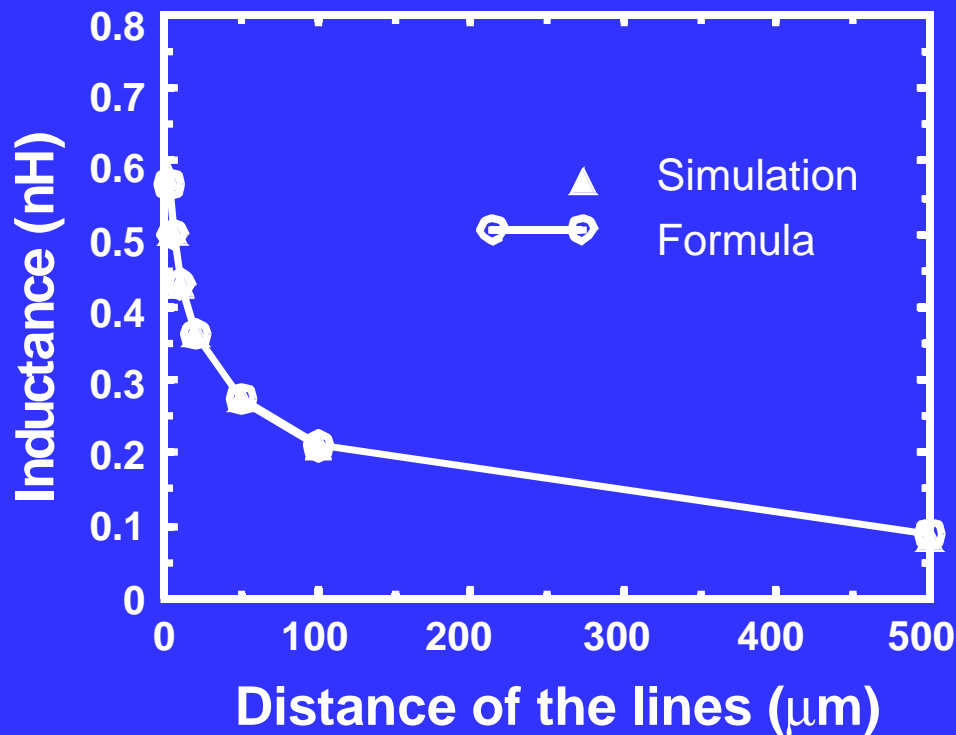


CASE 3

$$M = \frac{1}{2} [(M_{m+p} + M_{m+q}) - (M_p + M_q)]$$

Formula and Simulation

$$M = \frac{\mu_0}{4\pi} \left[l \ln\left(\frac{l}{l-m}\right) + m \ln\left(\frac{4m(l-m)}{d^2}\right) - 2m + d \right]$$



Case 4:

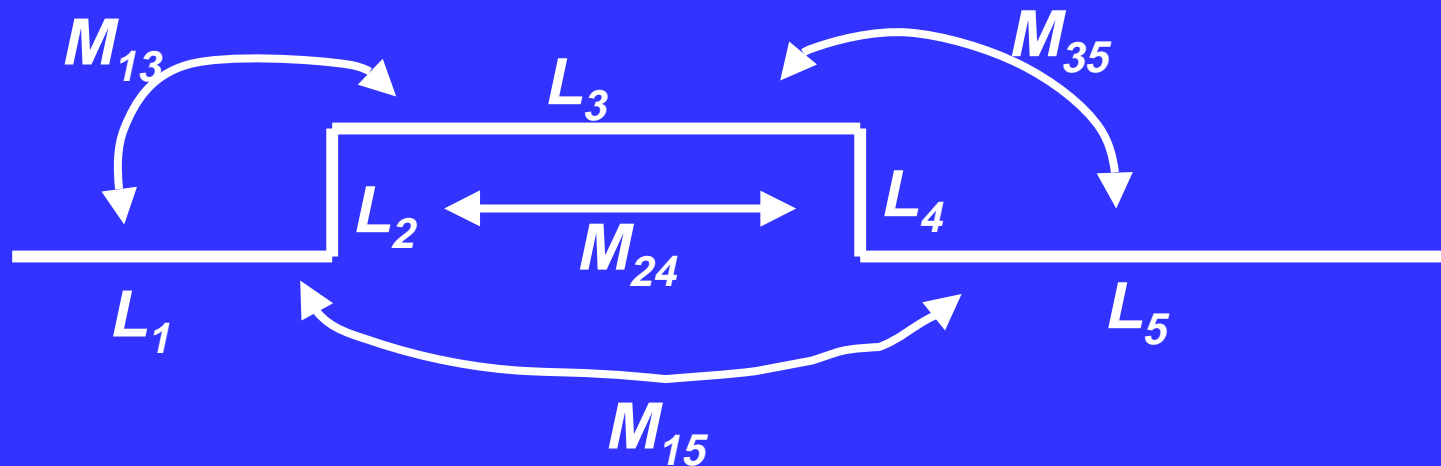
1 mm

d

0.5 mm

$W = 5 \mu\text{m}$, $t = 1 \mu\text{m}$

Self Inductance of a Whole Wire



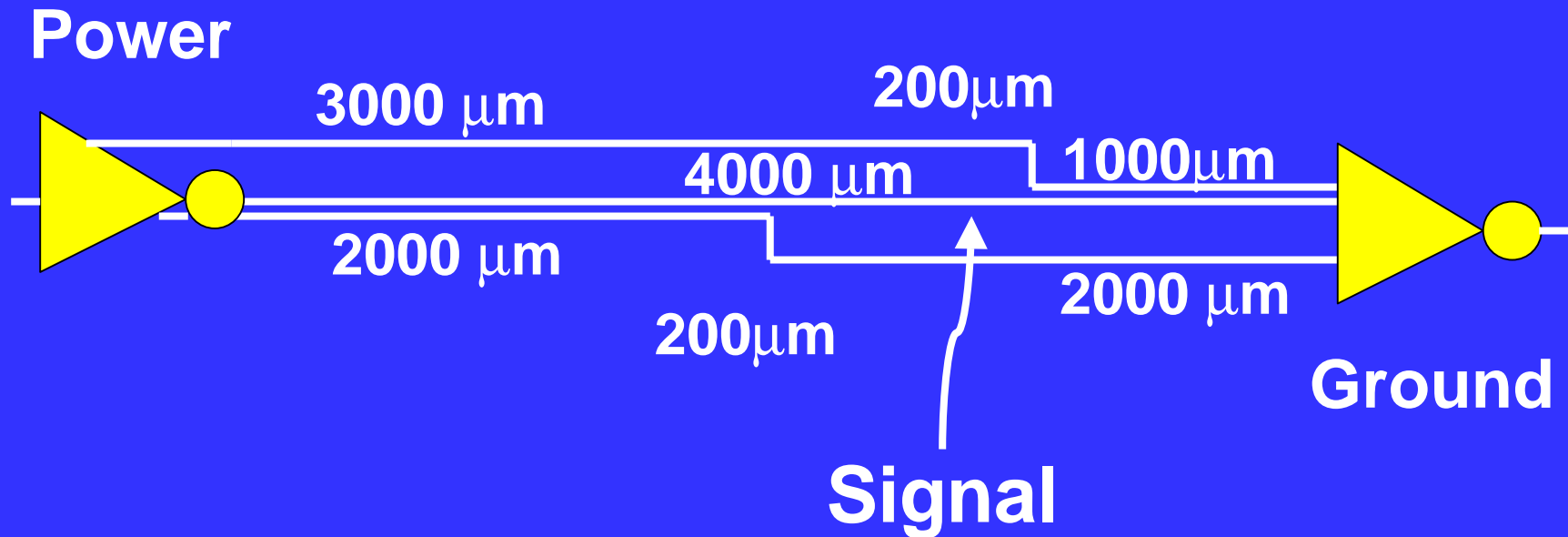
$$L_{total} = \sum_{i=1}^5 L_i + 2M_{13} + 2M_{15} + 2M_{24} + 2M_{35}$$

Formula and Simulation of Self Inductance

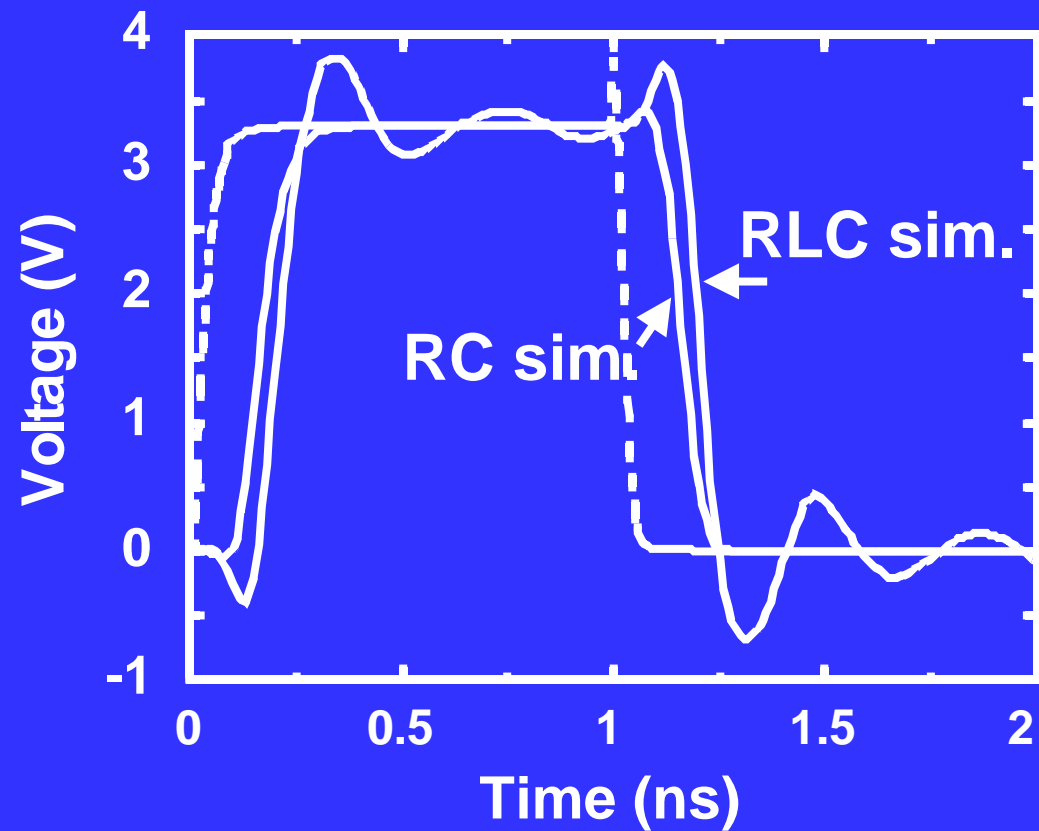
Inductance Unit: nH

Wire1: 3 segments, 3 turns (1.8 mm)			Wire2: 4 Segments, 4 turns (2.1 mm)			Wire3: 5 Segments, 5 turns (4 mm)		
Sim.	Cal.	Err.	Sim.	Cal.	Err.	Sim.	Cal.	Err.
2.27	2.26	0.4%	2.93	2.86	2.3%	5.35	5.17	3.4%

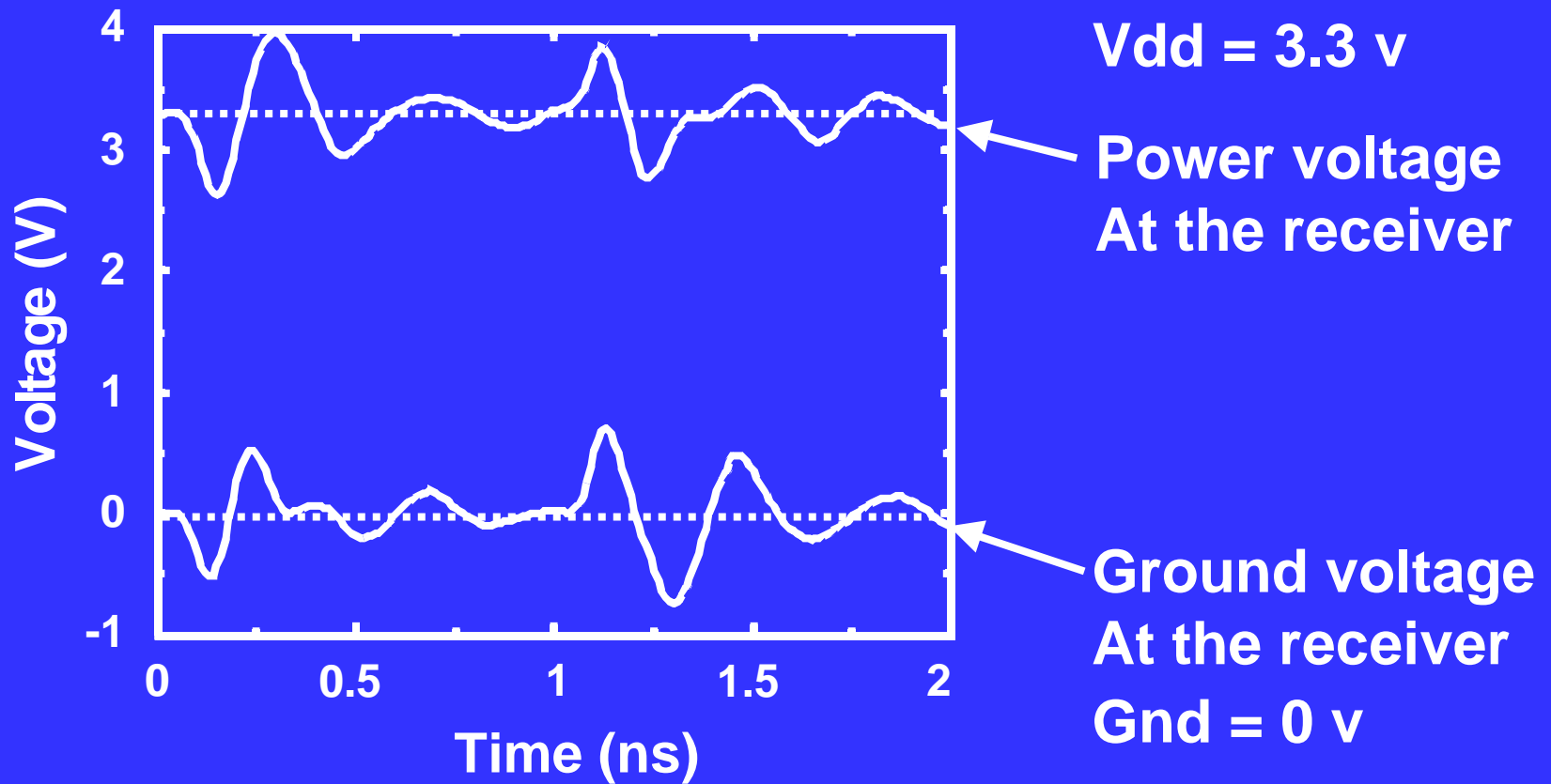
One Global Line Example



Signal Ringing Effects



Power and Ground Noise



Summary

- **Accurate automatic 3D geometry generation**
- **Analytical formulae for self and mutual inductance estimation**
- **Impact of on-chip inductance on signal integrity and power/ground noise**