Simulation and Analysis of Inductive Impacts on VLSI Interconnects in the Presence of Process Variations

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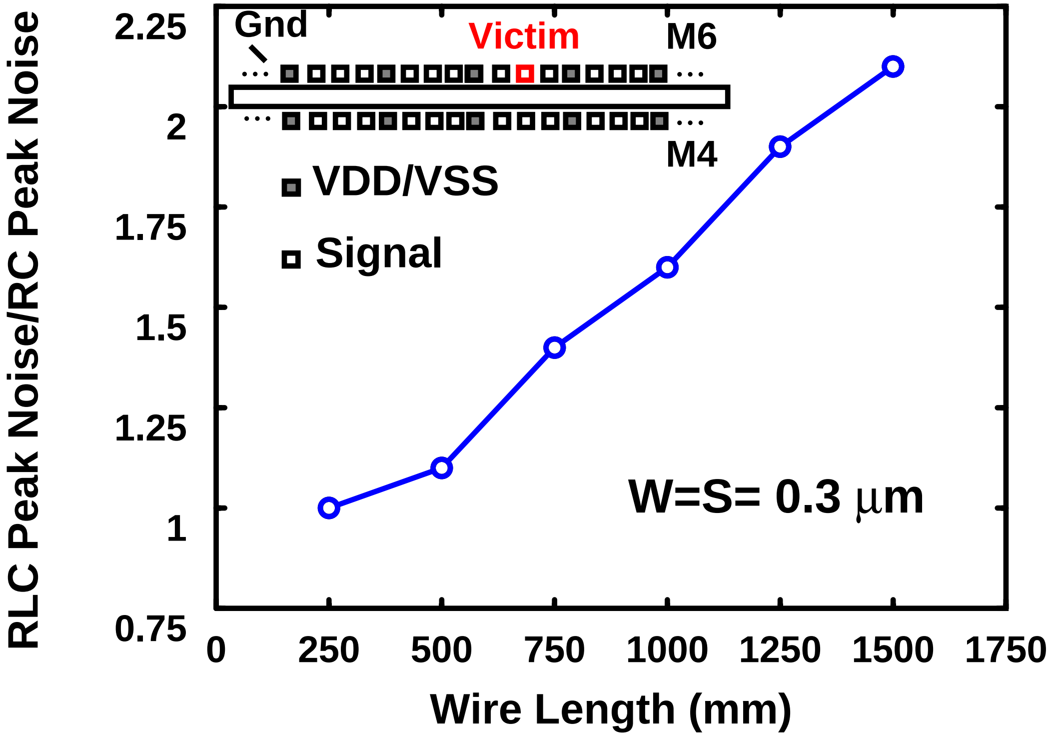
Outline

- Background and Motivation
- Inductive Impacts on Timing and Noise in 90nm Technology
- Process Variation Impacts on Timing and Noise in 90nm Technology
- Inductive Impacts in the Presence of Process and Environment Variations
- Conclusions

Background and Motivation

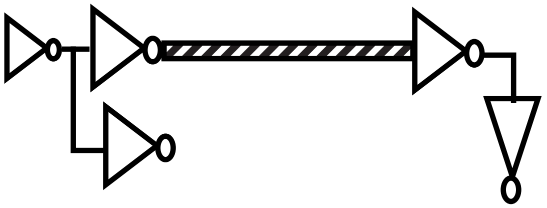
- On-chip inductance impact on signal integrity has been a problem for deep-submicron designs.



A 90 nm process technology

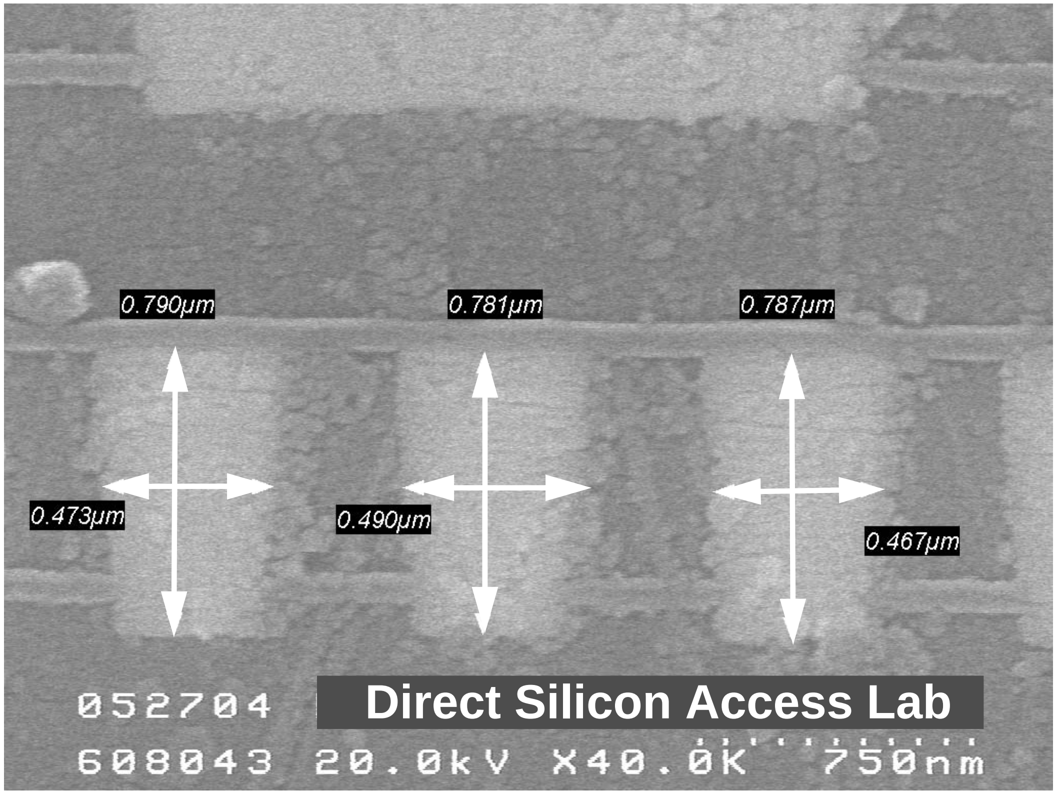
Two 15-bit buses in M6&M4

Input rise time: 48ps (20-80%)

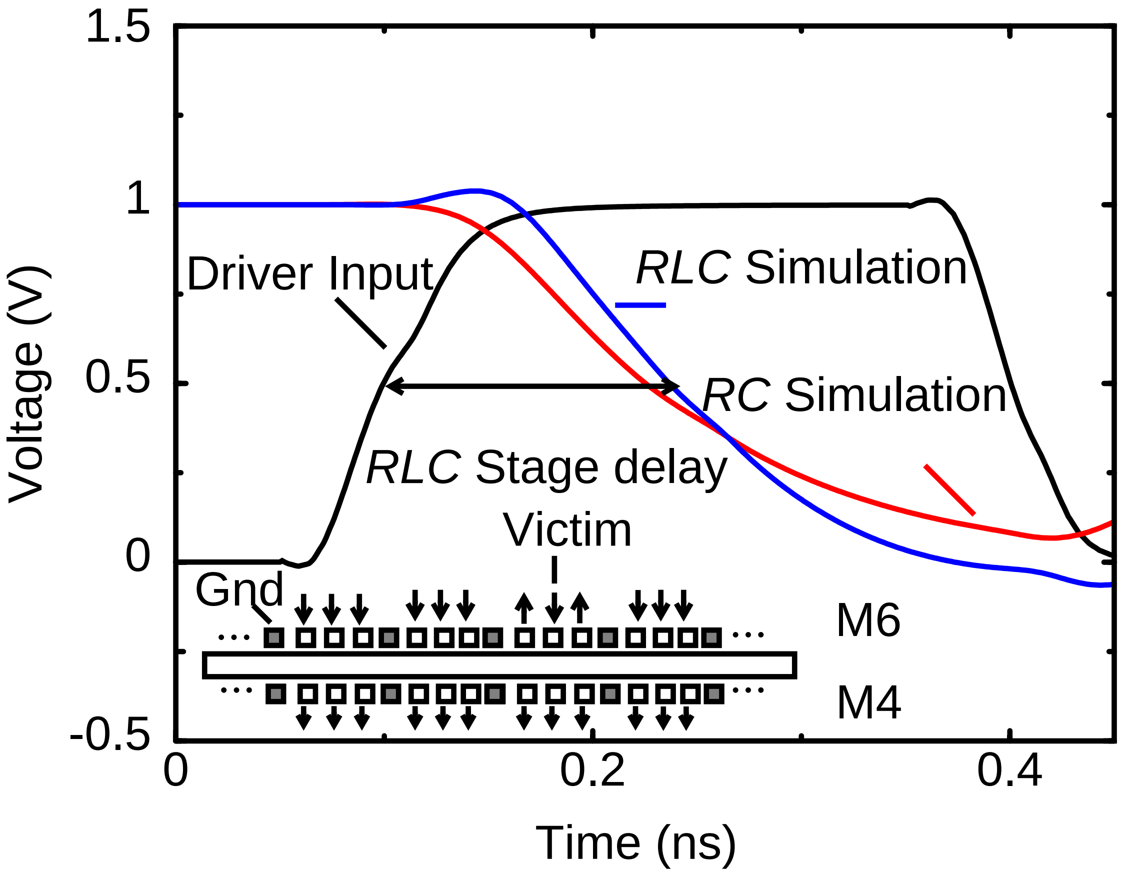


Background and Motivation

- Process variations become an issue in 90 nm technology and beyond

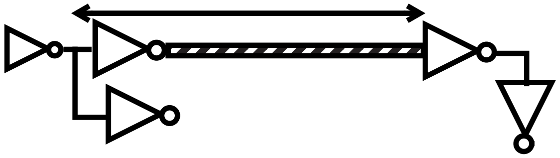


Inductive Impact on Stage Delay for Bus Signals



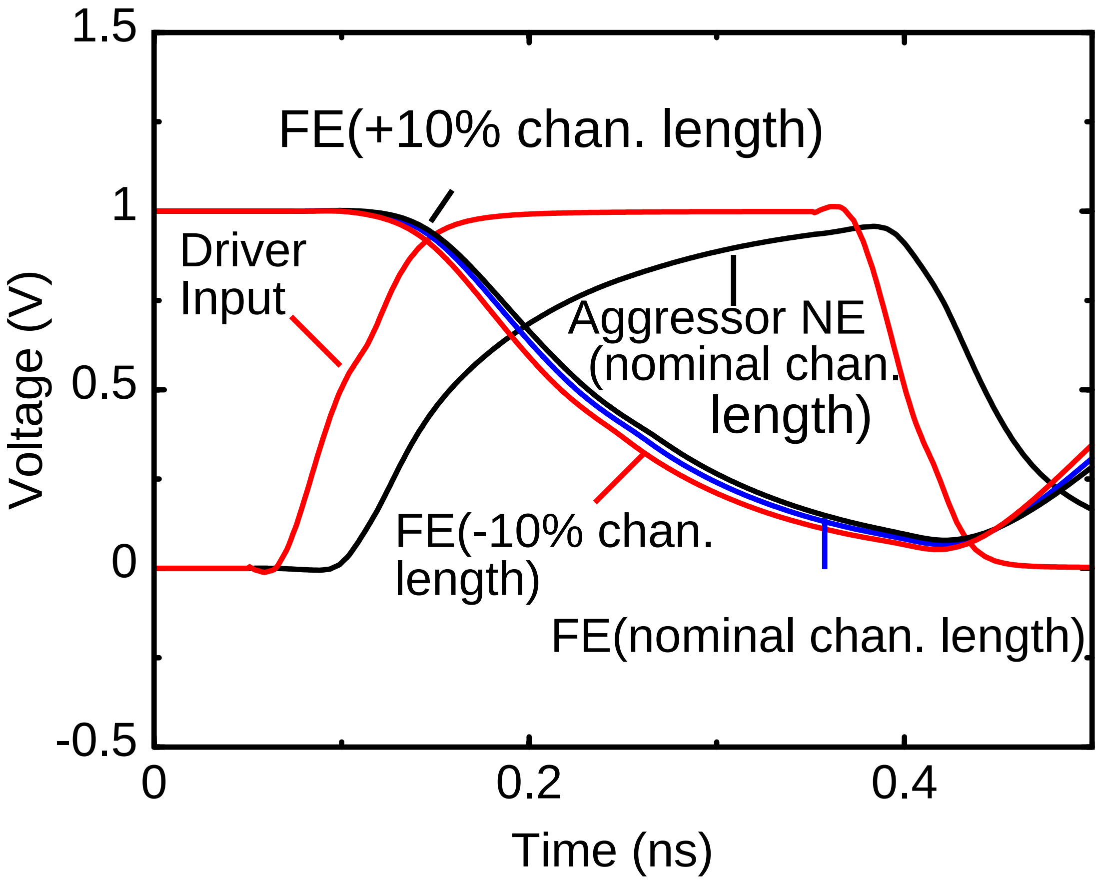
$$\text{Pushout} = \frac{(RLC\ \text{delay} - RC\ \text{delay})}{RC\ \text{delay}}$$

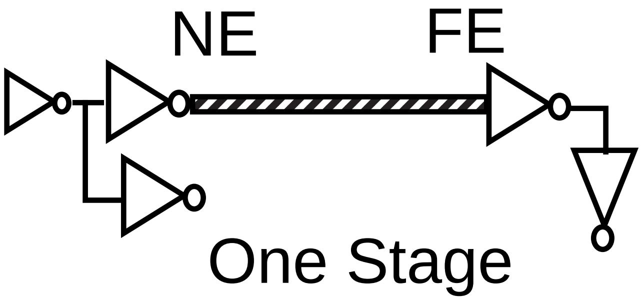
One Stage



Max timing pushout: 9.6%

Channel Length Variation Impact on Stage Delay for Bus Signals





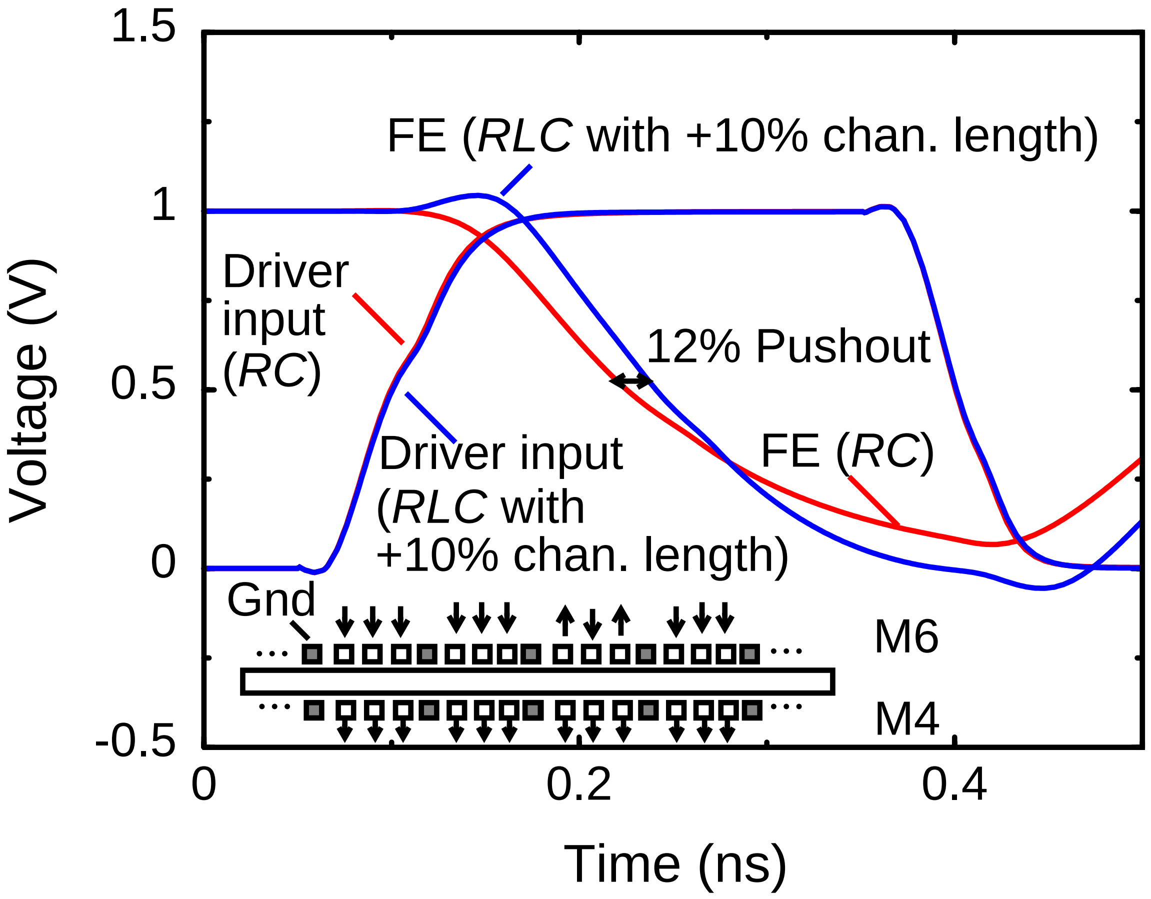
Stage Delay Variation: -5.97% to 4.8% vs. nominal case

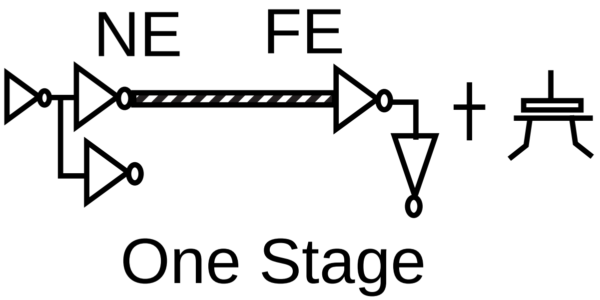
Device/Interconnect Variation Impact on Signal Timing and Noise

TABLE I IMPACTS FROM PROCESS VARIATIONS

	Device Variations			Interconnect Variations
Worst case delay and noise (*RC* Sim.)	Channel Length (-10% to +10%)	Threshold Voltage (-10% to +10%)	Dielectric Thickness (- 4% to +4%)	Metal/Dielectric Thickness (-10% to +10%)
Delay Pushout	-5.97% to 4.8%	-2.9% to 3.4%	0 to 1.6%	1.6% to 0.8%
Noise	1.1x to 1x	1x	1x	0.93x to 1.1x

Inductive Impact on Signal Delay with Channel Length Variation





Max timing pushout: 12%

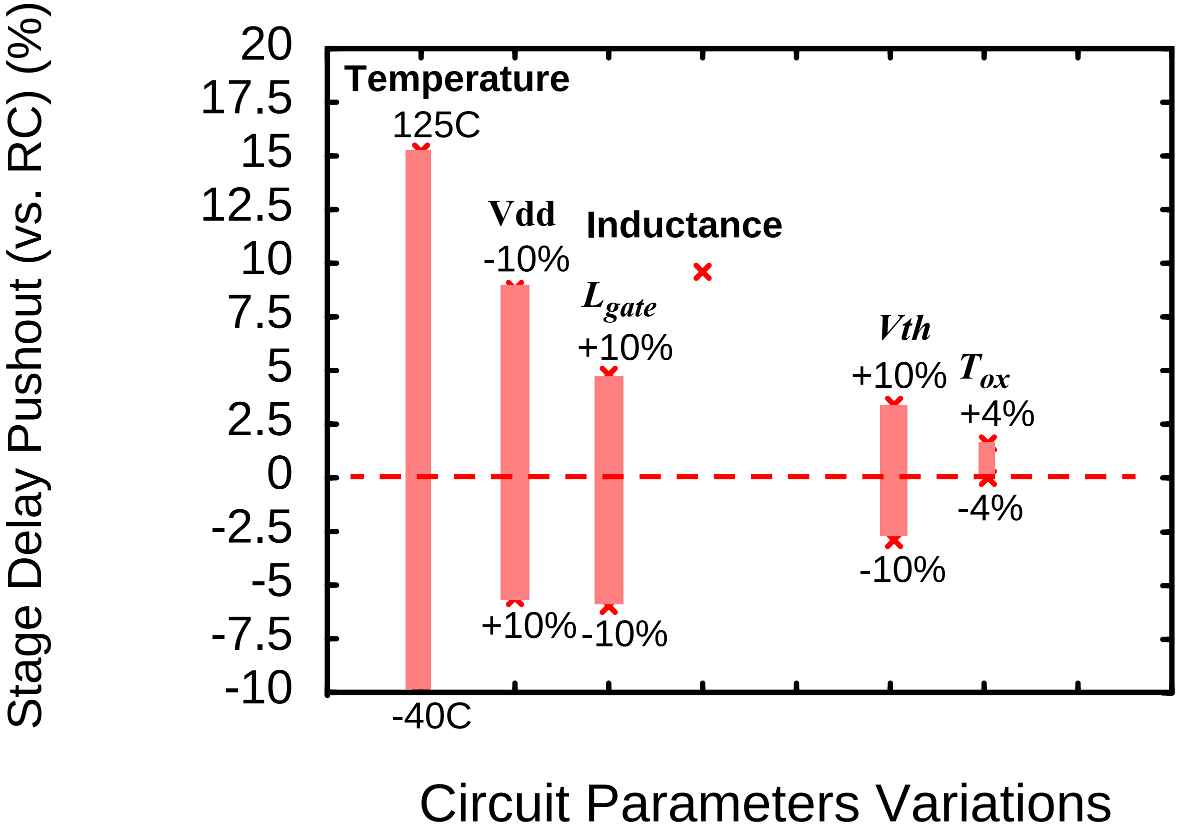
Inductance Impact with Process Variations

Worst case delay vs. *RC* Sim.	With Channel Length (-10% to 10%)	With Threshold Voltage (-10% to +10%)	With Intercon. Variations (-10% to +10%)
Delay Pushout	5.6% to 12%	6.4% to 12.8%	11.2% to 8.8%

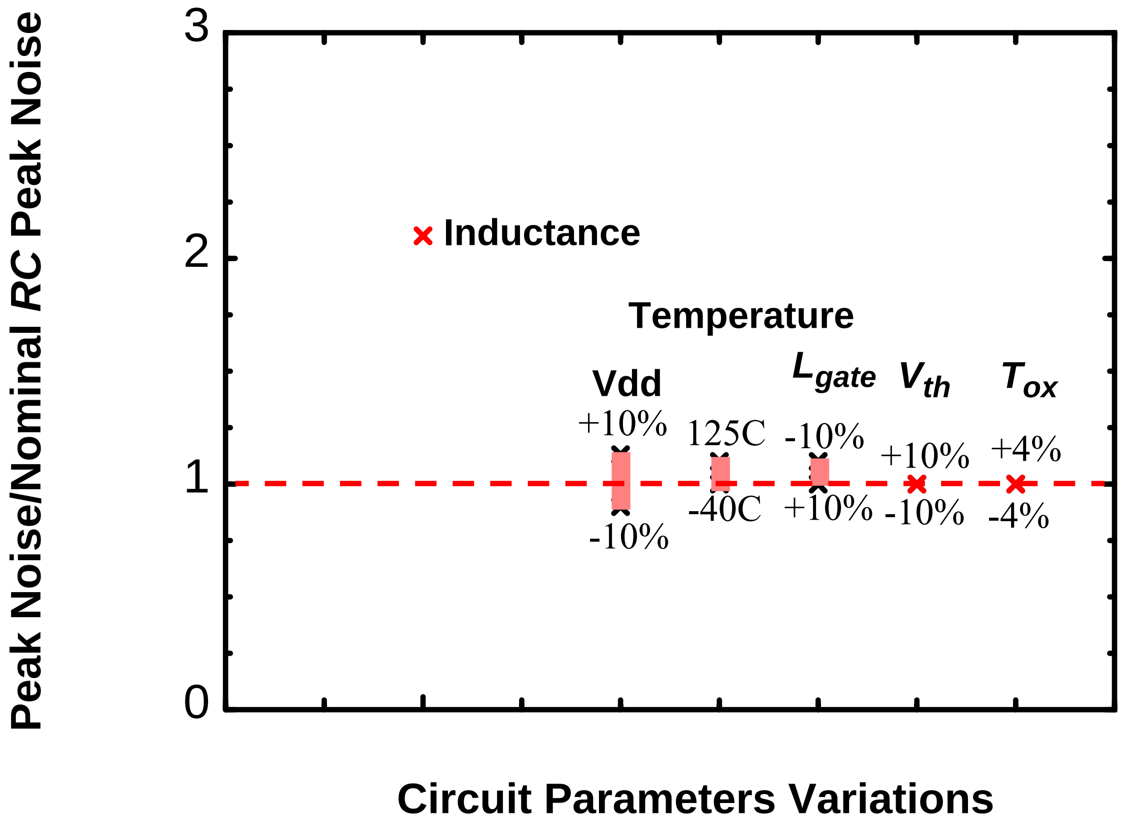
- ✧ The inductance push-out without process variations is 9.6%.

- Process variations add more pushout to inductive impact on timing, but not on noise.

Inductance, Process and Environment Impacts on Bus Timing



Inductance, Process and Environment Impacts on Bus Noise



Conclusions

- Simulation and analysis of VLSI bus interconnects in a 90 nm technology show:
  - Inductance impact on *max-timing:* ~9% more of *RC* stage delay; *Noise:* ~2x *RC* peak noise.
  - Process variations impact on *max-timing:* -5% to 5%; *Noise:* negligible impact.
  - Inductance and process variation impacts on *max-timing:* 5% to 12%. *Noise:* the same as the inductance impact.
- Ultra-high performance CPU designers need to examine the impacts in nano-meter designs.