# Simulation and Analysis of Inductive Impact on VLSI Interconnects in the Presence of Process Variations

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***Abstract* - On-chip inductance impact on signal integrity, complicated by process variations, becomes challenging for global interconnects in nanometer designs. Simulation and analysis of on-chip buses are presented for the impact of inductance in the presence of process variations. Results show that in 90nm technology there is significant inductive impact on max-timing (~ 9% push-out vs. *RC* delay) and noise (~ 2x *RC* noise). Device and interconnect variations add ~ 4% into *RLC* max-timing impact, while their impact on *RLC* signal noise is non-appreciable.**

## I. INTRODUCTION

When IC technology advances into the nanometer arena, interconnect signal integrity becomes more important, due to the smaller feature sizes and wire pitches. Devices with faster rise and fall times (typically tens of picoseconds) make global interconnects, such as clock nets, bus signals, power/ground grids, more vulnerable to *Ldi/dt* effects [1]-[6]. Meanwhile, nanometer process technologies have increased manufacturing and lithography-based distortions of wires, dielectrics, and devices. These distortions and variations include inter-die variations (e.g., dielectric layer thickness) and intra-die variations (e.g, device channel length), which require designers to understand and address the variations' impact on signal and power integrity [7][8].

At the 90 nm technology and beyond, smaller wire cross-sections increase wire resistance, which may alleviate self-inductance impact on timing; but smaller wire pitches increase mutual inductive coupling, and thus increase the impact on signal integrity. Bus signals can be impacted by inductance because they can potentially switch simultaneously. Fig. 1 plots the peak noise ratios of *RLC* and *RC* simulations for two typical buses in M6 and M4. The *RLC* noise can be as much as 2.1x *RC* noise for long wires, and 1.2x *RC* noise for short wires of 500 µm. This indicates that on-chip inductance impact on signal integrity is a serious concern for global interconnects at nanometer technologies. Device variations, such as channel length and threshold voltage variations, can be around ±10 % of target values, and result in transistor driving current and output resistance variations. Interconnect metal and dielectric layer thickness variations (about ±10 %) can result in wire capacitance, resistance and inductance variations. Designers need to understand quantitatively how much impact these parameter variations have on signal delay, noise, and power dissipation. In addition, it is important to analyze

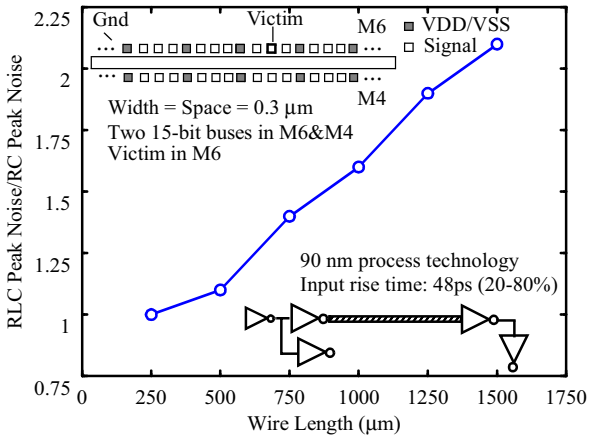


Fig. 1. The ratio of *RLC* peak noise over *RC* peak noise is greater than 1 for wires longer than 500 µm. Ignoring inductance in noise simulation underestimates signal noise.

collectively the inductance impact on signal integrity in the presence of process variations, because it becomes an important design issue in nanometer VLSI.

In this paper, inductance impact and process variation (device and interconnect) impact on max-timing delay and signal noise of on-chip bus signals are investigated separately in Sections II and III. In Section IV, inductance impact is studied together with process variations to identify the dominant factors in timing and noise impact. Conclusions are summarized in Section V.

## II. INDUCTANCE IMPACT ON BUS SIGNAL DELAY AND NOISE

### A. Simulation Setup

Consider two parallel 15-bit buses, one in M6 and one in M4, in 90 nm technology. Every three signals share two VDD/VSS as shown in Fig. 1. All wires are 1500 µm long. Such bus structures are typical in high performance CPU designs. Extra parallel quiet signal wires are added to mimic the real chip routing environment. Drivers are pre-buffered, and sized to be 20x in M6 and 16x in M4 in order to have reasonable rise/fall time for a GHz clock signal. RAPHAEL is used to extract capacitance, resistance and inductance of the interconnects. HSPICE is used in all circuit simulations to include any non-linear effect from driver devices.

A victim signal is in the center of the bus in M6. To simulate the worst case inductive impact on max-timing stage

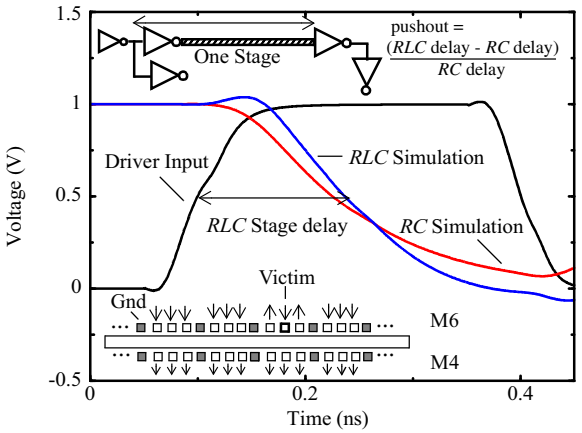


Fig. 2. The *RLC* stage delay is 137 ps while the *RC* stage delay is 125 ps - an inductive push-out of 9.6%.

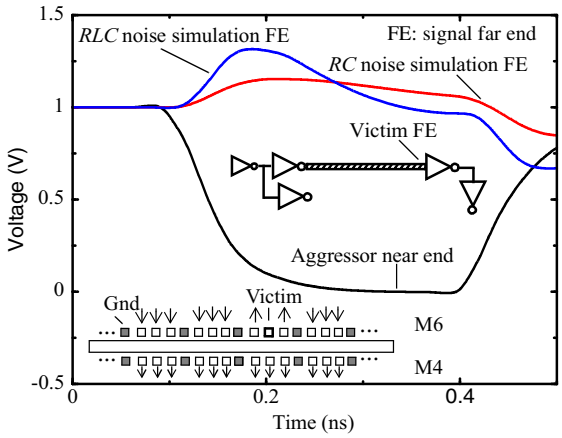


Fig. 3. The far-end (FE) *RC* noise is 0.15v, and the *RLC* FE noise is 0.31v The nearest two neighbor signals switch up and others switch down.

delay, the two nearest signals next to the victim (in M6) switch against the victim to maximize Miller effect of wire capacitance; while the rest of the signals switch with the victim to maximize inductive impact (shown by arrows in Fig.2). This is to see how much stage delay increases due to inductive impact against the worst case *RC* simulation. In terms of noise simulation, the victim wire keeps quiet, and all other switching activities are the same as the delay simulation. All the delay and noise are measured at the far end (FE) of the victim wire, i.e., at the input of the receiver. Propagation noise is not studied in this paper.

### *B. Inductance Impact on Signal Delay and Noise*

The circuit set up in the preceding sub-section is simulated both with inductance (*RLC*) and without inductance (*RC*). Stage delays are measured for the victim signal. Results show that *RLC* 50%-delay has 9.6% push-out compared to *RC* 50%-delay (See Fig. 2). Due to inductive impact, the victim signal starts to fall a bit later than it does in *RC* simulation, but has relatively faster fall time. To have accurate max-timing estimation, this extra inductive push-out needs to be taken into account in circuit design or the full-chip integration phase. Noise simulations show that *RLC* noise is 2.1x *RC* noise simulation (Fig. 3). The larger glitch and ringing signal may cause circuit functional failure, especially in dynamic circuits.

In order to avoid inductive delay and noise impact, analysis should be done in the early stages of design to create proper wire classes or to factor the impact into the design if they can not be avoided.

## III. PROCESS VARIATION IMPACT ON DELAY AND NOISE

Process variations have become an important design issue for nanometer circuits. Design for Manufacture (DFM) and Design for Yield (DFY) are now essential for ultra-high performance digital designs. It is necessary to understand the impact of process variations on signal integrity and power dissipation. In this section, device variations and interconnect variations are simulated without inductance to quantify these effects on signal max-timing delay and noise of *RC* circuits.

### *A. Device Variations (Channel Length, Threshold Voltage and Dielectric Layer Thickness)*

Device channel length ($L_{eff}$) variation has significant impact on drain current, which is a steep function of $L_{eff}$. The channel length variation can be as much as ±10 % of the final feature size [9]. Simulations of the max-timing delay show a range of -5.97% to 4.8% push-out variation due to channel length variation (See Fig. 4), which is a smaller impact than the inductive impact (9.6%). The non-symmetric delay variation is due to the fact that smaller channel length has much more affect on device driving current.

However, channel length variation has little impact on signal noise (1.1x - 1x). Threshold voltage can be varied due to Flat Band Voltage (VFB) change, which results in -2.9% to 3.4% max-timing push-out change. Dielectric layer thickness ($T_{ox}$) with ±4 % [9] variation has just a small impact on signal delay. Both threshold voltage and $T_{ox}$ variations have no significant impact on signal noise.

### *B. Interconnect Variations (Dielectric Layer Thickness and Metal Layer Thickness)*

Interconnects can have metal thickness and dielectric layer thickness variations. Metal thickness variation alters wire capacitance and resistance, thus *RC* delay and noise. Dielec-

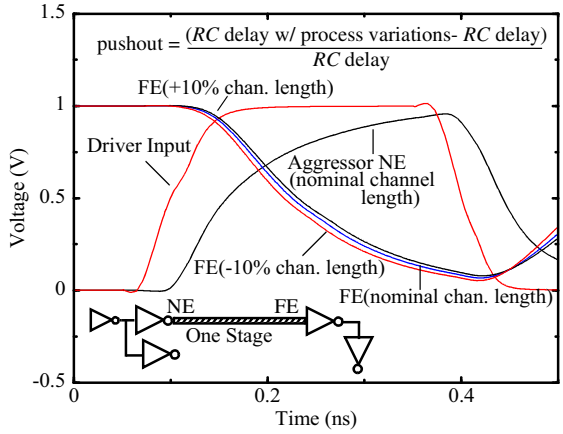


Fig. 4. A 10% decrease in channel length speeds up signals by 5.97% while 10% increase in channel length slows down the signals by 4.8%.

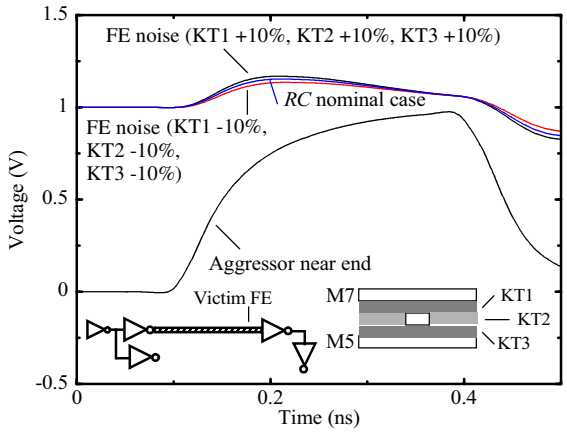


Fig. 5. Intra-layer coupling dominates the noise impact from interconnects variations.

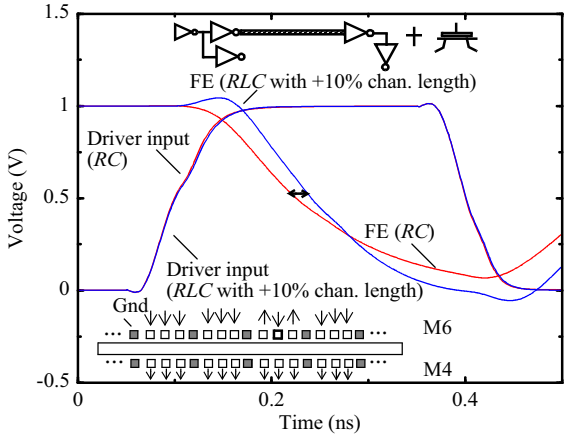


Fig. 6. *RLC* simulation with +10% channel length variation makes the max-timing pushout (12%) larger than the inductance impact (9.6%) and the channel length impact (4.8%), respectively.

tric layer thicknesses variation results in change of coupling capacitance. Metal thickness and dielectric layer thickness variations are typically ±10 %. Fig.5 presents a noise range of 1.1x to 0.93x *RC* noise, due to these interconnect variations. Both variations do not show strong impact on signal noise. The 10% increase in M6 thickness makes the same layer sidewall wire capacitance coupling stronger so that a bit larger noise is observed. The variation impact on delay depends on the dominant contribution from inter-layer or intra-layer capacitance. The 10% reduction in inter-layer dielectric thickness increases inter-layer capacitance, and slows down the max-timing delay by 1.6%. Table I lists the impacts on delay and noise from both device and interconnect variations.

TABLE I IMPACTS FROM PROCESS VARIATIONS

| | Device Variations | | | Interconnect Variations |
|---|---|---|---|---|
| Worst case delay and noise (*RC* Sim.) | Channel Length (-10% to +10%) | Threshold Voltage (-10% to +10%) | Dielectric Thickness (- 4% to +4%) | Metal/Dielectric Thickness (-10% to +10%) |
| Delay Push-out | -5.97% to 4.8% | -2.9% to 3.4% | 0 to 1.6% | 1.6% to 0.8% |
| Noise | 1.1x to 1x | 1x | 1x | 0.93x to 1.1x |

## IV. INDUCTANCE IMPACT IN THE PRESENCE OF PROCESS VARIATIONS

Inductance and process variations co-exit in real designs. To quantify inductance impact in the presence of process variations, and identify the dominant factor in the total impact is beneficial to chip designers. In this section, simulation of collective effects from both inductance and process variations are presented. Other impacts from environmental variations, namely supply voltage and temperature, are also included.

### *A. Inductance Impact with Process Variations*

As it is seen, inductance impact is larger than process variation impact for max-timing and noise. Inductance impact can become worse or become alleviated by process variations. For example, the inductance impact and a +10% increase of channel length yields 12% max-timing push-out, which is larger than the pure inductance push-out (9.6%), and the pure +10% channel-length-increase push-out (4.8%). See Fig. 6. However, collective impact is smaller than the sum of the two individual push-outs. If channel length varies to -10% smaller, inductive impact is alleviated by short channel effect, and push-out becomes 5.6%. It is worth pointing out that the increased current driving force (larger *di/dt*) from shorter channels does not make inductive effect more severe, because capacitive effect dominates the max-timing stage delay in this switching condition (maximum Miller effect).

Table II lists the inductance impact on delay in the presence of device variations and interconnect variations. One can see that channel length and threshold voltage may add more impact to inductance impact; while interconnects and dielectric layer thicknesses variations change the inductance impact less, because inductance is a weak function of wire geometry. In addition, all process variations do not add more noise to *RLC* noise (e.g., 1.03x for -10% channel length change).

TABLE II INDUCTANCE IMPACT WITH PROCESS VARIATOINS*

| Worst case delay vs. *RC* Sim. | With Channel Length (-10% to 10%) | With Threshold Voltage (-10% to +10%) | With Intercon. Variations (-10% to +10%) |
|---|---|---|---|
| Delay Pushout | 5.6% to 12% | 6.4% to 12.8% | 11.2% to 8.8% |

* The *RLC* push-out without process variations is 9.6%.

### *B. Delay, Noise and Power Consumption Variations Due to Inductance Effect, Process and Environmental Variations*

Process variations manifest themselves as the uncertainties of circuit performance, such as delay, noise and power consumption. Environmental variations, such as supply voltage and temperature variations, also impact circuit delay and noise. Some of these variations can come from inductance effect - for example, voltage variation may be due to the on-chip power grid and packaging inductance effect. Fig. 7 plots the variation ranges of the stage delay push-out vs. *RC* simu-

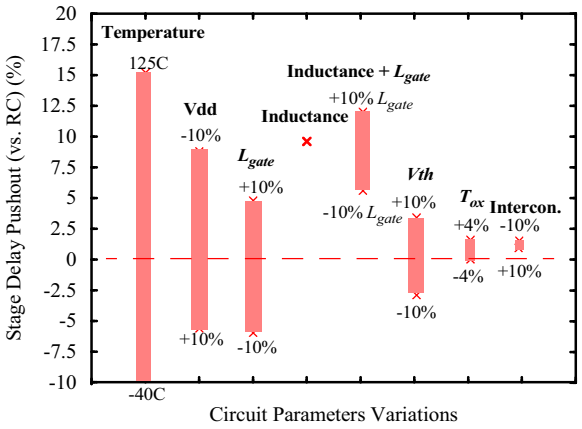


Fig. 7. Max-timing stage delay variations due to inductance, and process and environmental variations.

lation (used as the nominal case) of the same bus circuit. Besides inductance and channel length impact, temperature and supply voltage create large delay uncertainties. Fig. 8 shows the ratios of peak noise over *RC* peak noise. Inductance with channel length variation makes signal *RLC* noise even larger. The inductive waveform is similar to the one shown in Fig. 3 with ringing effect. Smaller channel lengths speed up the circuit, but create more noise. Other device, interconnects and environment variations have limited impact on peak noise values. In Fig. 9, power consumption is also investigated in terms of peak power in the bus structure during one clock cycle. As expected, supply voltage variation makes the largest peak power fluctuation. Threshold voltage and channel length variations also show appreciable power fluctuations, mostly due to drain current variation. Since this is an interconnect dominated circuit, temperature variation has limited impact on power consumption[1]. In Figs. 7 - 9, performance variations are sorted based on the variation ranges.

## V. CONCLUSIONS

Simulation and analysis of VLSI interconnects in 90 nm technology are presented, which shows inductance impact in the presence of process and environmental variations. In nanometer designs, inductance has significant impact on max-

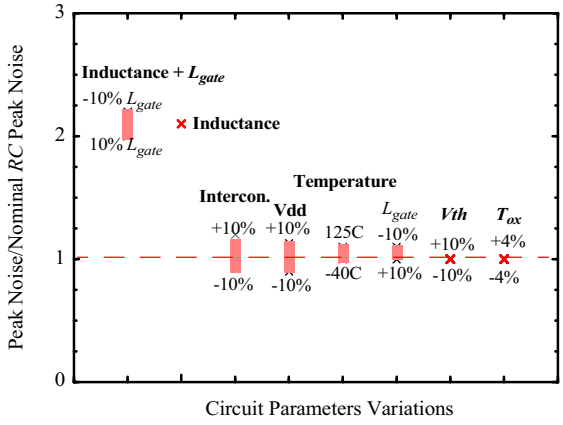


Fig. 8. Noise impact ranges due to inductance, and process and environmental variations.

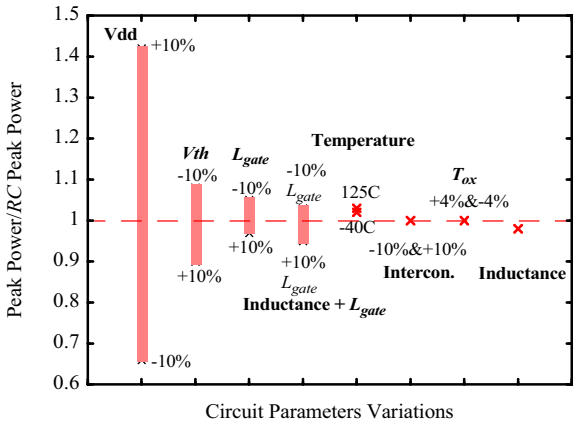


Fig. 9. Peak power variations due to inductance, and process and environmental variations. For average power, the three largest impacts are from *Vdd*, temperature and threshold voltage variations.

timing and noise of bus signals, which is around 9% for max-timing push-out (against *RC* delay) and 2x *RC* noise for peak noise. Process variations, such as device channel length and threshold voltage, also show about -5% to 5% push-out impact on max-timing, but negligible impact on noise. Collective impact of inductance and process variations (e.g., ±10 % channel length variations) is about 5% to 12% for max-timing, but does not show much noise difference compared to *RLC* simulations. Ultra-high performance CPU designers need to carefully examine these impacts on delay, noise and power variations in nanometer technologies.

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[1] Device's power dissipation has a strong dependency on temperature. In 90nm, for example, a 20x inverter at 125C shows 300x leakage power dissipation of the same inverter at -40C.