A Fast 3-D Modeling Approach to Electrical Parameters Extraction of Bonding Wires for RF Circuits

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***Abstract*—Bonding wires are extensively used in integrated circuit (IC) packaging and circuit design in RF applications. An approach to fast three-dimensional (3-D) modeling of the geometry for bonding wires in RF circuits and packages is demonstrated. The geometry can readily be used to extract electrical parameters such as inductance and capacitance. An equivalent circuit is presented to model the frequency response of bonding wires. To verify simulation accuracy, test structures have been made and measured. Excellent agreement between simulated and measured data is achieved for frequencies up to 10 GHz. The model is well suited for the design and analysis of circuits for cellular phone communication (i.e., order 2 GHz) and future wireless communication (i.e., order 5 GHz).**

***Index Terms*—Geometric modeling, IC packaging, integrated circuit modeling, RF circuit, semiconductor device bonding.**

I. Introduction

BECAUSE of growing concerns in high frequency design, consideration of parasitic effects for the bonding wires is essential in integrated circuit (IC) packaging of radio frequency (RF) and deep submicron high speed very large scale integrated (VLSI) circuits. As the frequency moves above several GHz, the parasitics caused by bonding wires, mainly inductance and capacitance, can no longer be ignored and require careful modeling. To predict the performance of packaged RF power devices, a compact model, including bonding wires, is desirable for circuit simulation. Bonding wires are sometimes also used in matching networks in RF ICs. Typically, to achieve good matching, adjustment of the bonding wires is required through empirical effort, with little or no help from simulation. Moreover, bonding wires are used in implementing high quality factor (Q) inductors as part of functional design of tuning networks in RF circuits, vis a vis on-chip spiral inductors. Therefore, for these applications, it is necessary that the electrical parameters of bonding wires be correctly extracted and their electrical performance be modeled accurately.

In order to model package parasitics, simulation of the intrinsic device is compared to the measured S-parameters of a packaged device [1]. This modeling approach relies on the accuracy of the intrinsic device model and requires measurement for individual devices. For complex 3-D geometries, a new physical method is needed to link extraction and the modeling process. A method based on bonding wire geometries has been previously reported in [2]. However, it involves manual measurement of the wire length; the shape (curvature) of the wires has not been sufficiently considered. Analytical formulae for straight wires are used to estimate the inductance. Since manual measurement is error prone and 3-D geometry information is not completely captured, accuracy of this approach is limited. In [3] analytical formulae are used to calculate the bonding wire's self and mutual inductance. But these equations were derived only for one specific geometry, shape or curvature of the wires—the methodology is not suited to generalized bonding wire configurations. For general 3-D geometries, automation would be preferred.

As circuits become more complex, the package and bonding wires become more complex as well. Fig. 1 shows an SEM photo of an RF power transistor; complicated geometry of the package must be taken into account. Capture of sufficient bonding wire information depends on accuracy and automation of the 3-D geometry modeling process. In this paper, a fast 3-D modeling approach is presented, which extracts the geometry from SEM photos, ultimately leading to extraction of electrical parameters. The input files for the field solvers, such as FASTHENRY [4] and FASTCAP [5], can be automatically generated based on this geometry. Electrical parameters (inductance, resistance and capacitance) and equivalent circuits are then obtained for circuit analysis. A carefully designed test structure has been fabricated and measured. The simulation results show excellent agreement with the measured data. The software is written in the Java programming language, offering potential use in remote and distributed design environments.

The paper is organized as follows. In Section II, a new geometry modeling method is introduced. In Section III, the design of test structures is detailed along with a simple equivalent circuit for the bonding wires. In Section IV, the simulation and measurement results for the test structures are compared and finally conclusions are summarized in Section V.

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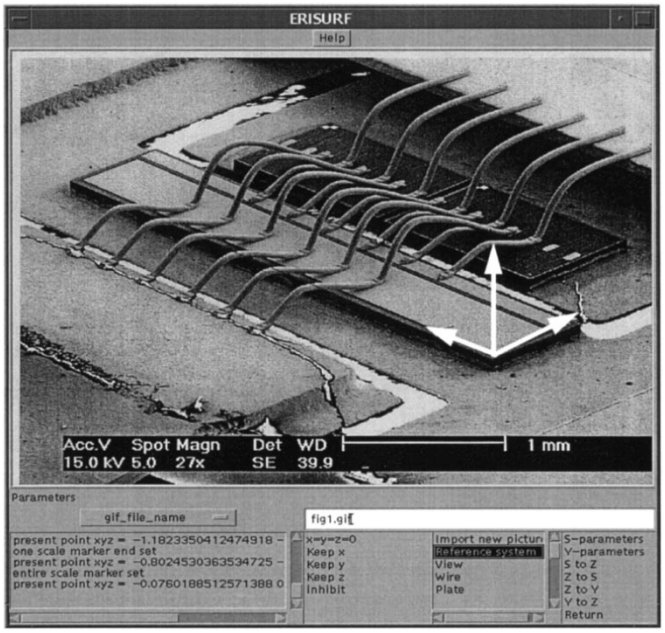


Fig. 1. A program is developed to capture the 3-D bonding wire geometry and to generate input files for field solvers.

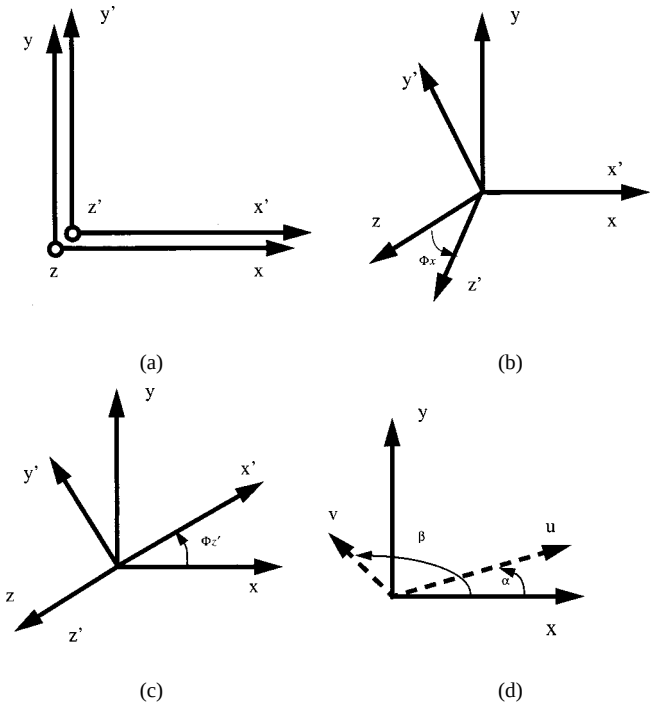


Fig. 2. Translation of world coordinate system and reference coordinate system. (a) World coordinate system and reference coordinate system are aligned. (b) Rotation around x. (c) Rotation around z'. (d) Projections of x' and y' on xy plane, u and v are their projections.

II. A Novel Geometry Extraction Method

Physically-based simulation of interconnects is possible only when detailed knowledge of 3-D geometry is available. In many cases the structures can be defined from planes parallel to the coordinate planes. Solid modeling tools have become popular in defining such geometries. The most common way of geometry capturing is based on projections of 2D objects from respective coordinate planes (xy, yz, and zx). If an object's projections to the coordinate planes are known, a 3-D geometry of the object can be constructed. This makes it possible to construct 3-D geometries, using conventional mechanical engineering drawing methodology.

To obtain the geometry of the wires, a new extraction method is developed. Even though shape can be controlled by the bonding machines with high accuracy (and reproducibility), it is difficult to predict the shape of bonding wires in advance. SEM photos have a large depth of focus and are used to capture the shape of wires. Complete 3-D information can be obtained from several photos with known viewing locations and angles. In practice, however, it is sufficient to use a single properly positioned photo and to make the extraction unique by adding limited assumptions about the geometry. Since SEM photos are portable, using electronic transport formats, this geometry modeling method can be exploited in modeling a variety of wire shapes as long as we have the SEM photos.

A program has been written that can display the SEM photo, including the definition of a reference coordinate system. A simplified drawing is superimposed on the photo interactively, and by moving the cursor on the screen the necessary depth information is captured which emulates 3-D movements and allows construction of the 3-D geometry.

The 3-D space and objects are described in a world coordinate system and a user defined reference coordinate system. The reference coordinate system can be considered as a result of two sequential rotations of the world coordinate system. The relationship between the two systems is described using transformation (rotation) matrices and one scaling matrix. The 3-D space is described in the world coordinate (x, y, z). On the screen, it is assumed that the x axis is always pointing to right, the y axis is always upright and the z axis points toward the user. The objects (bonding wires) are described in a user-defined reference system (x', y', z'). Fig. 2(a) shows the aligned world and reference coordinate systems. By assuming that the z' axis projection on screen—the xy plane—is always parallel with the y axis (i.e., upright on screen), we do not have rotation around the y axis. To transform the xyz system to the $x'y'z'$ system, we only need to first rotate the xyz system around the x axis and secondly, rotate around the new resulting z' axis. The rotation around x and the new z' axis are plotted in Fig. 2(b) and (c) and the corresponding matrices can be obtained [6].

Users define the reference system by actually specifying the x' and y' axes projections on the screen in the xy plane. This is usually done by putting the origin on the corner of a device and creating two projections along two selected edges of the device. As soon as the projections are drawn, the angle, α, between the x axis and the projection of x', and the angle, β, between the x axis and projection of y' are known [see Fig. 2(d)]. The two rotation matrices can be used to derive the relationships between Φ_x, $\Phi_{z'}$, α and β based on the fact that (A) the x axis rotation yields the x' axis, the y axis rotation determines the y' axis, and (B) the x' and y' axes can be represented by their projections on the xy plane

$$\tan\alpha = \frac{q_x}{q_y} \tag{1}$$

$$\tan\beta = \frac{r_x}{r_y} \tag{2}$$

where q_x and q_y are the two scalars representing the x' axis projection on the screen (xy plane)—in other words, vector

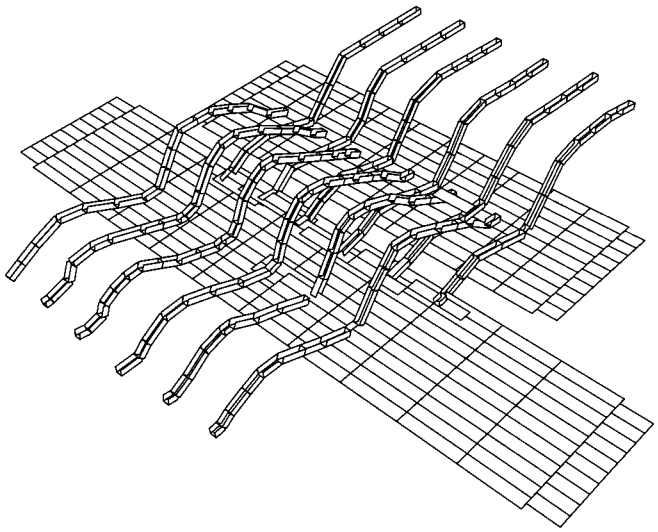


Fig. 3. Extracted 3-D geometry model from the Java program for further electrical simulation.

$\mathbf{u} = q_x\mathbf{x} + q_y\mathbf{y}$. Likewise, r_x and r_y are the components that represent the y' axis projection on the screen (xy plane). Vector $\mathbf{v} = r_x\mathbf{x} + r_y\mathbf{y}$.

With limited assumptions, once we define the $x'y'$ projections on the screen, a reference system is established which in turn defines its transformations with the world coordinate system. Whatever we draw on the screen can be converted to this system through two rotation matrices.

Programmed in Java, the tool can be run across a network (or internet) using a Virtual Java Machine (VJM) available in Netscape and Internet Explorer on most computer systems. The program automatically creates input files for the 3-D electromagnetic simulators such as FASTHENRY [4] and FASTCAP [5] to extract the electrical parameters for the structure. Fig. 1 shows the user interface of the software used to capture 3-D geometry, and the extracted drawing is shown in Fig. 3. The axes of the reference system can be seen at the corner of the capacitor's plate. Users can easily choose functions from the menu shown below the SEM photo (i.e., Fig. 1).

To check the accuracy of the geometry modeling method, SEM photos are taken from different view angles (e.g., 180^o rotation). Geometries are extracted from one SEM photo. If the extracted geometries are rotated 180^o, to fit another SEM photo taken after 180^o rotation, the extracted geometries fit the second SEM photo reasonably well as shown in Fig. 4. The primary error comes from neglecting the perspective factor which is usually small. The comparisons of the measurement and simulation of test structures in Section IV further confirm the accuracy of the geometry extraction. One limit of this method could be the fact that geometry distortion will occur if the SEM photo is taken from an improper viewing angle.

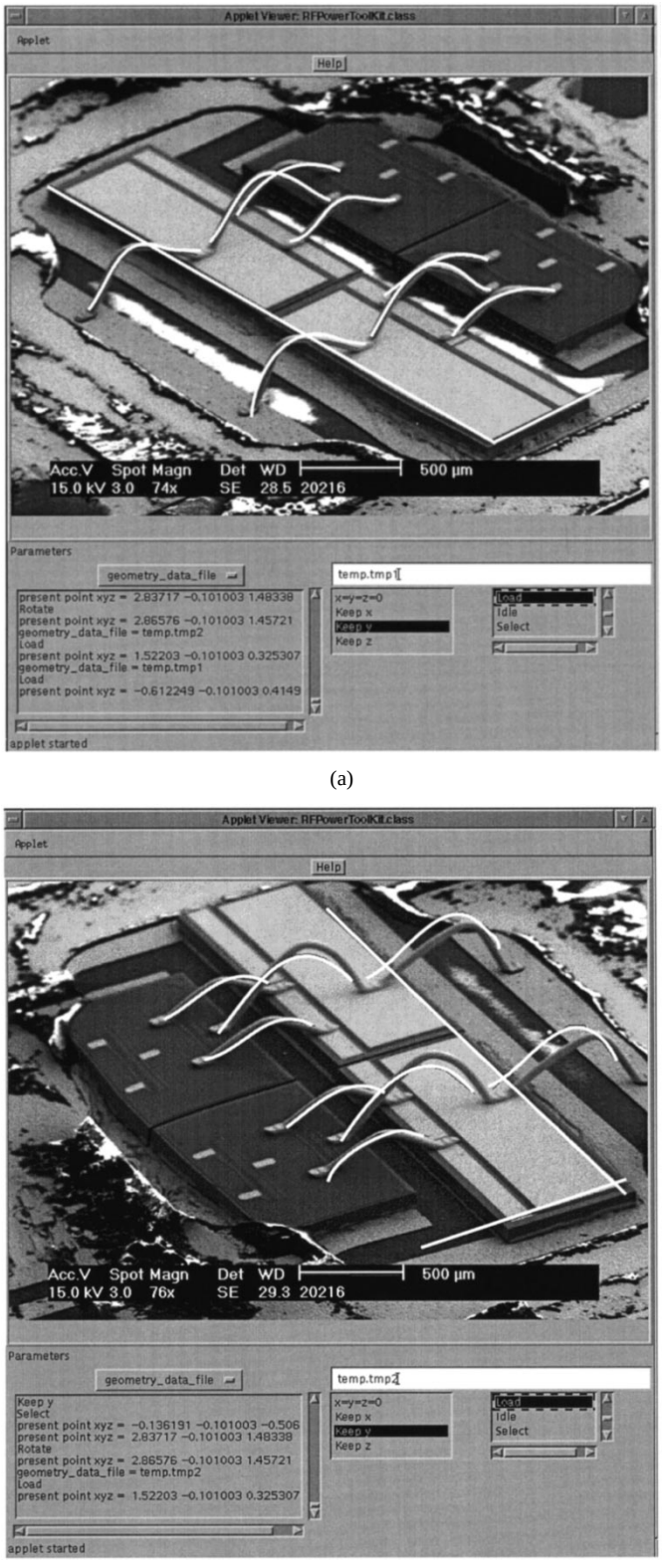


Fig. 4. (a) Traces extracted from one angle. (b) Traces extracted from Fig. 4(a) is rotated 180^o and fit the new SEM photo taken after 180^o view angle rotation.

III. Design of Test Structure and Model Parameter Extraction

A. Test Structures and Measurement

The accurate measurement of bonding wires for an entire RF circuit is difficult. Parasitics of the chip and coupling from other parts of the circuit are problematic, especially at high frequencies (GHz). To verify the accuracy of the modeling approach, test structures have been designed, targeted to enhance measurements accuracy. Two SEM photos of three test structures

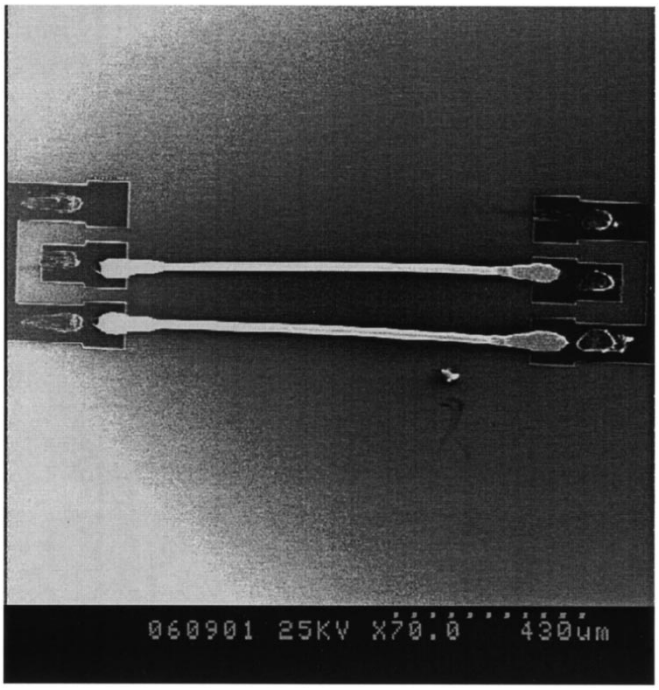


Fig. 5. SEM photo for stra21 test structure.

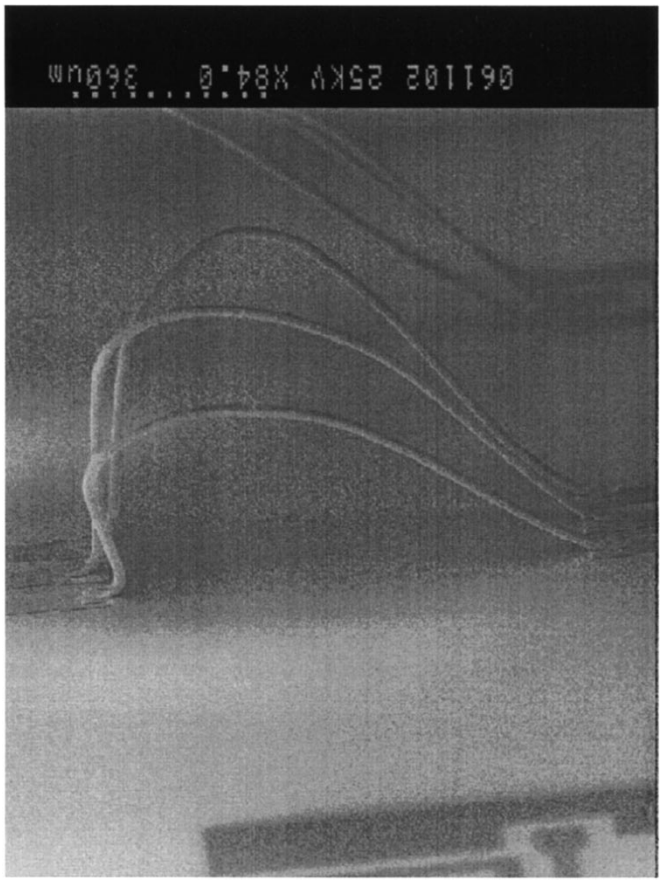


Fig. 6. SEM photo for curv31 test structure.

are shown in Figs. 5 and 6, which are referred as stra21 (two straight wires, each being 1 mm long) and curv31 (three curved wires, each being approximately 1 mm long), respectively. The other is curv22 (two curved wires, each being approximately 2 mm long). The bonding wires are made of 99.99% gold with a diameter of 0.7 mil (17.78 μm).

On-wafer testing was performed with a HP8720B Network Analyzer and Cascade Microtech coplanar ground-signal-ground (GSG) probes. The measurement setup is calibrated using the Cascade Impedance Standard Substrate (ISS). The shunt parasitics of the test structure were de-embedded using open calibration structures fabricated next to the device under test (DUT) [8]–[10]. An equivalent circuit for the two-port measurement set-up is shown in Fig. 7. Since the ground paths for return current appears in series with the DUT, the parasitic inductance and resistance of these ground paths should be made insignificant compared to the DUT impedance. Since the on-chip aluminum interconnect is much more resistive than the gold wire, the bonding wire's resistance will be totally masked by the ground path resistance. To overcome this problem, the return path is implemented using bonding wires as well in the test structures. As a result, the parasitics due to the return interconnect to the ground pad is completely avoided. During these measurements, the backside of the silicon substrate was grounded through the testing chuck. Furthermore, the parasitics of the probe pads were de-embedded using open dummy structures.

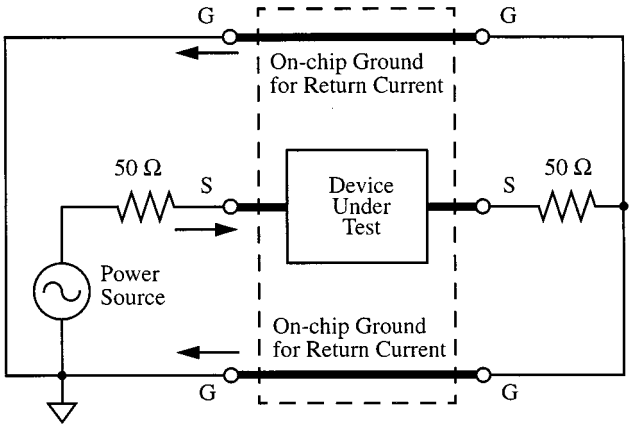


Fig. 7. An equivalent circuit of a typical on-wafer measurement set-up to illustrate the series ground path parasitics.

B. Equivalent Circuit for the Bonding Wires

Input to the field solvers (i.e., FASTHENRY and FASTCAP) can be generated automatically based on the constructed geometries. Self and mutual inductances and resistances of the bonding wires are then extracted using FASTHENRY. To accurately model the skin effect, the resistance is calculated considering the frequency dependence. A similar dependence is used for the inductance. It is generally assumed that parasitic capacitance is negligible for bonding wires because of its small diameter. However, if bonding wires are used in higher frequency applications (above 6 GHz), the capacitance of the bonding wires to the substrate and the mutual capacitances of bonding wires must be considered for accurate modeling.

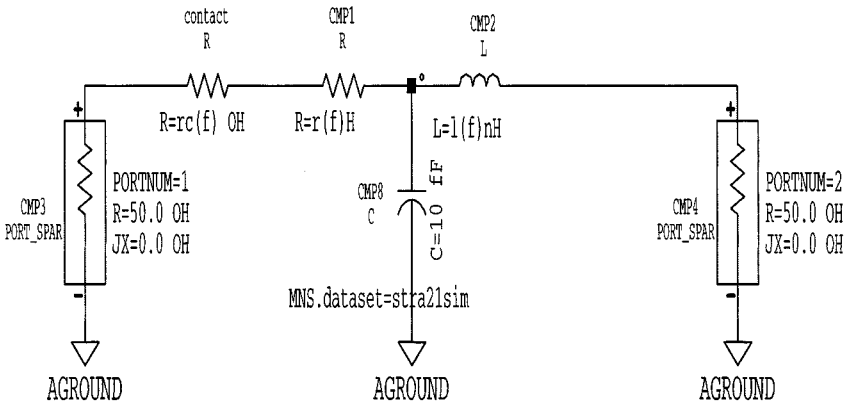


Fig. 8. Equivalent circuit for the bonding wire.

Meshed input to FASTCAP is also supported and can be used to generate capacitance models as needed.

In addition, in order to compare the simulation results and measurement data, contact impedance of the test probes and the bonding wire's solder balls, which are frequency dependent, should be included in the model since it is extremely difficult to mask or decouple contact resistance in the measurements. The resistance of a straight bonding wire can be estimated as follows [7].

$$R \simeq \frac{l}{2\pi r \delta \sigma} \tag{3}$$

where δ is the skin depth and σ is the conductivity. For gold at 293 K, σ is 2.22 $\mu\Omega$-cm at high frequencies [11]. r is the radius of the wire and l is its length. R is thus frequency dependent, owing to δ where for gold [11]:

$$\delta = \frac{0.075}{\sqrt{f}} \tag{4}$$

and f is frequency. The frequency dependent contact resistance can be deduced from the measured data by subtracting the resistance as expressed in (3) at various frequencies. Regression data fitting is used to find an analytical expression for the contact resistance. For example, the contact resistance for the stra21 and curv22 test structure can be found to be

$$R_{\text{contact}}\,(\Omega) = -0.0053f^3 + 0.3888f^2 - 1.4735f + 1.0816 \tag{5}$$

To capture the skin effect in simulation, wires are divided into a number of filaments. Each filament's height should be smaller than the skin depth which is 2.37 μm at 1 GHz and varies according to (4) for gold material. In our case, eight filaments are enough to accommodate the skin effect. More filaments entail increased computational complexity. The equivalent circuit for the entire test setup, including bonding wires, is shown in Fig. 8; the bonding wire's inductance, resistance, capacitance and contact resistance are all considered. Input and output ports are added for completeness.

IV. Comparison of Simulation and Measurement Results

To avoid the error induced by converting (via processing) the measurement data, S-parameters of the generated models were

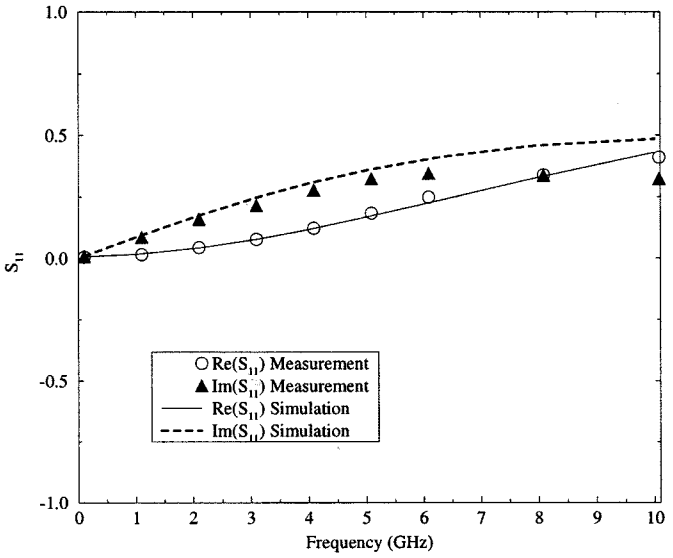


Fig. 9. S_{11} for the stra21 structure: data points are from measurement and lines from simulation without capacitance included.

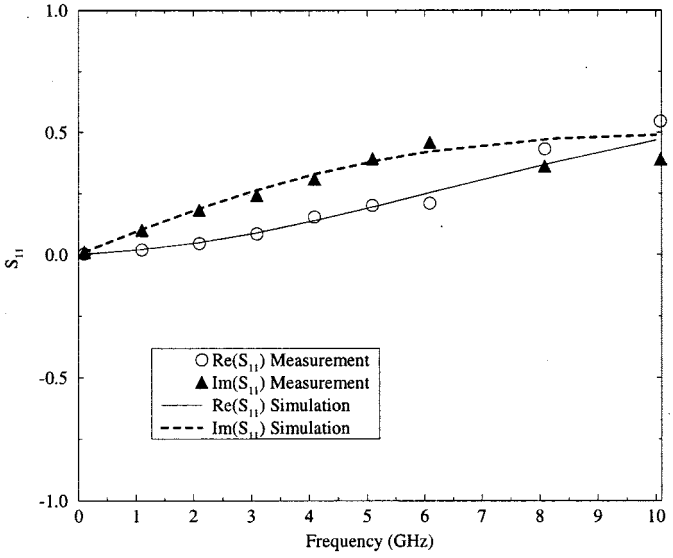
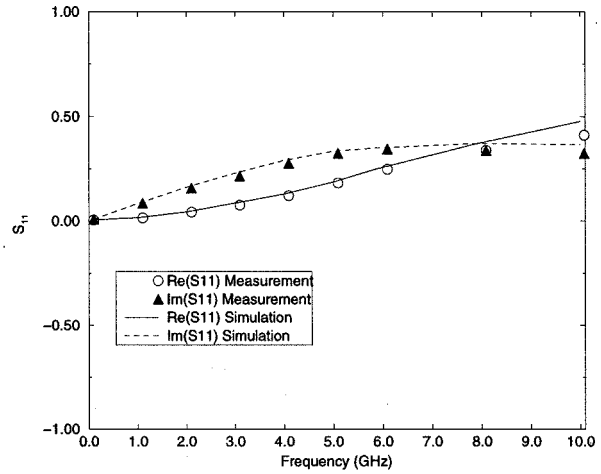
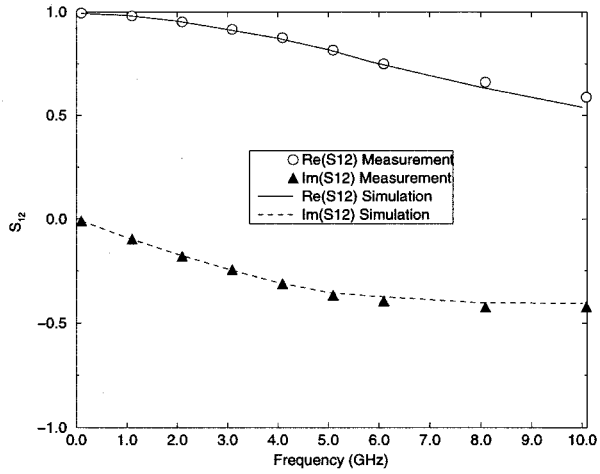


Fig. 10. S_{11} for the curv31 structure without capacitance included.

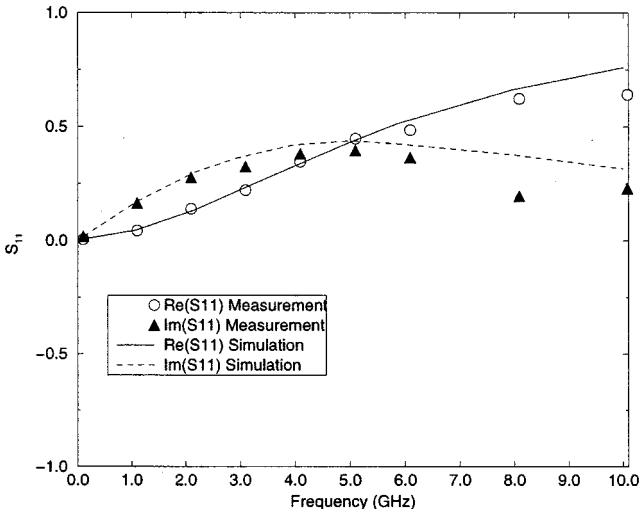


(a)

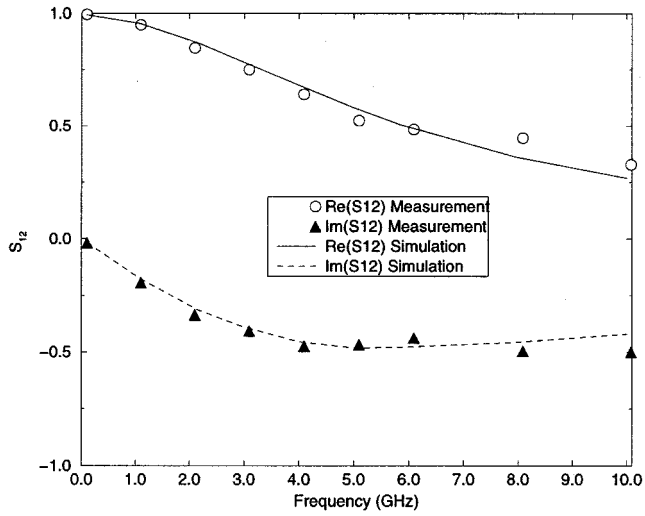


(b)

Fig. 11. S-parameters comparison for stra21 structure. (a) S_{11} for the stra21 structure: data points are from measurement and lines from simulation with capacitance included. (b) S_{12} for the stra21 structure with capacitance included.



(a)

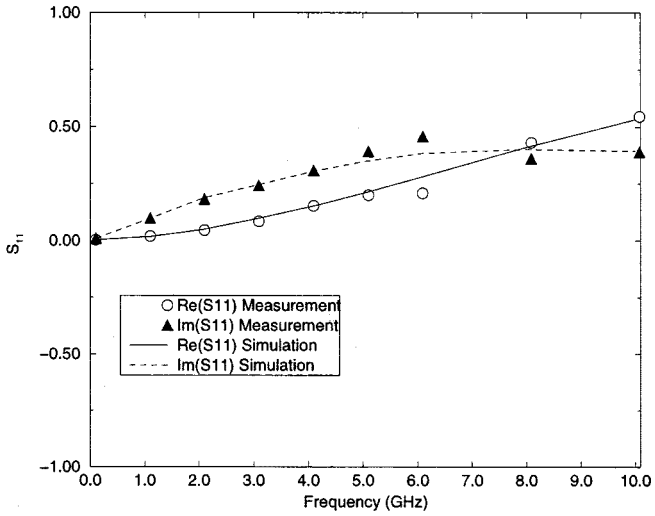


(b)

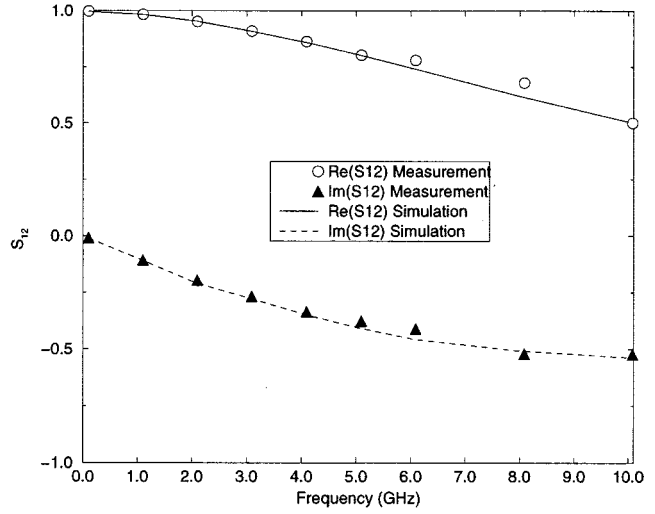
Fig. 12. S-parameters comparison for curv22 structure. (a) S_{11} for the curv22 structure with capacitance included. (b) S_{12} for the curv22 structure with capacitance included.

computed using HP-MDS or HSPICE and then compared directly to the measured S-parameters. In order to compare not only the magnitudes, but also their phases, real and imaginary parts are plotted and compared. Only comparing magnitudes of the S-parameters can lead to unconvincing conclusions about the phase, which is an equally important parameter. Figs. 9–10 show the comparison between the simulation and measurement of S_{11} of two different structures when only inductance and resistance are extracted. Since bonding wires are usually used around several GHz (where radiation is not a problem), the results are plotted up to 10 GHz. The agreement is excellent up to 5–6 GHz. From the figures, we can see that the real part of S_{11} increases as frequency increases, which is related to the resistance increase at higher frequencies. The imaginary part of the measurement, which is related to the reactance part, also increases up to 6 GHz and then decreases as frequency goes higher. While this differs from simulations at higher frequencies, the capacitance of the bonding wire brings down the S_{11} values. To model higher frequency bonding wires, capacitance should be taken into account. Figs. 11–13 show S_{11} and S_{12} comparisons of all the three structures with the bonding wire capacitances represented by the current model formulation. The agreement is then extended to 10 GHz, substantiating that parasitic capacitance plays an important role at higher frequencies. The relative simulation errors of the S-parameters usually are smaller than 5%.

Inductance values are also compared between simulations and measurements at a specific frequency based on the equivalent circuit which is shown in Fig. 8. S-parameters from measurement can be converted to Y parameters and the inductance of the wire can be extracted from Y_{11} of the test structure. Table I shows the inductance from the simulations and measurements at 1.1 GHz. The simulation errors are rather small (i.e., below 4%). RF designers usually use approximate analytical formulae for straight wires to estimate bonding wire inductance L and



(a)



(b)

Fig. 13. S-parameters comparison for curv31 structure. (a) S_{11} for the curv31 structure with capacitance included. (b) S_{12} for the curv31 structure with capacitance included.

mutual inductance M as shown below [7]

$$L \simeq \left[\frac{\mu_0}{2\pi}\right] \leq \left[\ln\left(\frac{2l}{r}\right) - 0.75\right] \tag{6}$$

$$M \simeq \left[\frac{\mu_0}{2\pi}\right] \leq \left[\ln\left(\frac{2l}{D}\right) - 1 + \frac{D}{l}\right] \tag{7}$$

where μ_0 is the permeability in free space, l the wire length, r the radius of the wire, and D the distance between two wires. The loop inductance of a two-wire structure can be estimated as

$$L_{\text{loop}} = L_1 + L_2 - 2M \tag{8}$$

where L_1 and L_2 are the wire's self inductance. Results from analytical calculations for straight lines of bonding wires are also included for comparison. However, these formulae only apply for straight wires which is usually not consistent with the shape

TABLE I
INDUCTANCE COMPARISON AT 1.1 GHz (nH)

	Stra21	Curv22	Curv31
Measurement	1.377	2.802	1.546
Simulation	1.414	2.694	1.533
Simulation Error	2.69%	3.85%	0.84%
Analytical Calculation	1.233	N/A	N/A
Calculation Error	10.5%	N/A	N/A

TABLE II
INDUCTANCE COMPARISON FOR THREE DIFFERENT WIRE SHAPES WITH SAME WIRE LENGTH OF 1.515 mm

	Straight wire	Curved wire		Π shape wire	
	Simulation result (nH)	Simulation result (nH)	Error if straight wire used	Simulation result (nH)	Error if straight wire used
100 MHz	1.192	1.011	17.9%	0.814	46.44%
1 GHz	1.160	0.979	18.49%	0.783	48.15%
10 GHz	1.152	0.970	18.76%	0.775	48.65%

TABLE III
MUTUAL INDUCTANCE SIMULATION COMPARISON FOR THREE DIFFERENT WIRE SHAPES WITH SAME WIRE LENGTH OF 1.515 mm. THE DISTANCE OF THE TWO WIRES IS 0.3 mm (nH)

	Straight wires	Curved wires	Π shape wires
100 MHz	0.457	0.305	0.176
10 GHz	0.457	0.305	0.176

of real wires. If we use these formulae to calculate the curv22 and curv31 structures, the inductance is 3.11 nH for curv22, 1.28 nH for curv31 and the relative error is 11.0% and 17.2%, respectively.

To investigate the shape dependence of inductance, further simulations and calculations were made assuming a wire with the same radius as that of the test structures. Three shapes are considered: a Π configuration, median curve (circle like) and straight line, all with the same length of 1.515 mm. The results are shown in Table II. It is observed that the difference between the straight wire and the two curved wires cannot be ignored. While the difference are within 18%–48%; the straight wire estimation, which circuit designers usually use, actually overestimates the inductance value and causes inaccurate modeling of the wires. The reason that curved wires have smaller inductance is due to the mutual inductance cancellation of the different segments of a single wire. The generally trend is that the larger curvature a wire has, the smaller its inductance. Self-inductance of a wire also has frequency dependence because of the skin effect. However, the resistance has little dependence on wire curvature if the wire length is fixed since the cross section of a wire does not vary with curvature. In terms of capacitance, the trend is that the more curved a wire is, the smaller capacitance it has since it has a larger distance to the substrate.

Examples of mutual inductance dependency on shape of the two wires are shown in Table III. If the length of the two wires is kept constant, the more curved wires become, the smaller the mutual inductance. This is because the mutual inductance

cancellation from different segments of the two different wires. Mutual inductance has little frequency dependency. Calculation of mutual inductance without considering wire shape overestimates the mutual inductance. The curvature (or shape) of the wires makes a difference for a wire's self and mutual inductances, in turn supporting the need for geometry modeling of bonding wire inductance.

V. Conclusion

A 3-D modeling approach for characterization (and design optimization) of bonding wires is presented. Test structures have been designed, fabricated and measured. A simple compact model of bonding wires is proposed. Simulated electrical parameters show excellent agreement with measured data up to 10 GHz. The major electrical parameter of bonding wires is inductance while at higher frequencies, capacitance becomes important too. Simulation shows that the shape of bonding wires is an important factor to bonding wire inductance. The simulation methodology can be used in support of both RF device modeling and circuit simulation. It is well suited for the design and analysis of circuits for cellular phone communication (i.e., order 2 GHz) and future wireless communication (i.e., order 5 GHz).

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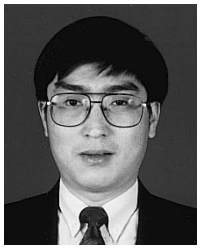

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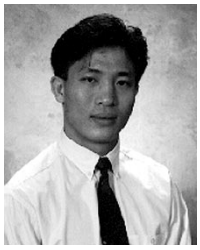

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