Compact On-Chip Wire Models for the Clock Distribution of High-Speed I/O Interfaces

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ABSTRACT

A lumped wire model is proposed for on-chip clock in the low-power and multi-gigahertz IO clock distributions. Ignoring the skin effect and inductive forward coupling, this model can be easily extracted using QuickCap and FastHenry, instead of more computing intensive full-wave solvers. Surrounding power/ground and signal wires within a 1000-μm window are all included in this model. The resulting SPICE netlist and simulation accurately model multiple current returns and the proximity effect at high frequencies. This model is validated with measured *S*-parameter up to 20 GHz using a 90 nm testing chip. The effective loop inductance is shown to have $2\times$ frequency variations which impacts directly on the peak frequency of an *LC* resonance clock distribution.

I. INTRODUCTION

High-speed I/O interfaces require high-quality low-jitter clocking systems to achieve their timing target. Meeting these requirements poses specific challenges for the design of the clock distribution on the silicon chip. One challenge for the clock design is the high frequency of the clocking signal in the interface. At least parts of the on-chip clocking system are operating at the data rate frequency of the interface, which is reaching multi-gigahertz in current production designs and will exceed 10 GHz very soon in future advanced designs. At these frequencies, the on-chip wires used for clock distribution cannot be modeled using traditional *RC* models any more; instead the clock wires have to be modeled as lossy transmission lines [1]-[3]. The accuracy requirement for these transmission line models is high due to the design strategies used for on-chip clocking systems of high-speed I/O interfaces. The clock distribution of high-speed interfaces usually avoids clock buffers as much as possible, since buffers can introduce jitters to the clock due to supply noise. As a result, on-chip clock distribution for high-speed I/O systems is largely wire dominated and the electrical parameters of the clock transmission lines determine the quality of the clock signals. An accurate model of the clock transmission lines is necessary for the design of these wire-dominated clock distributions, determining the maximum distance between clock buffers and the quality of the clock signal at all receiving circuits. In addition, the accuracy requirement for on-chip clock wire modeling increases further for advanced high-speed I/O systems targeting low-power applications. In these designs, the power dissipation for the clock distribution is reduced using *LC* resonance tanks to store the clocking energy. At the multi-gigahertz frequencies of high-speed designs, the inductance of the clock wires itself is contributing significantly to the inductance of this *LC* tank, and an accurate model of the transmission line parameters is essential to design an *LC* tank resonating at the intended operating frequency (see Figure 1).

A special challenge for the on-chip clock wire modeling is the frequency dependency of the resistance and inductance parameters. Frequency dependency of these parameters is well expected at high frequencies due to the skin effect. Because of small wire geometries, namely, thickness and widths, in 90 nm technologies and beyond, the skin effect is not evident. However, for on-chip clock wires embedded into a ground supply grid, frequency dependency of resistance and inductance is also caused by current distribution for the return currents inside this ground grid, often referred to as 'proximity effect'. This proximity effect typically sets in at frequencies easily in the range used for on-chip clock distribution, and has significant impact on the inductance of the clock wire system and therefore the inductance of the resulting *LC* tank. Although full-wave *RLC* extraction and simulation are possible, such computing-expensive extraction and simulation are neither practical nor necessary to large scale industry designs. In this paper, lumped wire and pad models are presented to simulate on-chip clock distribution networks. Wires are modeled as *RLC*-lumped PEEC segments [4]. Additional approximations are made for the skin effect and the inductance forward couplings. Simulation results

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of clock distributions show good agreement with test chip measurement up to 20 GHz. In addition, the high frequency proximity effect is captured. In Session II, both the wire and pad compact models are detailed. Correlation with test chip measurement is presented in Session III. Session IV summarizes the paper.

II. Modeling On-Chip Wires and Pads for Low-Power and High-Frequency Test Chips

A. Efficient Wire Models for On-Chip Wires at Multi-Gigahertz Frequencies

The proposed compact model consists of a limited number of lumped PEEC π segments to model the distributed effects. Wire resistance and capacitance are extracted using standard *RC* extraction tools, such as QuickCap. Inductance is extracted using FastHenry. To speed up circuit simulation, the forward couplings between two segments are eliminated. Wires are considered as single filaments and skin effect is safely ignored[1]. Figure 2 shows the circuit models with *RLC* extraction for a typical co-planar clock tree. In addition, it is assumed that majority of currents returns from the nearest grounds at multi-gigahertz frequencies. The number of lumped π segments is determined by the clock frequency and wire length to ensure the distributed effects are captured[2]. In the case of multiple current returns in ground grids, circuit macros are created to model the proximity effect at high frequencies in SPICE circuit simulation.

B. On-Chip Pad Models for Accurate Measurement De-Embedding

To validate on-chip wire models with test structures, probing pads in test structures need to be de-embedded [5]. Typically, an open pad structures can be manufactured side-by-side with test structures and *S*-parameters of the pads can be measured in order to de-embed the DUT, namely the wires. Alternatively, a compact model can be built for the probe pads using *RLC* network including the feeding wires from the pads to the wires of the DUT. In Figure 3, a typical probe pad and its compact model are illustrated. The *RLC* parameters are extracted using field solvers. Simulation shows that the feeding wires add ~7% of total DUT inductance and ~2% of total DUT resistance at high frequencies. Without a proper de-embedding process, measurement may overestimate DUT inductance at all frequencies and resistance at high frequencies.

III. Correlation of Compact Models with Measurement up to 20 GHz

To validate the proposed models, both single-ended and differential clock designs in test chips are measured. The *S*-parameters from simulated circuit models are compared with the measured ones. Furthermore, measured *RLC* parameters can be extracted from the de-embedded measurement to compare with the *RLC* parameters in the models. Both single-ended and differential clock test structures are illustrated in Figure 4, which are manufactured in a 90 nm technology.

At gigahertz frequencies, the proximity effect impacts on-chip wires in a profound way. Due to high frequencies, currents tend to return closer to the signal wires, resulting in a smaller loop inductance. This is due to the fact that currents always try to find the smallest impedance path. At DC or low frequencies, wire resistance dominates wire loop impedance. Currents spread themselves into many parallel paths in order to minimize the resistance. At high frequencies, inductive part dominates loop impedance. Currents try to return from the nearest grounds in order to minimize the return loops and to reduce the inductive impedance. Figure 5 shows the currents and their returns in DC and high frequency cases. Both proximity and skin effect can be explained by eddy currents in electromagnetic theory [6]. For small wire geometries used in current IC technologies, the proximity effect dominates, and the skin effect is not evident. To verify the model's effectiveness on resistance and inductance frequency dependence, power and ground wires in the test structures are connected like power and ground grids in a real chip.

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[1] The skin depth at 16 GHz clock frequency is roughly 0.52 μm for the copper materials. The typical wire thickness and width in 90 nm technology and below are smaller than 1 μm.

[2] Typically, one π model is needed for each wire length of 1/20 clock wavelength. For example, eight segments are sufficient to model 1 mm long wires at 20 GHz clock frequency.

A. Correlation of the On-Chip Wire Models for Single-Ended Clocks

The correlation between measured single-ended clocks and simulation is plotted in Figure 6. The *S*-parameters comparison show excellent agreement between measurement and simulation up to 20 GHz. Measured *RLC* parameters can also be converted from measured *S*-parameters and compared with simulated *RLC* results. Figure 7 plots the loop resistance of a single-ended clock tree. The resistance is flat at low frequencies, and ramps up at higher frequencies simply due to the proximity effect. The miss-match at lower frequencies is largely due to the process variations and its impact on current return loops[3], which is not modeled in simulation. In Figure 8, the inductance correlation is plotted, which shows the frequency dependency due to the proximity effect. Inductance becomes smaller at high frequencies because return loops are smaller. Capturing the $2\times$ inductance frequency variation is extremely important to *LC* resonance clock distributions in low-power I/O designs. Depending on the operating clock frequency, the inductance contribution from wires can vary significantly, which in turn determines the peak resonance frequency in the clock distribution. The miss-match at low frequency range could also be the result of resistance miss-match, which impacts the size of return loops.

B. Correlation of the On-Chip Wire Models for Differential Clocks

Differential clocks are extensively used in low power and high frequency I/O designs. It is essential to validate the models for the differential clock configuration. To measure differential clock signals, mixed-mode differential to differential *S*-parameters are used, where two clock wires are driven differentially at near and far end [7]. The *S*-parameter magnitude correlation between measurement and simulation is plotted in Figure 9. Good agreement is achieved in most of the frequency points. The miss-match above 10 GHz may be due to the frequency independent pad models used in the simulation.

IV. CONCLUSION

A lumped on-chip compact wire model for both single-ended and differential clocks are proposed for wire-only and low-power *LC*-resonance clock distributions. In addition, effective on-chip pad models are also presented. The models are correlated with a test chip up to 20 GHz in a 90 nm technology. SPICE circuit simulation using the model is able to capture the important inductance frequency dependency due to the proximity effect, which validates that the simplified PEEC *RLC* models are sufficient to model clock distributions in the low-power and high-frequency I/O applications. The miss-matches between measurement and simulation mostly result from the frequency independent pad models and process variations.

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[7] Anritsu, "Three and four port S-parameter measurements," *Anritsu Application Note*, http://www.us.anritsu.com.

[3] There are +/- 28% wire resistance variation and +/- 50% via resistance variations in this process.

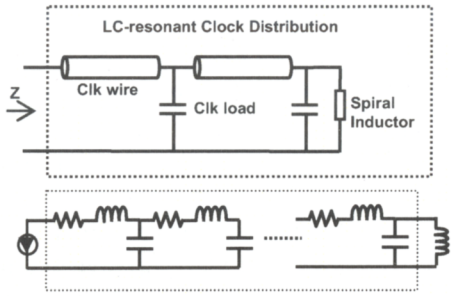

Figure 1. The *LC*-resonant clock distribution and its circuit model.

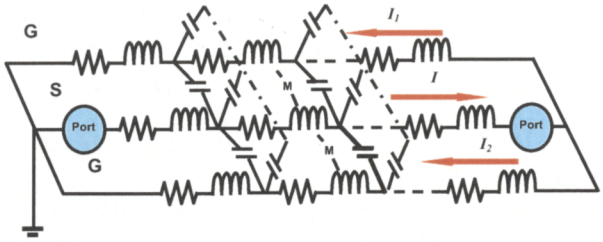

Figure 2. Multiple lumped π–models are used to model the distribute effects.

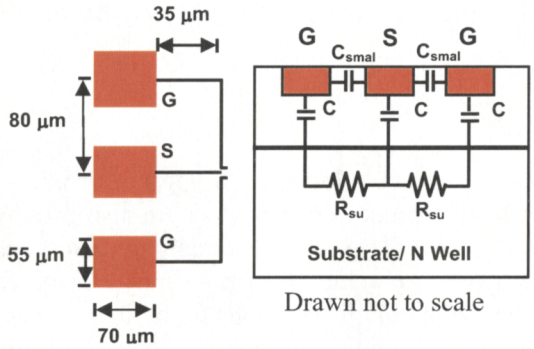

Figure 3. The compact model for probe pads and feeding wires.

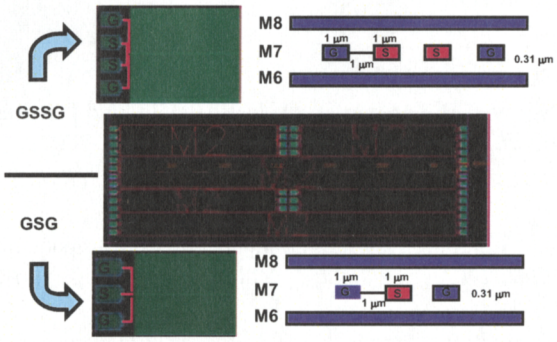

Figure 4. The single-ended and differential clock test structures.

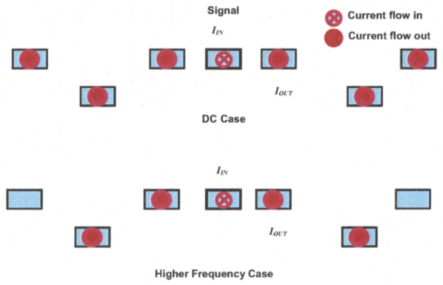

Figure 5. The proximity effect in parallel wires at high frequencies.

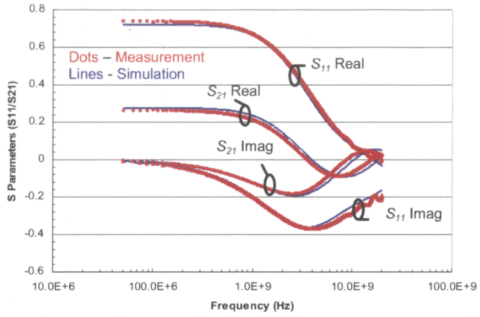

Figure 6. The *S*-parameter correlation for the single-ended clock: The average error is 8% (e.g. S_{11} Imag).

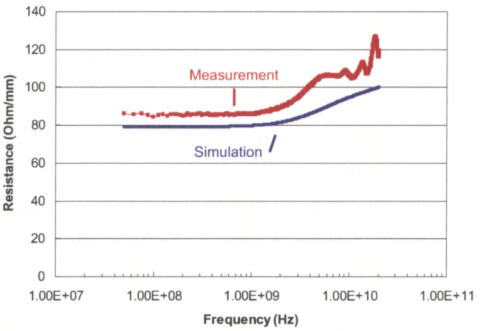

Figure 7. Loop resistance increases at high frequencies due to the proximity effect. The average error is 13%.

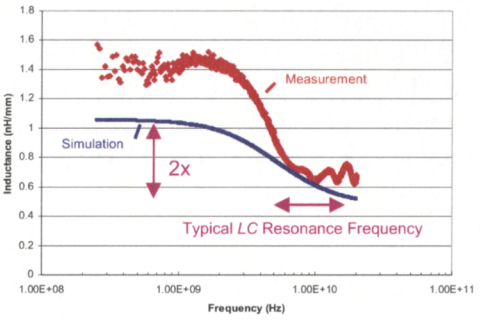

Figure 8. Loop inductance decreases (2x) at high frequencies due to the proximity effect. The average error is 14% above 500MHz.

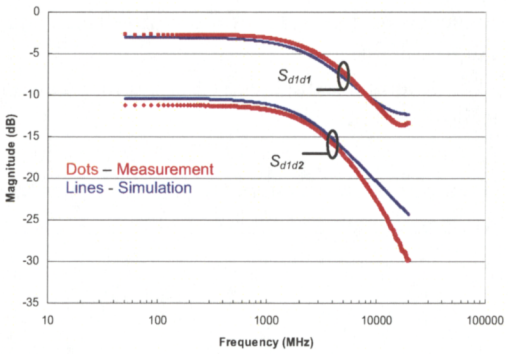

Figure 9. Mixed-mode differential to differential *S*-parameters comparison for the differential clock: The average error is 10% (e.g., S_{d1d2}).