# A Circuit-Based Noise Parameter Extraction Technique for MOSFETs

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*Abstract*- **Experimental verification of noise models is one of the major challenges in noise modeling. A circuit-based noise characterization technique is introduced which uses phase noise measurement data to extract MOSFET noise parameters. After a brief discussion on MOSFET noise, experimental data is presented on the severity of excess noise in a 0.18 μm CMOS process using the proposed technique. It is shown that in this process, the noise power of minimum-channel-length devices is up to 6 dB larger than that of long-channel devices. The proposed technique can be used for model verification as well as for parameter extraction in developing CMOS processes.**

## INTRODUCTION

Understanding noise in MOSFETs is crucial for the future of analog CMOS design. As early as 1986, experimental data has suggested that the classical long-channel MOSFET noise model [1] underestimates the drain current noise of short-channel devices (see for example [2]). Several studies have tried to replicate those results or theoretically explain this phenomenon (Fig. 1). These investigations have led to different (and sometimes conflicting) results for MOSFET noise behavior. Today, understanding noise in short-channel MOSFETs is still an ongoing challenge.

One of the major difficulties in noise modeling is experimental verification. The outcome of a noise measurement experiment can be affected by many parasitic elements and environmental variables. In order to obtain reliable results, these elements and variables should be de-embedded, and accounted for or controlled during the course of the experiment. Because of the complexity of such experiments, there are usually protracted discussion about the validity of any experimental noise data reported in the literature and the accuracy of the respective noise models. Also, many state-of-the-art CMOS processes lack a reliable set of noise parameters because of these difficulties.

We introduce a circuit-based technique for MOSFET noise characterization based on phase noise measurement. Being based on phase noise measurements, this method is faster than direct device noise characterization because the phase noise of an oscillator is mainly set by the noise sources and electrical components inside the oscillation loop. Thus most off-chip parasitic elements do not have a significant effect on the phase noise of integrated oscillators. Furthermore, phase noise measurement is a comparative measurement between the signal power at the center frequency and that at a small offset frequency [3]. Therefore, the effects of many parasitic elements such as cable loss and impedance mismatch are significantly canceled out. This greatly reduces the number of non-idealities in this indirect characterization and makes it faster and less costly to perform.

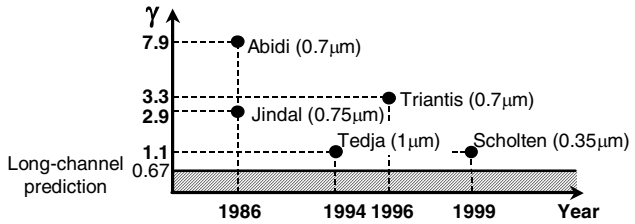


Fig. 1. Some reported values of Gamma noise factor in various technologies.

The organization of this paper is as follows. We first present a brief discussion of noise in modern MOSFETs. We then introduce an asymmetrical ring oscillator that will be used for indirect characterization of device noise using phase noise measurement data. Using this oscillator, we extract noise parameters for a 0.18 μm CMOS process.

## NOISE MODELING FOR MODERN MOSFETS

### A. *Noise in Long-Channel MOSFETs*

The classical approach for the formulation of drain noise PSD (power spectral density) is graphically shown in Fig. 2 [1]. In this approach, the channel is first sliced into small pieces of resistance *dR*. These slices are then replaced by their noisy model and the noise contribution of each slice at the output terminal is calculated using analytical or numerical means. Subsequently, these contributions are summed up, assuming independence. For an ideal long-channel MOSFET, this formulation results in $\overline{i_{nd}^2} = 4kT\gamma g_{do}$ where γ is called the Gamma factor whose numerical value is 2/3 for devices working in saturation and $g_{d0}$ is the output conductance of the device for $v_D$=0 (with the value of $v_G$ unaltered).

### B. *Noise in Short-Channel MOSFETs: A Simple Physical Argument*

As can be seen in Fig. 1, the Gamma factor (and thus the noise PSD) of modern short-channel devices is often larger than the number predicted by the long-channel model. The calculation of noise PSD in short-channel MOSFETs is more complicated than ideal long-channel devices because of the short-channel effects. One of the important characteristics of

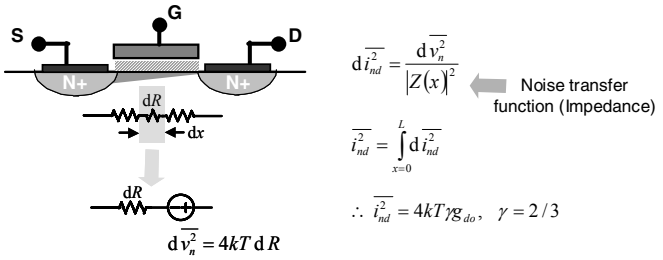


Fig. 2. Classical formulation of MOSFET noise.

short-channel MOSFETs is that the current flow in these devices is not entirely controlled by the channel resistance. Rather, the current flow is limited by both channel resistance and the potential barrier next to the source [4]. In many aspects, these devices behave similar to ballistic MOSFETs in which current is solely limited by the potential barrier[1].

To intuitively understand noise in ballistic MOSFETs, consider an ideal device in which carriers do not undergo any scattering in the channel. Current flow in such a device is mainly limited by carrier injection from the source across the source potential barrier (Fig. 3). Let us also assume that the time duration of carrier flight from the source to the drain is considerably smaller than the average time interval between two consecutive injections from the source. In such a device, carrier injections are nearly mutually independent because the injection of each carrier does not affect the electrostatic fields of the device long enough and strong enough to have a sensible effect on the probability of the next injection. This situation leads to the appearance of shot noise [6]. Therefore, the drain noise of a ballistic device can be modeled by a white noise current source with a PSD of $2qI_{DC}$ where $q$ is the electron charge. The foregoing discussion provides an intuitive understanding of noise in ballistic MOSFETs; an analytical discussion is given in [4] and [7].

The noise properties of today's short-channel (semi-ballistic) devices can be explained based on the foregoing discussion. In semi-ballistic MOSFETs, each injected carrier has to undergo some channel scattering before reaching the drain (Fig. 3). This process alters the electrostatic fields in the device after each carrier injection until the injected electron is absorbed and device fields relax to their steady-state condition. Therefore, the probability of carrier injection is reduced after the injection of each electron. This process generates a negative feedback which regulates the carrier flow and makes the noise PSD smaller than $2qI_{DC}$, a phenomenon that is referred to as partial suppression of shot noise.

Partial suppression of shot noise has been studied analytically for vacuum tubes in [8]. According to this analysis, current flow in a modern (high-efficiency-cathode) vacuum tube (for which the current is limited by the space-charge potential) is given by $2k_sqI_{DC}$ where $k_s<1$ is called the shot noise suppression factor (also known as fano factor). This is because in these devices the injection of each carrier from the cathode alters the fields in the space charge region which reduces the probability of the next injection. Since the carrier transport in semi-ballistic MOSFETs closely resembles that in modern

1. Detailed quantum mechanical analysis shows that today's MOSFETs operate at fifty percent of their ballistic limit [5].

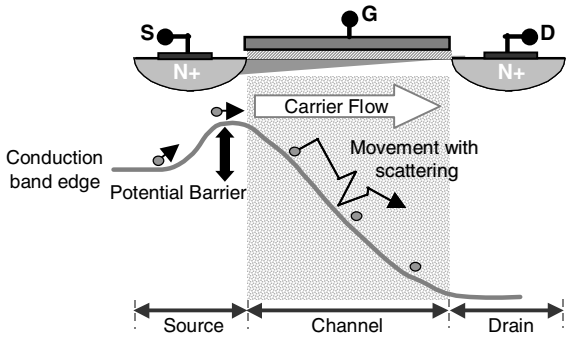


Fig. 3. Two current limiting mechanisms in every MOSFET are the potential barrier next to the source and the channel resistance.

vacuum tubes, the same analytical derivation can be used to conclude that noise power in these devices can also be modeled by $2k_sqI_{DC}$. Based on this argument, the noise PSD of short-channel devices can best be characterized by the shot noise suppression factor ($k_s$) and not by the Gamma factor which is most suitable for long-channel devices.

The appearance of partially-suppressed shot noise in small-scale conductors is not unprecedented. It has already been theoretically predicted and experimentally observed in mesoscopic conductors, conductors of the sizes comparable to phonon-phonon scattering length and ballistic MOSFETs (e.g. [9][7]). The application of these findings to short-channel, semi-ballistic MOSFETs is, however, still new and requires more investigation. Nevertheless, we will report the shot noise suppression factor for the short-channel MOSFETs studied in this work because it appears to be more relevant in these devices.

## Indirect Device Noise Characterization

### *A. An Oscillator for Indirect Noise Characterization.*

Indirect characterization of device noise through phase noise measurement calls for an oscillator with predictable (but not necessarily low) phase noise. Fig. 4 shows one such oscillator designed for this study. The phase noise of this oscillator is accurately predictable using the time-domain phase noise formulation method presented in [10] because most of the simplifying assumptions used in that formulation is satisfied in this oscillator.

As can be seen in Fig. 4, our asymmetrical ring oscillator is composed of seven inverters capacitively loaded with large metal-insulator-metal (MIM) capacitors. These capacitors are designed to be large enough to swamp the total capacitance of all internal nodes of the oscillator. Therefore the total capacitance is guaranteed to be linear and have a weak temperature dependency. Furthermore using same size capacitors in different ring oscillators makes it possible to compare the noise of MOSFETs of various channel lengths.

The seven inverters in the oscillation loop are sized differently, hence the name asymmetrical. There are three 1X inverters and four 10X ones in the oscillation loop. With the loading capacitors being the same, the outputs of the small inverters change much more slowly than the outputs of large inverters (Fig. 4). Thus the frequency of oscillation is mainly determined by these inverters. Also, because of the faster volt-

age rate of change, the noise of large inverters has an insignificant effect on the phase noise of the oscillator. This is because the induced jitter at each stage is inversely proportional to the square of the voltage rate of change at its output. Even though current noise power at the output of the large inverters is approximately ten times stronger than that at the output of the small oscillators, their jitter contribution is ten times smaller because of the faster voltage rate of change. Therefore the formulations presented in [10] are valid for this oscillator with N=3.

Another feature of this oscillator is the fact that the gate to source voltage of the transistors in small inverters is nearly constant for the duration of charge or discharge of the capacitors at their outputs. This is because the large inverters are capable of charging and discharging their output nodes much faster than are the small inverters. Since these nodes are the input to small inverters, the gate to source voltage of the transistors in these inverters stays constant during most of the charge and discharge time. This means that the biasing condition of the transistors whose noise power sets the oscillator's phase noise is constant during their active time. This is an important virtue of this oscillator which enables reliable indirect characterization of device noise through phase noise measurements for various bias voltages. As can be seen, the approximations involved in the time-domain formulation of phase noise presented in [10] are closely satisfied in this oscillator. Thus we expect this formulation to provide accurate numbers for phase noise for a given device noise level. Similarly, it should be possible to back-calculate device noise power using the same equations after measuring phase noise.

To study noise at different channel lengths, three oscillators have been designed with the same topology and the same loading capacitance but different channel lengths. We expect the shortest transistors to be semi-ballistic devices and the longest MOSFETs to follow long-channel MOSFET formulation. The width-to-length ratio is kept constant in these oscillators to ensure comparable oscillation frequencies. The transistors are built with multiple gate fingers to minimize gate resistance noise. In all cases, the noise power of the gate resistance is at least an order of magnitude smaller than the device noise, according to the provided models. All inverters in all three oscillators are loaded by similar MIM capacitors of a nominal value of 500 fF. Thus the loading capacitance is, to the first order, the same in these oscillators. Using circuit simulation, we have also estimated the parasitic capacitance at internal nodes by increasing the loading capacitance to $2C_{MIM}$ and taking note of the frequency change.

The oscillators described above are fabricated in a commercially-available 0.18 µm CMOS process technology. Fig. 5 shows a photo of the die carrying these oscillators. In the following section we present the result of phase noise measurement on these oscillators and their implication for noise of the MOSFETs fabricated in this process.

### *B. Phase Noise Measurement Results and Discussion*

The phase noise of the three aforementioned oscillators are measured at a typical supply voltage of 1.8 V. The results are shown in Fig. 6. As can be seen in this figure, at an offset frequency of 1 MHz (which is located in the $1/f^2$ region) the long-channel oscillators has smaller phase noise, as expected because of excess noise. To quantify this effect, Fig. 7 compares the phase noise of these oscillators to the minimum achievable phase noise of ring oscillators [10] at the same power consumption and oscillation frequency (T=300 K is assumed). Multiple measurements have been performed at each data point to enhance accuracy. The solid line connects the average values. As can be seen, the difference between the minimum achievable phase noise and the measured phase noise is 6.5 dB larger at 0.18 µm channel length. Thus the noise power of the 0.18 µm transistors is almost four times the noise power of 0.54 µm transistors in this technology.

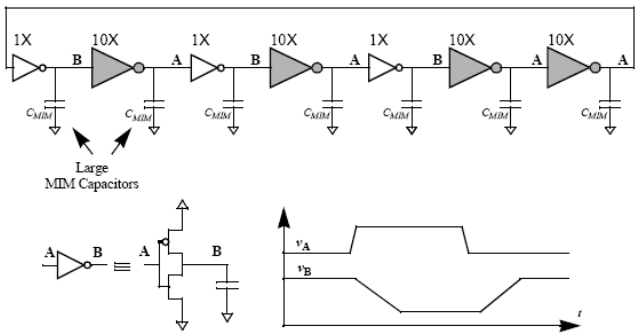


Fig. 4. An asymmetrical ring oscillator for the characterization of device noise through phase noise measurement.

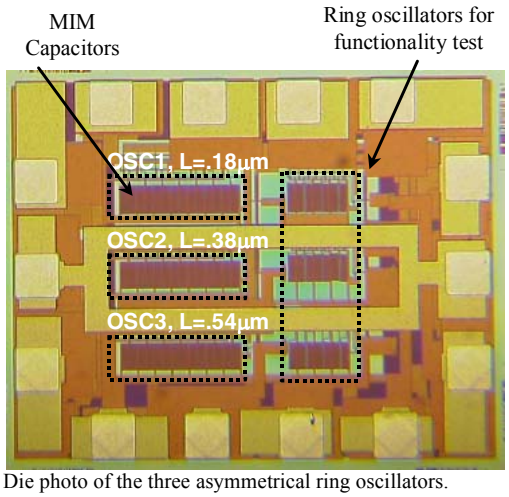


Fig. 5. Die photo of the three asymmetrical ring oscillators.

For long-channel (0.54 µm) transistors, we have extracted the gamma factor from phase noise data (Fig. 8). Note that, the gamma factor in this case is slightly larger than the long-channel prediction. The deviation of the gamma factor from its long-channel value and its increase at high gate voltages can be partly attributed to measurement error or it can be an indication of some short-channel effects in these transistors.

For short-channel (0.18 µm) transistors, we have extracted the shot-noise suppression factor ($k_s$) from phase noise data (Fig. 9). Note that this factor is close to 0.7 in this case and drops at high gate voltages. The apparent slight increase of $k_s$ at $v_{GS}$=2.2 and 1.9 is within the error bars and thus may be artifacts. The overall drop of $k_s$ at high $v_{GS}$ values is due to mobility degradation at high gate voltages which means more scattering events in the channel and greater suppression of shot noise. In general, drain noise in short-channel devices is close to seventy percent of full shot noise in this technology.

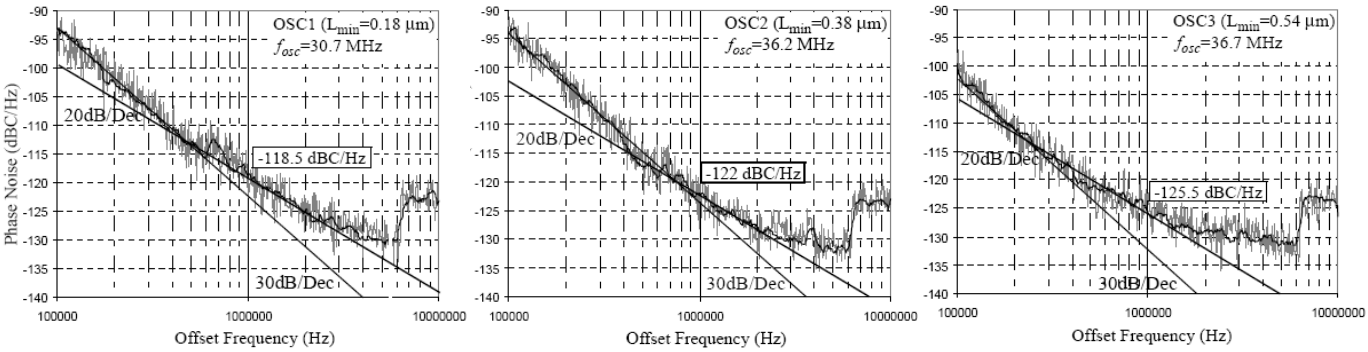


Fig. 6. Phase noise of the asymmetrical ring oscillator using 0.18µ, 0.38µ and 0.54µ devices.

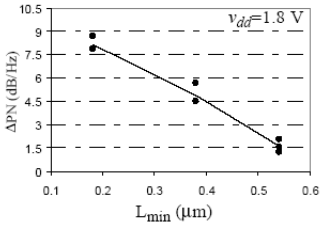


Fig. 7. Excess phase noise versus the channel length of minimum-size devices used in the asymmetrical ring oscillator.

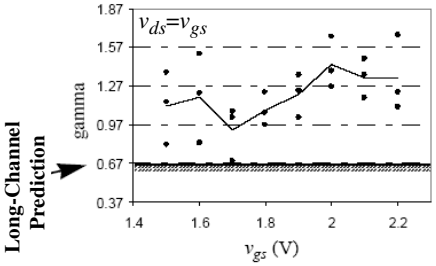


Fig. 8. Gamma factor for long-channel (0.54µm) transistors.

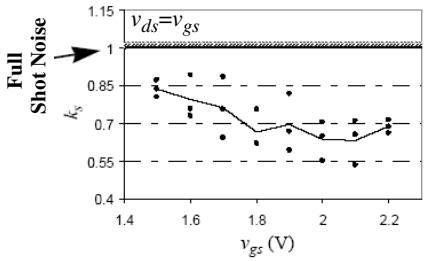


Fig. 9. Shot noise suppression factor for short-channel (0.18µm) transistors

## CONCLUSION

We introduced a circuit-based method for extracting MOSFET noise parameters using phase noise measurement. Although parameter values extracted using this method may not be as accurate as direct device noise characterization (particularly in the case of shot noise suppression factor where direct characterization often provides smaller numbers for comparable devices), they provide very good accuracy regarding the comparative noise power in various devices. The test structures used for this characterization are simple ring oscillators which are routinely used for process characterization. Therefore the overhead of performing this indirect noise characterization is minimum while the information that can be extracted is invaluable for early process characterization as well as for providing guidelines to low-noise analog designers designing in a mature CMOS process technology.

Using the proposed method we extracted noise parameters for various devices in a 0.18µm CMOS process. In this process, the phase noise of the oscillators built using short-channel devices is nearly 6 dB inferior to that of those built using long-channel devices (at the same power consumption and oscillation frequency). The extracted gamma factor and shot noise suppression factor for long- and short-channel devices are around 1 and 0.7 respectively. Our noise characterization suggests that up to 6 dB phase noise improvement is possible by using three times minimum channel length devices. It is straightforward to conclude that similar improvement is achievable for amplitude noise at the cost of slower devices.

## ACKNOWLEDGMENT

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