LUMPED, INDUCTORLESS OSCILLATORS: HOW FAR CAN THEY GO?

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Abstract

The fundamental question of how much we can ultimately reduce the phase noise of a lumped, inductorless oscillator through careful design is addressed and it is shown that the fluctuation dissipation theorem of thermodynamics imposes a lower limit on the phase noise. An analytical formulation of this limit is presented and it is shown that the phase noise of ring oscillators with long-channel MOS devices is closer to this limit compared to that of the relaxation oscillators or ring oscillators with short channel MOS devices.

Introduction

Due to the increasing demand for high-level integration of electronic circuits, lumped, inductorless oscillators (LIOs) have become an extremely attractive choice for today's IC designers. Relaxation and ring oscillators are used in several applications including clock recovery circuits for serial data communications (1) and on-chip clock distribution (2). However, applications in radio frequency (RF) circuits is quite limited mainly due to inferior phase noise behavior compared to inductor-based oscillators. Although several investigations have been performed to improve the phase-noise of LIOs (*e.g.* (3)), the fundamental question of whether or not there is a minimum achievable phase noise for this class of oscillators has not been addressed. This lingering question causes a great deal of uncertainty about the scalability of RFIC design without using tuned circuits.

In this paper we address this question and show that one of the fundamental principles of thermodynamics sets a lower limit on the phase noise of LIOs. Using a simplified model, we then present a quantitative analysis of this minimum achievable phase noise. Finally, we present several examples from previously published results on relaxation and ring oscillators to compare the minimum achievable phase noise to the experimental results from real designs.

The Physical Argument for Minimum Achievable Phase Noise

The phase noise of an oscillator is an indication of the fact that the oscillator is not continuously oscillating with the same frequency. To build a stable (and hence low-phase-noise) oscillator, one should be able to enforce the period of oscillation in a reliable fashion. In other words, a constant with the dimension of time is required to dictate the oscillation period. In inductor-based oscillators (like the Colpitts) this constant is $\sqrt{LC}$ were L is the inductor and C is the capacitor. In transmission-line-based oscillators the ratio of l/v establishes the time constant in which l is the length of the transmission line and v is the velocity of electromagnetic wave inside the transmission line. In LIOs the product of RC is usually the time constant. There is, however, a fundamental difference between this latter case and the first two ones. The fluctuation dissipation theorem of thermodynamics dictates that there exists a finite amount of thermal noise associated with any resistor. Thus, in contrast to inductor-based and transmission-line-based oscillators, the time constant of LIOs is inherently noisy because of the resistor noise. Consequently, even if the rest of the circuit is noise-free, the resistor noise imposes a lower limit on the phase noise of LIOs.

To provide a quantitative prediction of this minimum achievable phase noise, we use a simple model for an LIO (Fig. 1). Only the equilibrium resistor noise (given by $4kT/R$) is taken into account in this formulation of minimum achievable phase noise. Although ring oscillators do not completely resemble this model, the final result for the lower limit of phase noise is still applicable to them. In fact, by taking into account the transistor noise and noise bandwidth in critical circuit nodes of a ring oscillator, it can be shown that their minimum achievable phase noise is always slightly higher than that of the model given in Fig. 1.

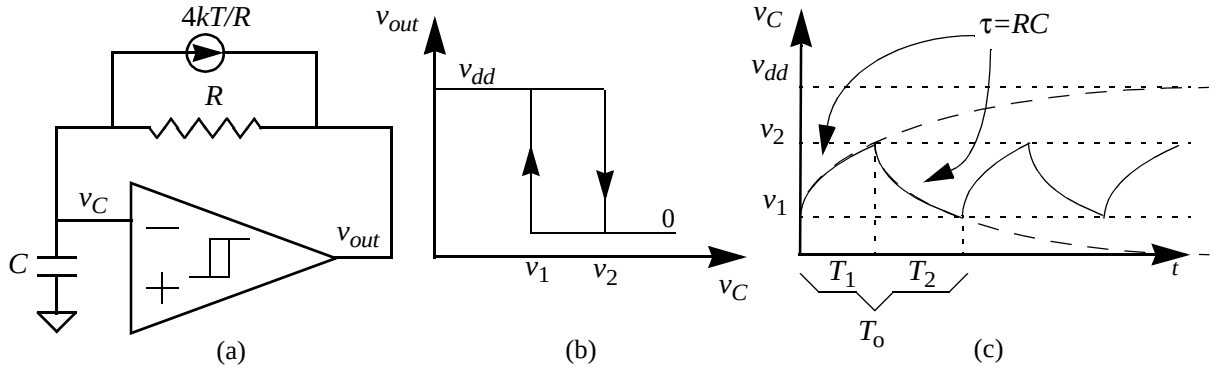

Fig. 1: (a) A typical *RC* relaxation oscillator. (b) The Schmitt comparator transfer function. (c) The waveform for the capacitor voltage

Analytical Formulation of Phase Noise for the *RC* Relaxation Oscillator

Fig. 1 shows a typical *RC* relaxation oscillator, which will be used as a simplified model for an LIO. The oscillator is composed of a Schmitt comparator in an *RC* feedback loop. We first derive the basic equations governing the behavior of this oscillator and present an analysis of the jitter. In this analysis, the equilibrium resistor noise (given by $4kT/R$) is taken into account while all other noise sources associated with the comparator and all non-equilibrium noise sources (like $1/f$ noise) are neglected. We then provide an analytical formulation of phase noise for this relaxation oscillator. The expression that we derive provides the minimum achievable phase noise dictated by the first principles of thermodynamics.

A. Frequency and Minimum Power Dissipation

The oscillator of Fig. 1 works as follows: during the first half of the period, the capacitor voltage changes exponentially from v_1 to v_2 (the two comparison levels). The duration of the first half of the period is found to be

$$T_1 = RC \times \ln\left(\frac{v_{dd} - v_1}{v_{dd} - v_2}\right) \tag{1}$$

Similarly, the duration of the second half of the period is

$$T_2 = RC \times \ln\left(\frac{v_2}{v_1}\right) \tag{2}$$

and the frequency of oscillation is given by

$$f_{osc} = \frac{1}{T_o} = \frac{1}{T_1 + T_2} = \frac{1}{RC \times \ln\left(\frac{v_{dd} - v_1}{v_{dd} - v_2} \times \frac{v_2}{v_1}\right)} \tag{3}$$

where T_o is the period of oscillation.

The absolute minimum power dissipation of this oscillator (neglecting the power consumed by the comparator) is dictated by the amount of charge transferred to the capacitor as its voltage moves between v_1 and v_2 in each cycle:

$$P_{min} = v_{dd} C (v_2 - v_1) f_{osc} \tag{4}$$

B. Jitter

The jitter is generated by the fluctuations of v_C which are in turn caused by the resistor noise. The probability density function of the fluctuations of v_C at any given time t can be found using the circuit model of Fig. 2. Assuming that the capacitor voltage is zero at t=0, this voltage as a function of the noise current, i_n, is given by

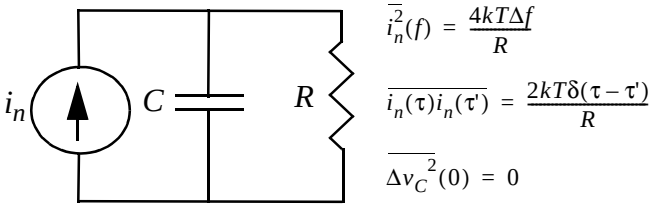

Fig. 2: The circuit model and the basic equations for calculating the variance of the capacitor voltage at any time t ($v_C(t)$) given that its value is accurately known at time t=0.

$$v_C(t) = \frac{e^{-\frac{t}{RC}}}{C} \int_0^t e^{\frac{\tau}{RC}} i_n(\tau) d\tau \tag{5}$$

Since i_n is a Gaussian process with zero mean, (5) dictates that v_C is also a Gaussian process with zero mean. Consequently, the fluctuations of v_C will be completely described by finding its variance. Using (5) we can find the variance of v_C:

$$\overline{v_C^2(t)} = \frac{e^{-\frac{2t}{RC}}}{C^2} \int_0^t \int_0^t e^{\frac{\tau + \tau'}{RC}} \overline{i_n(\tau) i_n(\tau')} d\tau d\tau' \tag{6}$$

in which $\overline{i_n(\tau) i_n(\tau')}$ is the autocorrelation function of the noise source whose value is given in the onset of Fig. 2. Using this autocorrelation function in (6) and performing the integration, the variance of v_C is found to be[1]

$$\overline{v_C^2(t)} = \frac{kT}{C}\left(1 - e^{-\frac{2t}{RC}}\right) \tag{7}$$

Note that as $t \to \infty$ the variance of v_C converges to kT/C and becomes independent of R. By replacing t in (7) by T_1 or T_2, we can find the variance of the v_C at the end of the first and second half-periods, respectively.

As the capacitor voltage approaches the decision levels, the fluctuations of v_C shifts the switching instance form its anticipated time and hence results in jitter. As far as the timing jitter for T_1 (T_2) is concerned, the fluctuations of v_C can be interpreted as some uncertainty on the decision level v_2 (v_1). Using (1) and (2) the variances of T_1 and T_2 are then evaluated as:

$$\overline{(\Delta T_1)^2} = \left|\frac{\partial T_1}{\partial v_2}\right|^2 \overline{(\Delta v_2)^2} = \left(\frac{RC}{v_{dd} - v_2}\right)^2 \overline{(\Delta v_C)^2} \tag{8}$$

$$\overline{(\Delta T_2)^2} = \left|\frac{\partial T_2}{\partial v_1}\right|^2 \overline{(\Delta v_1)^2} = \left(\frac{RC}{v_1}\right)^2 \overline{(\Delta v_C)^2} \tag{9}$$

1. The presented derivation is simplified for brevity. A rigorous derivation shows that the final result is, nevertheless, correct.

where the linearization approximation is justified due to the fact that the noise level is always small. The total uncertainty in the period (cycle-to-cycle jitter) is given by:

$$\overline{(\Delta T_o)^2} = kTR^2C\left(\frac{1}{(v_{dd}-v_2)^2}+\frac{1}{v_1^2}\right)\left(1-e^{-\frac{T_o}{RC}}\right) \qquad (10)$$

We have assumed a duty cycle of 50% so that we can replace $2t$ in (7) by T_o. Note also that ΔT_1 and ΔT_2 are uncorrected variables. The switching takes place exactly when v_C equals v_1 or v_2. Consequently, at the beginning of each half cycle the value of v_C is known accurately. Since the only noise source taken into account is white, the uncertainty of v_C and hence $T_{1,2}$ at the end of each half cycle is completely independent of the one at the end of previous half cycle. This ensures us that ΔT_1 and ΔT_2 are in fact independent.

After solving (3) for R and using it in (10) we get

$$\overline{(\Delta T_o)^2} = \frac{kT}{2Cf_{osc}^2v_{dd}^2}\cdot\frac{(1-2v_{1n})}{v_{1n}^2\ln\left(\frac{1}{v_{1n}}-1\right)^2(1-v_{1n})^2} \qquad (11)$$

where $v_{1n} = v_1/v_{dd}$ is the normalized decision level. We have assumed v_2=v_{dd}-v_1, which ensures a duty cycle of 50%. The second part of (11), called the normalized jitter, is only a function of v_{1n} and can be plotted versus this parameter. Fig. 3 present such a plot showing that the normalized jitter is minimized for v_{1n}=0.24. For constant values of temperature, capacitance, oscillation frequency and bias voltage, jitter (and hence phase noise) assumes its minimum value for v_1=0.24v_{dd} and v_2=0.76v_{dd}. Hereafter, we will use these values to find the minimum achievable phase noise. The minimum power dissipation and minimum cycle-to-cycle jitter are then found to be

$$P_{min} = 0.52Cf_{osc}v_{dd}^2 \qquad (12)$$

$$\overline{(\Delta T_o)^2} = 2\overline{(\Delta T_1)^2} = \frac{5.9kT}{Cf_{osc}^2v_{dd}^2} = \frac{3.1kT}{P_{min}f_{osc}} \qquad (13)$$

C. Phase Noise

The output of the relaxation oscillator of Fig. 1 is a stochastic square wave signal with mutually-independent, Gaussian-distribution cycle-to-cycle jitter. As presented in (4), the phase noise of such a signal has a close-to-Lorentzian shape around each harmonic. The phase noise around the first harmonic at an offset frequency of $\Delta\omega = |\omega - 2\pi f_{osc}|$ is given by

$$PN(\Delta f) = \frac{f_0^3\overline{(\Delta T)^2}}{(\pi f_0^3\overline{(\Delta T)^2})^2+(f-f_0)^2} \qquad (14)$$

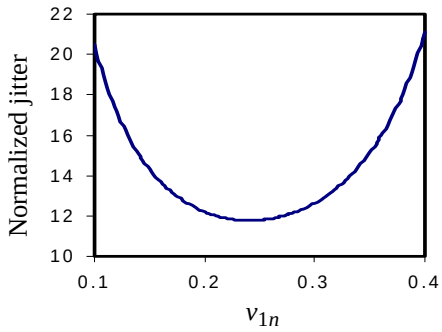

Fig. 3: Normalized jitter vs normalized decision level v_{1n}.

This equation predicts that the phase noise has a $1/f^2$ shape for sufficiently large offset frequencies, which is consistent with the previously reported measurement results ((5) and (6)). Using (13) in (14) the phase noise at these offset frequencies is found to be

$$PN(\Delta f) = \frac{5.9f_{osc}kT}{Cv_{dd}^2(\Delta f)^2} = \frac{3.1kT}{P_{min}}\left(\frac{f_{osc}}{\Delta f}\right)^2 \qquad (15)$$

The phase noise is inversely proportional to the minimum power dissipation, which is in turn proportional to the capacitor value and the square of the bias voltage.

Experimental Results

The expression given in (15) provides the minimum achievable phase-noise for the idealized version of the relaxation oscillator shown in Fig. 1. Most practical relaxation oscillators, however, are not implemented in this fashion. Fig. 4 provides the schematic and the design parameters of a CMOS relaxation oscillator reported in (5). Although this oscillator is not exactly of the same form as the idealized relaxation oscillator given in Fig. 1, it is still considered an LIO. In the case of the oscillator of Fig. 4, the charging and discharging mechanism of the capacitor is not through a resistor but rather through the current sources and the transistors. Nevertheless, these components are noisy and thus impose a minimum achievable phase noise for this architecture.

Fig. 5 compares the phase noise reported in (5) to the minimum achievable phase noise given by the second part of (15) under a constraint of constant power. To calculate P_{min}, we have assumed v_{dd}=3.3V which is typical for the 0.5µm technology. The minimum achievable phase noise for this power level is -122.6dBc/Hz and -136.6dBc/Hz at 1MHz and 5MHz offset frequencies, respectively. The measured values reported in (5) are -102dBc/Hz and -115dBc/Hz. Without increasing the power dissipation, around 21dB of phase noise improvement is possible before hitting the limit line of minimum achievable phase noise dictated by the first principles of thermodynamics for this class of oscillators. A similar architecture is reported in (6) as a relaxation VCO, which draws 2.3mA of current from a 6V power supply at 115MHz (Fig. 5.a and Fig. 7 in (6)). Under constant power-constrained

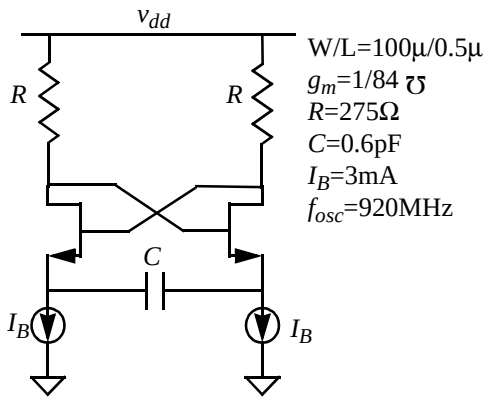

Fig. 4: The schematic and design parameters of the relaxation oscillator reported in (5).

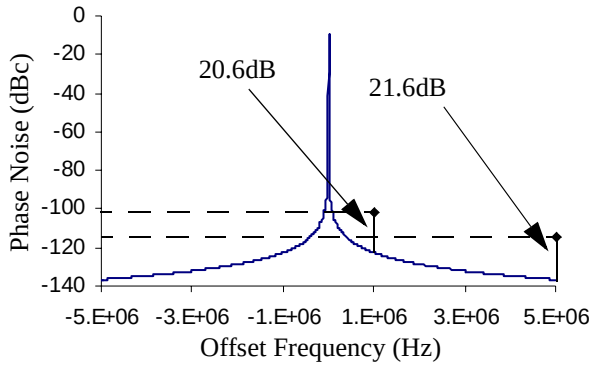

Fig. 5: Minimum achievable phase noise compared to the data reported in (5) for an oscillator with f_{osc}=920MHz and P_{min}=19.8mW at T=300°K.

design, (15) predicts that the minimum achievable phase noise for this oscillator is -139dBc/Hz at an offset frequency of 1MHz. This is again 21dB lower than the reported value of -118dBc/Hz given in (6). These two examples illustrate that the relaxation oscillator configuration is not an optimum choice in terms of the power-phase noise tradeoff.

Experimental data on ring oscillators shows that these oscillators perform better in terms of power-phase noise tradeoff. Table I compares the measurement results reported in (3) to the theoretical prediction of the minimum achievable phase noise for the same power. The index numbers are the same as the ones assigned in (3). N is the number of stages and L_{min} is the channel length of the smallest transistor in the circuit. The data is presented in descending order of L_{min}. The difference between measured and predicted phase noise in this case is smaller than 9dB with most numbers around 6dB much better than the relaxation oscillator case. The difference between the minimum achievable phase noise and the measured phase noise increases with decreasing L_{min}. This can possibly be attributed to the excess noise in short-channel MOS devices the origins of which is discussed in (7).

Table I: Experimental results vs. theoretical prediction of minimum achievable phase noise at Δf=1MHz for the ring oscillators of (3).

Index	N	L_{min} µm	f_{osc} MHz	Power mW	$PN_{meas.}$ dBc/Hz	PN_{min} dBc/Hz	ΔPN dB	Current Starved
1	5	2	232	1.5	-118.5	-123.4	4.6	No
2	11	2	115	2.5	-126	-131.7	5.7	No
4	3	0.53	751	5.85	-114	-119.1	5.1	Yes
5	5	0.39	850	6.27	-112.6	-118.3	5.7	Yes
6	7	0.36	931	6.22	-111.7	-117.5	5.8	Yes
7	9	0.32	932	6.82	-112.5	117.9	5.4	Yes
8	11	0.32	869	6.62	-112.2	118.3	6.1	Yes
9	15	0.28	929	7	-112.3	118	5.7	Yes
10	17	0.25	898	9.5	-112	119.6	7.6	Yes
11	19	0.25	959	9.75	-110.9	119.2	8.3	Yes
3	19	0.25	1330	25	-111.5	120.4	8.9	No

Conclusion

The lower limit of phase noise in LIOs is shown to be dictated by the fluctuation dissipation theorem of thermodynamics. Using a simplified model for this class of oscillators, a quantitative prediction of this minimum achievable phase noise is presented and the phase noise is expressed as a function of temperature, power dissipation, frequency of oscillation and the offset frequency. The phase noise of ring oscillators is generally closer to this limit compared to that of the relaxation oscillators, making a ring oscillator a more attractive choice in terms of power-phase noise tradeoff. It is shown that the phase noise improvement through careful design is fundamentally limited to 5 to 10dB for practical ring oscillator designs. The difference between the minimum achievable phase noise and the actual measured phase noise of a typical ring oscillators increases as we shrink the channel length of the MOS devices, which can be explained as due to the excess noise in short-channel MOS devices.

Acknowledgments

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References

(1) L. DeVito, J. Newton, R. Croughwell, J. Bulzacchelli, and F. Benkley, "A 52MHz and 155MHz clock-recovery PLL," in *ISSCC Dig. Tech. Papers*, Feb. 1991, pp.142-143.

(2) I. A. Young, J. K. Greason, and K. L. Wong, "A PLL clock generator with 5 to 110MHz of lock range for microprocessors," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1599-1607, Nov. 1992.

(3) A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, pp. 790-804, June 1999.

(4) R. Navid, T. H. Lee, and R. W. Dutton, "An analytical formulation of phase noise of signals with Gaussian distribution jitter," unpublished.

(5) B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 31, pp. 331-343, Mar. 1996.

(6) J. G. Sneep and C. J. M. Verhoeven, "A new low-noise 100-MHz balanced relaxation oscillator," *IEEE J. Solid-State Circuits*, vol. 25, pp. 692-698, Jun. 1990.

(7) R. Navid and R. W. Dutton, "The physical phenomena responsible for excess noise in short-channel MOS devices," in *International Conference on Simulation of Semiconductor Processes and Devices* (*SISPAD*) *Dig. Tech. Papers*, Sep. 2002, pp. 75-78.