Thermal Modeling and Device Noise Properties of 3D-SOI Technology

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Introduction: Long interconnections in planar CMOS technologies are limiting system performance [1]. 3D-SOI technology utilizes the vertical dimension and is a promising solution to this problem. In this 0.18μm technology, three Fully-Depleted (FD) SOI wafers are bonded together and integrated using through-wafer vias [2]. The wafers are named TierA (**A**), TierB (**B**), and TierC (**C**), with A closest to the 675μm thick substrate. Fig. 1 shows the wafer stack.

However, 3D-SOI technology has challenging issues. Fig. 2a shows transistor performance degradation due to thermal-induced mobility reduction. Fig.2b shows diode performance degradation due to 3D packaging and parasitic resistive effects. These effects on circuit performance show opposite trends; an electro-thermal simulation is required to help circuit designers better predict actual circuit performance.

Experiments: A transistor (DUT) is surrounded by diode-connected MOSFETs, which act as heat sources to control the DUT temperature. The DUT has four connections to the gate, which can be used to measure gate resistance. The test chip is first placed in a hot chamber, and the temperature dependence of gate resistance is calibrated. The test chip is then placed in ambient, and heat sources are used to control the DUT temperature. Changes in gate resistance are measured to determine temperature [3].

The thermal time constant for self-heating can be determined by the AC output conductance technique [4].

Device noise is quantified by asymmetric ring oscillators (RO) [5] with channel lengths of 0.18μm (**1X**), 0.54μm (**3X**), and 1.08μm (**6X**).

Thermal Model and Electro-Thermal Simulations:

An experimentally-verified, physically-based thermal model valid for all operating conditions is developed (Fig. 3, Tbl. 1). Thermal resistance is normalized to total channel area [4]. The thermal model is compared to measurements for different operating conditions (Fig. 4).

Electro-thermal simulations were performed to predict the oscillation frequencies of ROs implemented on different tiers. For the first set of experiments, only one oscillator is turned on at any one time. Fig. 5 shows measured oscillation frequencies and simulation results. For the second set of experiments, all oscillators are turned on at the same time. Measurements and simulation results are plotted in Fig. 6. In Fig. 5-6, "Parasitic Effect only" is when temperature is set to 25°C for all tiers. "Thermal Effect only" is for parasitic resistances set to zero.

Discussion of Electro-Thermal results: Examining Fig. 5, C has the lowest oscillation frequency for 1X, and A has the lowest oscillation frequency for 3X and 6X (not shown). This is due to thermal effects being dominant in 1X, and 3D packaging effects being dominant in 3X and 6X. From Fig. 2a, drive current is lowest on C when thermal effects are dominant. Since the oscillators are nominally the same on all tiers, lower drive current translates to lower oscillation frequency. Thermal effects are dominant in 1X as they have a smaller area over which to dissipate heat. For 3X and 6X, heat dissipation is efficient enough that 3D packaging effects become dominant. From Fig. 2b, A has the lowest current when 3D packaging effects are dominant. Hence, A has the lowest oscillation frequency for 3X and 6X.

For Fig. 6, B has the lowest oscillation frequency for 1X, and A has the lowest oscillation frequency for 3X and 6X (not shown). When all oscillators are turned on at the same time, the operating temperature of B is much higher than when only one oscillator is on. This increase in temperature, as well as the ever-present parasitic effects, contributed to B having the lowest oscillation frequency for 1X.

The different observed dominant effects are validated using simulations (Fig. 5-6). Experimental oscillation frequencies vary as predicted by "Thermal Effect only" for 1X and "Parasitic Effect only" for 3X. Considering both effects as in "Electro-Thermal Simulation" gives the best match to actual circuit performance for all cases. Note that Fig. 2a is due to mobility degradation. As transistors approach the ballistic transport regime, drive current increases with temperature. In that case, A is expected to always have the worst performance, as both thermal and packaging effects work against it.

Device Noise: Device noise is quantified using the same ring oscillators [5]. Delta Phase Noise (DPN Fig. 7) is the difference between measured phase noise and the minimum achievable phase noise. This metric compensates for differences in power consumption and oscillation frequency of different oscillators, and is a figure of merit for device noise [6, 7]. Lower DPN means better device noise performance. Device noise improved by 13.7dB going from 1X devices to 3X devices. Further increase of channel length does not improve noise performance, which is consistent with a comparable 0.18μm bulk CMOS process [5].

For 3X, device noise performance is best on A and worst on C. This is consistent with having a temperature gradient between tiers. From measurements, temperature is lowest on A and highest on C. For long channel devices, this translates to the best device noise performance on A and worst on C.

The reverse is true for 1X: device noise performance is best on C and worst on A, even though C is the hottest.

This is because shot noise is dominant in short channel devices, and higher temperatures do not necessarily worsen device noise performance in this regime [5].

Conclusions: Performance of 3D-ICs is influenced by thermal effects as well as 3D packaging and parasitic effects. Actual circuit performance is difficult to predict as thermal and 3D packaging effects act in opposite ways. To provide design insight, a stacked wafer 3D-SOI technology was characterized and a thermal model was developed. Electro-thermal simulations of 3D-ICs were performed, and simulation results match measured data. Performance of the first (bottom) tier is expected to always be worst for advanced technology. Device noise is measured for this technology. Comparisons are made with a comparable 0.18µm bulk CMOS technology.

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References:

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TierC Active Layer
TierC Passive Layer
TierB Active Layer
TierB Passive Layer
TierA Passive Layer
TierA Active Layer
Substrate

Fig 1: Stackup of 3D-SOI technology.

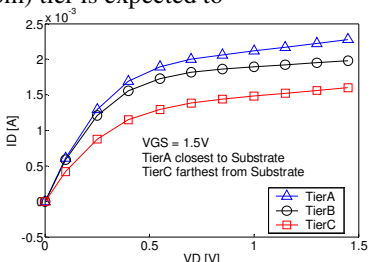


Fig 2a: Id-Vd curve of 3D-SOI NMOS, with VGS held at 1.5V. W/L = 6µm /0.2µm. The performance degradation of TierB and C is due to Thermal effects.

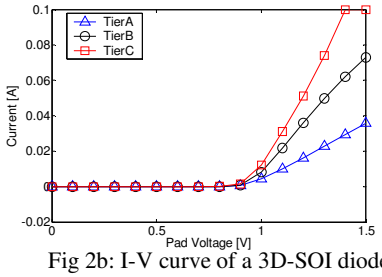


Fig 2b: I-V curve of a 3D-SOI diode. Performance degradation of TierA and B is due to 3D packaging (through-wafer vias) and other parasitic resistive effects.

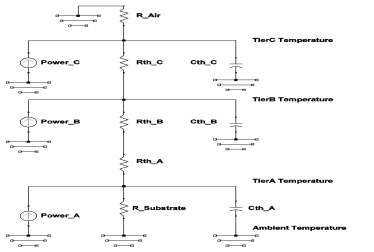
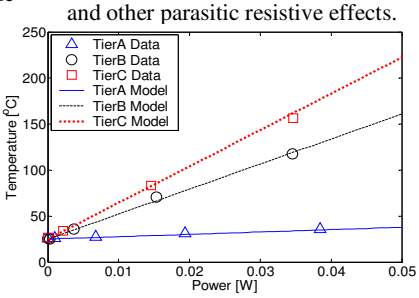


Fig. 3: Thermal model used in this work. Power is the electrical I*V product, and thermal resistances shown in Tbl. 1.

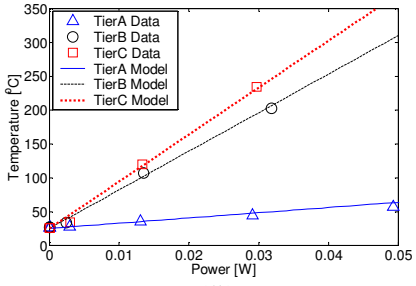
	Time Constant [s]	Normalized Thermal R [(K/W) * m^2]
R_Air	-	1.2e-3
TierC	3.9e-7	6.6528e-8
TierB	3.8e-7	6.6528e-8
TierA	3.2e-7	6.6528e-8
R_Substrate	-	1.391e-8

Tbl. 1: Table summarizing the thermal model. Thermal resistances normalized to total channel area.



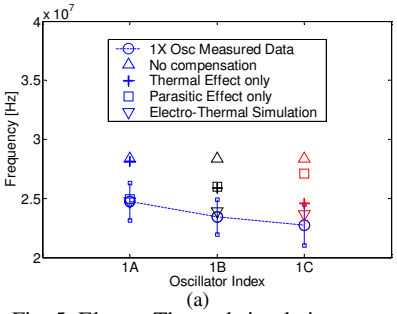
(4a)

Fig. 4: Figures comparing thermal model with measured temperatures. (a) Only one tier is active at any one time.

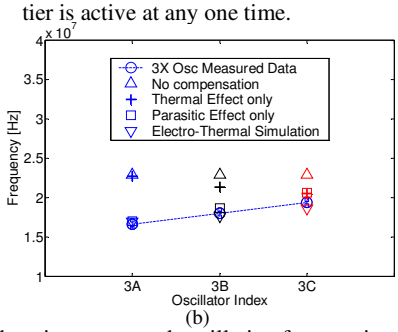


(4b)

(b) All three tiers active at the same time.

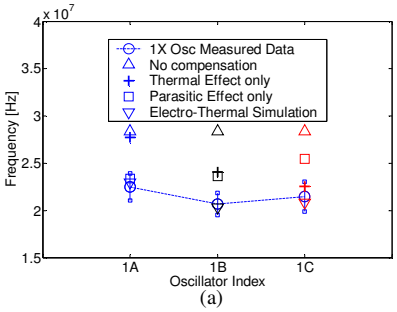


(a)

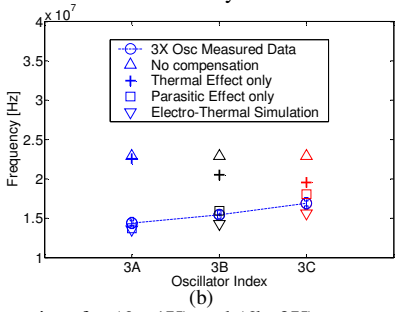


(b)

Fig. 5: Electro-Thermal simulations compared against measured oscillation frequencies for all three tiers. Only one oscillator ON at any one time for (5a, 1X) and (5b, 3X).



(a)



(b)

Fig. 6: All oscillators ON at the same time for (6a, 1X) and (6b, 3X).

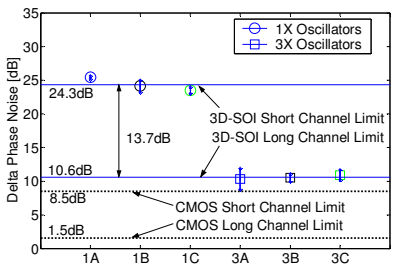


Fig. 7: Figure showing measured device noise for 1X devices and 3X devices.