

## Resume

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<b>Name</b>	Kyung Rok Kim
<b>Date &amp; place of birth</b>	Born on February 14, 1976 in Seoul, Republic of KOREA
<b>Present occupation</b>	Post-Doctoral Researcher
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### Education

Post-Doctoral Research Staff, Stanford TCAD Group, Stanford University, Sep. 2004 ~ present  
Ph. D. Electrical Engineering, Seoul National University, Seoul, Korea, Aug. 2004  
M.S. Electrical Engineering, Seoul National University, Seoul, Korea, Feb. 2001  
B.S. Electrical Engineering, Seoul National University, Seoul, Korea, Feb. 1999

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### Theme of Thesis

Implementation of algorithm and extraction tool to determine the effective channel length of CMOS device (BS thesis)  
Development of single-electron transistors based on electrically induced tunnel barriers by dual depletion gates (MS thesis)  
Silicon Quantum Tunneling Device Based on Band-to-Band Tunneling Mechanism(Ph.D. thesis)

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### Research Experience

Research assistant of electron-beam lithography system in inter-university semiconductor research center (ISRC @ SNU)  
TCAD-based model development for quantum-mechanical tunneling and quantization effect  
CMOS technology-based tunneling devices exploiting band-to-band tunneling  
Design and simulation of negative-differential resistance (NDR) devices

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### Skills

Circuit Simulation and Layout : HSPICE, Cadence tools  
Device simulators : MEDICI, DAVINCI, TAURUS (PMEI), Atlas, DESSIS  
Process simulators : TSUPREM4, DIOS, FLOOPS  
Silicon Process : Master of Electron-Beam Lithography, Photolithography, Dry/Wet Etch, LP/PE CVD, Oxidation, Ion Implantation... etc. (Experience of full CMOS process)  
Math : MATLAB, Mathematica

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## Publication List

### Journals (archival journal, refereed)

- [1] **Kyung Rok Kim**, Hyun Ho Kim, Ki-Whan Song, Jung Im Huh, Jong Duk Lee, and Byung Gook Park, "Field-Induced Inter-band Tunneling Effect Transistor (FITET) With Negative-Differential Transconductance and Negative-Differential Conductance," *IEEE Transactions on Nanotechnology*, Vol. 4, No. 3, pp. 317-321, May 2005.
- [2] **Kyung Rok Kim**, Dae Hwan Kim, Ki-Whan Song, Gwanghyeon Baek, Hyun Ho Kim, Jung Im Huh, Jong Duk Lee, and Byung Gook Park, "Silicon-Based Field-Induced Band-to-band Tunneling Effect Transistor," *IEEE Electron Device Letters*, Vol. 25, No. 6, pp. 439-441, June 2004.
- [3] **Kyung Rok Kim**, Ki-Whan Song, Dae Hwan Kim, Gwanghyeon Baek, Hyun Ho Kim, Jung Im Huh, Jong Duk Lee, Byung Gook Park, "Analytical Modeling of Realistic Single-Electron Transistors Based on Metal-Oxide-Semiconductor Structure with a Unique Distribution Function in the Coulomb-Blockade Oscillation Region," *Jpn. J. Appl. Phys.* Vol. 43, Part 1, No. 4B, pp.2031-2035, April 2004.
- [4] **Kyung Rok Kim**, Dae Hwan Kim, Jong Duk Lee, and Byung-Gook Park, "Coulomb Oscillations Based on Band-to-band Tunneling in a Degenerately Doped Silicon Metal-Oxide-Semiconductor Field-Effect Transistor," *Virtual Journal of Nanoscale Science & Technology*, Vol. 9, Issue 16, (APL Vol. 84, pp. 3178-3180), Apr. 2004.
- [5] **Kyung Rok Kim**, Dae Hwan Kim, Jong Duk Lee, Byung-Gook Park, "Coulomb Oscillations Based on Band-to-band Tunneling in a Degenerately Doped Silicon Metal-Oxide-Semiconductor Field-Effect Transistor," *Appl. Phys. Lett.*, Vol. 84, No. 16, pp. 3178~3180, Apr. 2004.
- [6] **Kyung Rok Kim**, Dae Hwan Kim, Suk-Kang Sung, Jong Duk Lee, and Byung-Gook Park, "Negative-differential transconductance characteristics at room temperature in 30-nm square-channel SOI nMOSFETs with a degenerately doped body," *IEEE Electron Device Letters*, Vol. 23, No. 10, pp. 612 -614, Oct. 2002.
- [7] **Kyung Rok Kim**, Dae Hwan Kim, Suk-Kang Sung, Jong Duk Lee, Byung-Gook Park, Bum Ho Choi, Sung Woo Hwang, and Doyeol Ahn, "Single-Electron Transistors with Sidewall Depletion Gates on a Silicon-On-Insulator Nano-Wire," *Jpn. J. Appl. Phys.*, Vol. 41, Part 1, No. 4B, pp. 2574-2577, Apr. 2002.
- [8] **Kyung Rok Kim**, Dae Hwan Kim, Jong Duk Lee, and Byung-Gook Park, "Characteristics of Silicon-On-Insulator Single-Electron Transistors with Electrically Induced Tunnel Barriers," *Journal of the Korean Physical Society*, Vol. 40, No. 1, pp. 140~144, Jan. 2002.
- [9] Ki-Whan Song, **Kyung Rok Kim**, Jong Duk Lee, Byung-Gook Park, Sang-Hoon Lee, and Dae Hwan Kim, "A SPICE Model of Realistic Single-Electron Transistors and Its Application to Multiple-Valued Logic," *Journal of Korean Physical Society*, Vol. 44, No. 1, pp. 121-124, Jan. 2004.
- [10] Byung-Gook Park, Dae Hwan Kim, **Kyung Rok Kim**, Ki-Whan Song, Jong Duk Lee, "Single-

electron transistors fabricated with sidewall spacer patterning," *Superlattices and Microstructures*, Vol. 34, pp. 231-239, September-December 2003.

[11] Dae Hwan Kim, Suk-Kang Sung, **Kyung Rok Kim**, Jong Duk Lee, and Byung-Gook Park, "Single-Electron Transistors Based on Gate-Induced Si Island for Single-Electron Logic Application," *IEEE Transactions on Nanotechnology*, Vol. 1, No. 4, pp. 170-175, Dec. 2002.

[12] Sang-Hoon Lee, Dae Hwan Kim, **Kyung Rok Kim**, Jong Duk Lee, Byung-Gook Park, Young-Jin Gu, Gi-Young Yang, and Jeong-Taek Kong, "A Practical SPICE Model Based on the Physics and Characteristics of Realistic Single-Electron Transistors," *IEEE Transactions on Nanotechnology*, Vol. 1, No. 4, pp. 226-232, Dec. 2002.

[13] Dae Hwan Kim, Suk-Kang Sung, **Kyung Rok Kim**, Jong Duk Lee, and Byung-Gook Park, "Fabrication of single-electron tunneling transistors with an electrically formed Coulomb island in a silicon-on-insulator nanowire," *Virtual Journal of Nanoscale Science & Technology*, Volume 6, Issue 25, (JVSTb Vol. 20, pp. 1410-1418), Dec. 2002.

[14] Dae Hwan Kim, Suk-Kang Sung, **Kyung Rok Kim**, Jong Duk Lee, Byung-Gook Park, Bum Ho Choi, Sung Woo Hwang and Doyeol Ahn, "Single-Electron Transistors with Sidewall Depletion Gates on an SOI Nanowire and Their Application to Single-Electron Inverters," *Journal of The Korean Physical Society*, Vol. 41, No. 4, pp. 505-508, Oct. 2002.

[15] Young Jin Choi, Byung Yong Choi, **Kyung Rok Kim**, Jong Duk Lee, and Byung-Gook Park, "A new 50-nm NMOSFET with side-gates for virtual source-drain extensions," *IEEE Transactions on Electron Devices*, Vol. 49, No. 10, pp. 1833-1835, Oct. 2002.

[16] Dae Hwan Kim, Suk-Kang Sung, **Kyung Rok Kim**, Jong Duk Lee, and Byung-Gook Park, "Fabrication of single-electron tunneling transistors with an electrically formed Coulomb island in a silicon-on-insulator nanowire," *J. Vac. Sci. Technol. B.*, Vol. 20, Issues 4, pp. 1410-1418, Jul. 2002.

[17] Dae Hwan Kim, **Kyung Rok Kim**, Suk Kang Sung, Jong Duk Lee, and Byung-Gook Park, "Dynamic exclusive-OR gate based on gate-induced Si island single electron transistor," *IEE Electronics Letters*, Vol. 38, No. 11, pp. 527~529, May 2002.

[18] Suk-Kang Sung, Dae Hwan Kim, Jae-Sung Sim, **Kyung Rok Kim**, Yong Kyu Lee, Jong Duk Lee, Soo Doo Chae, Byung Man Kim, and Byung-Gook Park, "Single-Electron MOS Memory with a Defined Quantum Dot Based on Conventional VLSI Technology," *Jpn. J. Appl. Phys.*, Vol. 41, Part 1, No. 4B, pp. 2606-2610, Apr. 2002.

[19] Dae Hwan Kim, Suk-Kang Sung, **Kyung Rok Kim**, Jong Duk Lee, Byung-Gook Park, Bum Ho Choi, Sung Woo Hwang, Doyeol Ahn, "Silicon single-electron transistors with sidewall depletion gates and their application to dynamic single-electron transistor logic," *IEEE Transactions on Electron Devices*, Vol. 49, NO. 4, pp. 627-635, Apr. 2001.

[20] D. H. Kim, S.-K. Sung, J. S. Sim, **K. R. Kim**, J. D. Lee, B.-G. Park, B. H. Choi, S. W. Hwang, and D. Ahn, "Single-electron transistor based on silicon-on-insulator quantum wire fabricated by a side-wall patterning method," *Appl. Phys. Lett.*, Vol. 79, pp. 3812~3814, Dec. 2001.

**Conferences (refereed)**

- [1] **Kyung Rok Kim** and Robert W. Dutton, "Effects of Local Electric Field and Effective Tunnel Mass on the Simulation of Band-to-Band Tunnel Diode Model," to be presented at Int'l Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Tokyo Japan, September 2005.
- [2] **Kyung Rok Kim**, Hyun Ho Kim, Ki-Whan Song, Jung Im Huh, Jong Duk Lee, and Byung-Gook Park, "SOI MOSFET-Based Quantum Tunneling Device - FIBTET," 62nd Annual Device Research Conference, pp. 217-218, Indiana, USA, June. 21-23, 2004.
- [3] **Kyung Rok Kim**, Hyun Ho Kim, Jung-Im Huh, Dae Hwan Kim, Ki-Whan Song, Jong Duk Lee, and Byung-Gook Park, "Field Induced Band-to-Band Tunneling Effect Transistor - FIBTET with Negative-Differential Transconductance and Negative-Differential Conductance Characteristics," IEEE 2004 Silicon Nanoelectronics Workshop, Honolulu, Hawaii, USA, pp. 11-12, Jun. 13-14, 2004.
- [4] **Kyung Rok Kim**, Gwanghyeon Baek, Ki-Whan Song, Hyun Ho Kim, Jung-Im Huh, Jong Duk Lee, and Byung-Gook Park, "Silicon MOSFET-based Field Induced Band-to-Band Tunneling Effect Transistor – FIBTET", 2003 Int'l Semiconductor Device Research Symposium, Washington, USA, Dec. 10-12, 2003.
- [5] **Kyung Rok Kim**, Ki-Whan Song, Gwanghyeon Baek, Hyun Ho Kim, Jung Im Huh, Jong Duk Lee, Byung Gook Park, "Analytical SPICE Modeling of Realistic MOS-based Single-Electron Transistors-"MOSETs" with a Unique Distribution Function in the Coulomb Oscillation Region," Int'l Conf. on Solid State Devices and Materials 2003, pp.330-331, Tokyo, Japan, Sept. 16-18, 2003.
- [6] **Kyung Rok Kim**, Dae Hwan Kim, Ki-Whan Song, Sang-Hoon Lee, Jaewoo Kyung, Jong Duk Lee, and Byung-Gook Park, "Observation of Single-Electron Charging Effects Based on Band-to-band Tunneling in a MOS-based Single-Electron Transistor-"MOSET" ", IEEE 2003 Silicon Nanoelectronics Workshop, Kyoto, Japan, pp. 72-73, June 8-9, 2003.
- [7] **Kyung Rok Kim**, Dae Hwan Kim, Jong Duk Lee, and Byung-Gook Park, "Room Temperature Negative Differential Conductance Characteristics in 30-nm Square Channel Silicon-On-Insulator n-MOSFETs", IEEE 2002 Silicon Nanoelectronics Workshop, Honolulu, Hawaii, U.S.A, pp. 9-10, Jun. 9-10, 2002.
- [8] **K. R. Kim**, D. H. Kim, S. K. Sung, J. D. Lee, B.-G. Park, B. H. Choi, S. W. Hwang, and D. Ahn, "Single Electron Transistors with Sidewall Depletion Gates on a Silicon-On-Insulator Nano-Wire," Int'l Conf. on Solid State Devices and Materials 2001, pp.552-553, Tokyo, Japan, Sept. 26-28, 2001.
- [9] **Kyung Rok Kim**, Dae Hwan Kim, Jong Duk Lee, Byung-Gook Park, "Single Electron Transistors Based on Silicon-On-Insulator Wire Patterened by Sidewall Masking Technology and Electrically Induced Tunnel Barriers," 2001 Silicon Nanoelectronics Workshop, pp. 42-43, Kyoto, Japan, Jun. 10-11, 2001.
- [10] **Kyung Rok Kim**, Dae Hwan Kim, Jong Duk Lee, Byung-Gook Park, "Characteristics of Silicon-On Insulator Single Electron Transistors with Electrically Induced Tunnel Barriers," The 8th Korean Conference on Semiconductors, pp. 155-156, Seoul, Korea, Feb. 14-15, 2001.

- [11] **Kyung Rok Kim**, Dae Hwan Kim, Jong Duk Lee, Byung Gook Park, "A study of Single Electron Logic Characterization Using a SPICE Macro-Modeling", IEEK Summer Conference 2000, pp111-114 June, 2000.
- [12] Hyun Ho Kim, **Kyung Rok Kim**, Jung-Im Huh, Ki-Whan Song, Il-Han Park, Jong Duk Lee and Byung-Gook Park, "Room Temperature Characteristics in Single-Electron Transistors with a Quantum Dot Formed by Anisotropic TMAH Wet Etch," IEEE 2004 Silicon Nanoelectronics Workshop, Honolulu, Hawaii, U.S.A, pp. 79-80, June 13-14, 2004.
- [13] Jung Im Huh, Dae Hwan Kim, **Kyung Rok Kim**, Hyun Ho Kim, Ki-Whan Song, Jong Duk Lee and Byung-Gook Park, "Coupled Parallel Quantum Dots in Silicon Single-Electron Transistors by the Three-Dimensional Field Effects," IEEE 2004 Silicon Nanoelectronics Workshop, Honolulu, Hawaii, U.S.A, pp. 83-84, June 13-14, 2004.
- [14] Gwanghyeon Baek, Ki-Whan Song, Yong Kyu Lee, Kyung Rok Kim, Byung Yong Choi, Jong Duk Lee, Byung-Gook Park, "Fabrication of Single-Electron Transistors and CMOS Devices on a SOI Wafer," The 11th Korean Conference on Semiconductors, Seoul, Korea, vol. 1, pp. 387-388, Feb. 19-20, 2004.
- [15] Ki-Whan Song, Gwanghyeon Baek, Sang-Hoon Lee, Dae Hwan Kim, **Kyung Rok Kim**, Dong-Soo Woo, Jae Sung Sim, Jong Duk Lee, and Byung-Gook Park, "Realistic Single-Electron Transistor Modeling and Novel CMOS/SET Hybrid Circuits," 2003 Thrid IEEE Conference on Nanotechnology(IEEE-NANO 2003), pp.119-121, San Francisco, CA, USA, Aug. 12-14, 2003.
- [16] Ki-Whan Song, Sang Hoon Lee, Dae Hwan Kim, **Kyung Rok Kim**, Jaewoo Kyung, Gwanghyeon Baek, Chun-An Lee, Jong Duk Lee, and Byung-Gook Park, "Complementary Self-Biased Scheme for the Robust Design of CMOS/SET Hybrid Multi-Valued Logic," 33rd International Symposium on Multiple-Valued Logic, Tokyo, Japan, pp.267-272, May 16-19, 2003.
- [17] Chang Ju Lee, Suk-Kang Sung, Yong Kyu Lee, **Kyung Rok Kim**, Jae Seong Sim, Tae Hun Kim, Ji Hye Kong, Jong Duk Lee, and Byung-Gook Park, "70-nm-long and 30-nm-wide Channel SONOS Memory Fabricated on an SOI Wafer," The 10th Korean Conference on Semiconductors, Seoul, Korea, pp. 581-582, Feb. 27-28, 2003.
- [18] Sang-Hoon Lee, Ki-Whan Song, Dae Hwan Kim, **Kyung Rok Kim**, Jong Duk Lee, Byung-Gook Park, Young-Jin Gu, Gi-Young Yang, Young-Kwan Park, and Jeong-Taek Kong, "A SPICE Model of Realistic Single-Electron Transistors and its Application to Multiple-Valued Logic," The 10th Korean Conference on Semiconductors, Seoul, Korea, pp. 109-110, Feb. 27-28, 2003.
- [19] Chang Ju Lee, Suk-Kang Sung, Yong Kyu Lee, **Kyung Rok Kim**, Jae Seong Sim, Tae Hun Kim, Ji Hye Kong, Jong Duk Lee, and Byung-Gook Park, Soo doo Chae, and Chung woo Kim, "70-nm-long and 30-nm-wide Channel SONOS Memory Fabricated on an SOI Wafer," IEEE Non-Volatile Semiconductor Memory Workshop, Monterey, CA, USA, pp. 69-70, Feb. 16-20, 2003.
- [20] Young Jin Choi, Byung Yong Choi, Dong-Soo Woo, **Kyung Rok Kim**, Woo Young Choi, Cheon Ahn Lee, Jong Duk Lee, and Byung-Gook Park, "A New Side-gate nMOSFET with 50nm

Gate Length", IEEE 2002 Silicon Nanoelectronics Workshop, Honolulu, Hawaii, U.S.A, pp. 13-14, June 9-10, 2002.

[21] Dae Hwan Kim, Suk-Kang Sung, **Kyung Rok Kim**, Jong Duk Lee, and Byung-Gook Park, "Single-Electron Transistors Based on Gate-Induced Si Island for Single-Electron Logic Application", IEEE 2002 Silicon Nanoelectronics Workshop, Honolulu, Hawaii, U.S.A, pp. 57-58, June 9-10, 2002.

[22] Young Jin Choi, Byung Yong Choi, Dong-Soo Woo, **Kyung Rok Kim**, Woo Young Choi, Cheon Ahn Lee, Jong Duk Lee, and Byung-Gook Park, "A New 50nm nMOSFET with Side-Gates for Virtual Source/Drain Extension," The 9th Korean Conference on Semiconductors, Chunan, Korea, pp. 65-66, Feb. 21-22, 2002.

[23] Dae Hwan Kim, Suk-Kang Sung, **Kyung Rok Kim**, Jong Duk Lee, and Byung-Gook Park, "Single-Electron Transistors with Sidewall Depletion Gates on an SOI Nanowire and Their Application to Single-Electron Inverter," The 9th Korean Conference on Semiconductors, Chunan, Korea, pp. 91-92, Feb. 21-22, 2002.

[24] Dae Hwan Kim, Suk-Kang Sung, **Kyung Rok Kim**, Bum Ho Choi, Sung Woo Hwang, Doyeol Ahn, Jong Duk Lee, and Byung-Gook Park, "Si Single-Electron Transistors with Sidewall Depletion Gates and their Application to Dynamic Single-Electron Transistor Logic", International Electron Devices Meeting, Washington DC, U.S.A., pp. 151-154, Dec. 2~5, 2001.

[25] Woo Young Choi, Suk Kang Sung, **Kyung Rok Kim**, Jong Duk Lee, and Byung-Gook park, "Nanoscale Poly-Si Line Formation and Its Uniformity," 2001 Asia-Pacific Workshop on Fundamental and Application of Advanced Semiconductor Devices, pp. 11-16, Cheju, Korea, Jul. 4-7, 2001.

[26] D. H. Kim, **K. R. Kim**, S. K. Sung, B. H. Choi, S. W. Hwang, D. Ahn, J. D. Lee, B.-G. park, "Single Electron Transistors with Sidewall Depletion Gates on a Silicon-On-Insulator Quantum Wire," 59th Annual Device Research Conference, pp. 133-134, Notre Dame, Indiana, USA, Jun. 25-27, 2001.

[27] Dae Hwan Kim, Dong-Hyuk Chae, Suk-Kang Sung, **Kyung Rok Kim**, Jong Duk Lee, and Byung-Gook Park, "Room Temperature SETL-Oriented Dual Gate Single Electron Transistor and its Modeling," The 7th Korean Conference on Semiconductors, pp.297~298, January, 2000.

#### **Other Papers/Talks (non-refereed or invited)**

[1] Byung-Gook Park, **Kyung Rok Kim**, Ki-Whan Song, Hyun Ho Kim, Jung Im Huh, and Jong Duk Lee, "Silicon Quantum Tunneling Devices - FIBTET and MOSET," Int'l Conf. on Solid State Devices and Materials 2004, Tokyo, Japan, pp. 120-121, September 15-17 2004.

[2] Byung-Gook Park, Dae Hwan Kim, **Kyung Rok Kim**, Ki-Whan Song, and Jong Duk Lee, "Single-Electron Transistors Fabricated with Sidewall Spacer Patterning," 6th International Conference on New Phenomena in Mesoscopic Structures 6 Surfaces and Interfaces in Mesoscopic

Devices 4, pp.108-109, Hawaii, USA, Nov. 30-Dec. 5, 2003.

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**Patents**

Korean patent No. 444,270, Aug. 3, 2004.

U. S. patent No. 6,800,511, Oct. 5, 2004

“Method for fabricating semiconductor device with negative differential conductance or transconductance

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