Resume for Francis M. Rotella

CONTACT & AFFILIATIONS

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Senior Member of IEEE
Member of RFIC Symposium Technical Program Committee on "Modeling and CAD"

WORK EXPERIENCE

5/07 - **Manager, Device Modeling.** Peregrine Semiconductor, San Diego, CA 92121
- Responsible for delivering models and developing LPE decks for silicon on sapphire process.
- Define direction for modeling group, establish priorities, and allocate resources.
- Co-ordinate with Technology, CAD, and Design groups to align projects to meet company goals.
- Individual contributor on tasks including model extraction, equipment configuration, LPE methodology, model library development, and any project where my skills are needed.
- Mentor and guide junior members of the modeling team.

1/05 - 5/07 **Member of Research Staff.** Fujitsu Laboratories of America, Sunnyvale, CA 94085
- Established and managed an RF modeling and RFIC measurement lab (up to 65GHz)
- Supported measurement strategy and characterization of a 40Gbs CDR.
- Developed models for transmission lines and passive components for circuit design needs.
- Updated BSIM4 digital FET models to be represent RF characteristics of physical device.
- Developed a research program for RF CMOS PA, established a measurement methodology, evaluated transistor performance from initial test chip, and transferred results to group in Japan.

9/99 - 12/04 **Principal Electrical Engineer.** Skyworks Solutions (Conexant Systems spin-off), Irvine, CA 92612
- Lead multiple projects on characterization test chips and statistical model library development.
- Developed, implemented, and supported circuit models for on-chip inductors in Silicon and GaAs. Provided best practice guidelines to design community.
- Supported electromagnetic simulation and model generation of passive components. Provided analysis and modeling for coupling of on-chip components, traces, and bond wires.
- Supported RF passive and varactor model development and extraction.
- Assisted design community with optimization of LC tank circuit, filters, and baluns.
- Experience in RF & analog characterization test structure design and layout.
- Provided high frequency evaluation of foundry processes and validation of models.
- Provided bond pad design and guidelines on substrate isolation.
- Managed projects for embedded passive development in multiple package technologies.
- Provided guidance and mentored junior engineers in package modeling group.

6/98 - 7/99 **Device and Process Development Engineer.** Spectrian, Sunnyvale, CA 94089
- Responsible for TCAD analysis/optimization of RF power devices.
- Responsible for development of multi-layer metal process and RFIC passive components.
- Worked on team evaluating HCI of high BV LDMOS FET's.
- Provided input on all R&D issues relating to current technology.

SUMMARY OF PUBLICATIONS & PATENTS

PATENTS: Two patents issued on passive device design and implementation in a CAD environment.
PAPERS: Over 10 first author publications on RF modeling, device design, and design for manufacturing
Over 20 papers total including collaboration with colleagues on circuit design

EDUCATION

June 2000 **Stanford University.** Stanford, CA 94305
Ph.D. in Electrical Engineering

Dissertation: *Mixed Circuit and Device Simulation for Analysis, Design, and Optimization of Opto-Electronic, Radio Frequency, and High Speed Semiconductor Devices*.

Florida Institute of Technology. Melbourne, FL 32905
March 1992 MSEE Major depth in semiconductor device physics.
June 1990 BSEE Course work focused on electronic circuits.

Master's Thesis: *Effect of Emitter Width on the Current Gain of a Bipolar Junction Transistor.*

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SOFTWARE AND LABORATORY SKILLS

CAD TOOLS: Cadence (Virtuoso & Analog Artist), PISCES, Raphael, IE3D, Sonnet EM, HFSS, RFDE, ADS

LAB TOOLS: On-wafer RF probing, MATLAB Instrument Control Toolbox, ICCAP, VNA Calibration and De-embedding schemes, GPIB programming, Maury ATS Software, Load-Pull for Power

SOFTWARE: Matlab (Optimization Toolbox, Compiler Toolbox), HTML, C and Fortran programing, UNIX shell scripts, some Skill, ability to use scripting languages to complete work efficiently

WORK EXPERIENCES DURING UNIVERISTY STUDIES

6/96 - 3/98 **Research Consultant (Part Time) and Summer Position (Intern).** Motorola, Tempe, AZ 85284

- Modeled and analyzed discrete RF power devices (LDMOS) with surrounding parasitic circuitry in order to optimize gain and efficiency in power amplifier circuits.

6/95-9/95 **Associate Engineer (Intern).** International Business Machines, Burlington, VT 05405

- Developed an IBM mixed circuit/device simulator and applied to SRAM alpha particle errors.

9/93 - 1/94 **Research Consultant (Part Time).** Hewlett Packard, San Jose, CA 95131

- Simulation of radiation pattern & efficiency to optimize a hetero-structure LED material layers.

1988 - 1992 **Associate Engineer (Intern).** Harris Semiconductor (now Intersil), Palm Bay, FL 32902

- Multiple summer positions over a four year period focusing on design for manufacturing.
- Analyzed statistical circuit and device simulations to extract circuit model parameters.
- Worked on a development team for an engineering and process characterization database.
- Developed an expert system for individual photo-lithography process steps based on historical measurements.

UNIVERSITY RESEARCH EXPERIENCE

9/92 - 6/98 **Research Assistant.** Stanford University, Stanford, CA 94305

- Mixed circuit and device simulation, modeling, and analysis of high frequency power devices, optical devices, and high speed devices utilizing circuit and device simulators.
- University software development.
- Interacted with IBM, HP, Motorola, Ericsson

Dissertation: *Mixed Circuit and Device Simulation for Analysis, Design, and Optimization of Opto-Electronic, Radio Frequency, and High Speed Semiconductor Devices*.

10/89 - 3/92 **Research Assistant.** Florida Institute of Technology, Melbourne, FL 32905

- Researched statistical simulations of integrated circuit processing and individual device operation to support a design for manufacturing system (refer to publications).
- Help develop a semiconductor process laboratory course.
- Hands-on experience with unit process, transistor, and unit cell design.
- Interacted with Harris Semiconductor

Master's Thesis: *Effect of Emitter Width on the Current Gain of a Bipolar Junction Transistor.*

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LIST OF PATENTS

#6,588,002 Method and system for predictive layout generation for inductors with reduced design cycle.

#7,135,366 Method for fabricating a lateral metal-insulator-metal capacitor and a capacitor fabricated according to the method.

INDUSTRY PUBLICATIONS

Primary Contributor

"Design, Characterization, Modeling, and Model Validation of Silicon on-Wafer M:N Balun Components under Matched and Mis-Match Conditions." F. Rotella, C. Cismaru, G. Tkachenko, Y. Cheng, and P. Zampardi. *Journal of Solid State Circuits.* May 2006.

"Design, Characterization, Modeling, and Model Validation of Silicon on-Wafer M:N Balun Components under Matched and Mis-Match Conditions." F. Rotella, G. Tkachenko, and Y. Cheng. RFIC Symposium, June 2005.

"A Broad-Band Lumped Element Inductor Model Incorporating Skin Effect and Substrate Loss for Technology Performance Assessment and RFIC Design." F. Rotella, B. Bhattacharya, V. Blaschke, M. Matloubian, A. Brotman, Y. Cheng, R. Divecharia, D. Howard, K. Lampaert, P. Miliozzi, M. Racanelli, P. Singh, and P. Zampardi. *Transactions on Electron Devices*. July 2005.

"Characterizing and Optimizing High Q Inductors for RFIC Design in Silicon Processes." F. Rotella, D. Howard, M. Racanelli, and P. Zampardi. RFIC Symposium, June 2003.

"A Broad-Band Scalable Lumped-Element Inductor Model Using Analytic Expressions to Incorporate Skin Effect, Substrate Loss, and Proximity Effect." F. Rotella, V. Blaschke, and D. Howard. IEDM, Dec. 2002.

"Modeling and Optimization of Inductors with Patterned Ground Shields for a High Performance Fully Integrated Switched Tuning VCO." F. Rotella and J. Zachan. CICC. May 2002.

Contributing Author

"A 40-to-44Gb/s 3x Oversampling CMOS CDS/1:16 DEMUX." N. Nedovic, N. Tzartzanis, H. Tamura, F. Rotella, M. Wiklund, Y. Mizutani, Y. Okaniwa, T. Kuroda, J. Ogawa, & W. Walker. *Journal of Solid State Circuits.* Dec. 2007.

"A 40-to-44Gb/s 3x Oversampling CMOS CDS/1:16 DEMUX." N. Nedovic, N. Tzartzanis, H. Tamura, F. Rotella, M. Wiklund, J. Ogawa, W. Walker. ISSCC, Feb. 2007.

"Linearity Analysis of RF LDMOS Devices Utilizing Harmonic Balance Device Simulation." O. Tornblad, C. Ito, F. Rotella, G. Ma, & R. Dutton. SISPAD, Sept. 2005.

"Analysis of RF Flip-Chip On-Chip Inductance." G. Lee, M. Megahed, F. Rotella, and F. De Flaviis. European Microwave Conference, Sept. 2002.

UNIVERSITY PUBLICATIONS

Primary Contributor

"Modeling, Analysis, and Design of RF LDMOS Devices Using Harmonic Balance Device Simulation." F. Rotella, G. Ma, Z. Yu, and R. Dutton. *Transactions on Microwave Theory and Techniques*. June 2000.

"Design Optimization of RF Power MOSFET's Using Large Signal Analysis Device Simulation of Matching Networks." F. Rotella, G. Ma, Z. Yu, and R. Dutton. SISPAD, Sept. 1998.

"Harmonic Balance Device Analysis of an LDMOS RF Power Amplifier with Parasitics and Matching Network." F. Rotella, B. Troyanovsky, Z. Yu. R. Dutton, and G. Ma. SISPAD, Sept. 1997.

"Integrated Circuit Design For Manufacturing Through Statistical Simulations of Process Steps." T. Sanders., K. Rekab, D. Means, and F. Rotella. *Transactions on Semiconductor Manufacturing*. Nov. 1992.

"Techniques for Optimizing Statistical Simulations." F. Rotella and T. Sanders. University/ Government/ Industry Microelectronics Symposium, May 1991.

"IC Process Design for Manufacturing Methodology." F. Rotella and T. Sanders. Florida Microelectronics Conference, May 1990.

Contributing Author

"Device Simulation for RF Applications." R. W. Dutton, B. Troyanovsky, Z. Yu, T. Arnborg, F. Rotella, G. Ma, J. Sato-Iwanaga. IEDM, Dec. 1997.

"Large Signal Analysis of RF/Microwave Devices with Parasitics Using Harmonic Balance Device Simulation." B. Troyanovsky, F. Rotella, Z. Yu, R. Dutton, and J Sato-Iwanaga. SASIMI, Nov. 1996.

"Device and Circuit Simulation for Heterogeneous Technology." Z. Yu, F. Rotella, B. Troyanovsky, and R. Dutton. SASIMI, Nov. 1995.

"Layout-based Extraction of IC Electrical Behavior Model." K. Wang, F. Rotella, T. Chen, D. Yang, A. Lee, Z. Yu, R.W. Knepper, J. Watt, and R.W. Dutton. IEDM Software Showcase, Dec. 1994.

"Next-Generation Stanford TCAD---SUPREM 007 and PISCES 2ET." S. Beebe, F. Rotella, Z. Sahul, D. Yergeau, G. McKenna, L. So, Z. Yu, K.C. Wu, E. Kan, J. McVittie, and R. W. Dutton. IEDM Software Showcase, Dec. 1994.

"Integrated TCAD for OEIC Applications." R.W. Dutton, F. Rotella, L. So, and Z. Yu. SPIE International Symposium, Jan. 1994.

"Statistical Design Methodology for Integrated Circuit Technology." T. Sanders., K. Rekab, D. Means, and F. Rotella. Government Microcircuit Applications Conference, Nov. 1991.