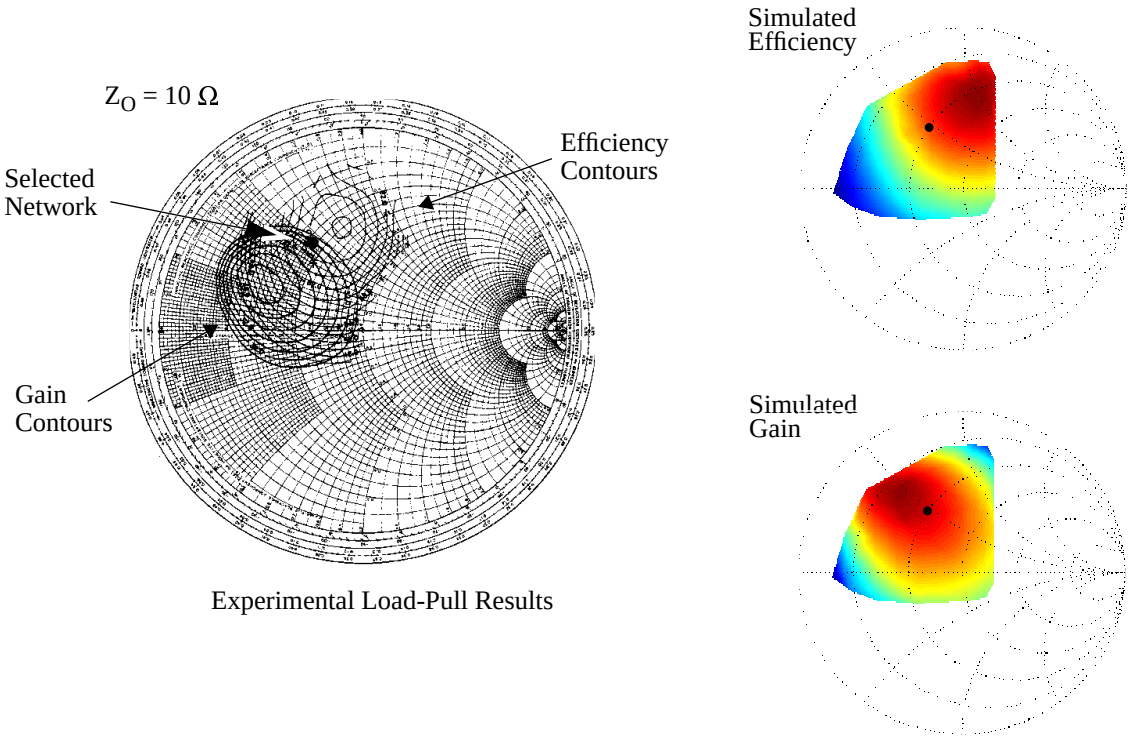

Figure 4: Comparison of e xperimental and simulated load-pull analysis. The dark en point represents that matching network used in the earlier RF response.

5. Conclusions

This paper addresses the modeling of an LDMOS transistor and its optimization using harmonic balance simulation. Given a tuned model, the ef fects of matching netw orks are e xamined through a load-pull simulation. These simulations have been completed systematically in order to pre vent erroneous results and incorrect conclusions.

6. Acknowledgments

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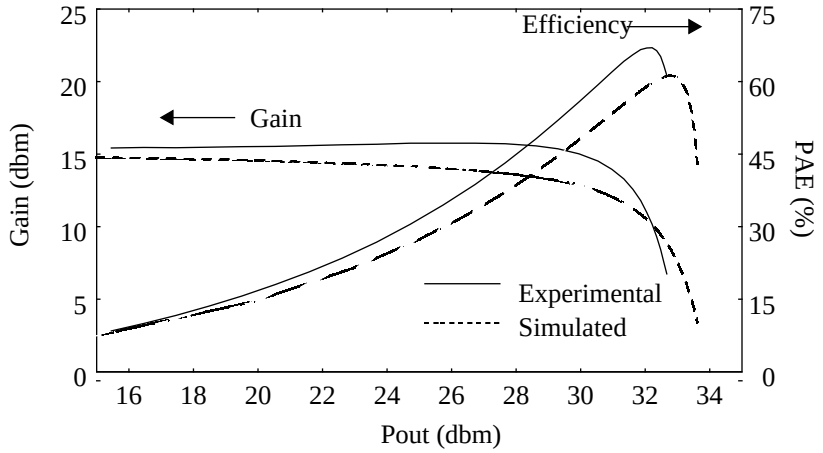


Figure 3: RF responses for gain and efficiency of a power amplifier.

more power in Class A operation. Efficiency increases until just after the gain starts to decrease. At this point, P_{out} approaches P_{in} resulting in a lower power added efficiency (PAE) to the input signal. Simulation shows good agreement with the experimental results.

4. Optimization of Matching Networks (Load-Pull)

Gain and efficiency depend upon the matching networks that connect the signal source and load to the amplifier. One of the important design choice is to make sure that a good matching network allows for a smooth impedance transition from the input signal to the input impedance of the amplifier and then to the load impedance. The goal is to have the network transmit at the fundamental frequency without reflections or attentuation due to filtering and likewise have the network filter out higher order harmonics without reflections back into the amplifier.

The input and output matching networks have only limited interactions with each other and are thus tuned independently. The input matching network is tuned to minimize reflections back to the signal source using a best guess for the output matching network. To determine the best output matching network, the reflection coefficient looking towards the load (Γ_{load} in Fig. 2) is swept across a range of values over which the best response is expected (i.e. a load-pull)[4]. For each matching network, the gain and efficiency is measured for a constant input power and plotted over the range of the network's reflection coefficients.

Fig. 4 shows experimental contour plots for gain and efficiency on a Smith chart which is used to represent the different reflection coefficients of the output matching network. The darken point on the graphs indicates the matching network used to generate the earlier plot of gain and efficiency. The selection criteria for this point depend upon the application for the device. The alignment of the maxima and the shape of the contours demonstrate that the simulated results (Fig. 4) agree with the experimental data.

There are some problems with the load-pull simulation. Load-pull equipment is designed to optimize the impedance for a specific reflection coefficient given that a reflection coefficient can be realized by multiple combinations of impedances. In simulation the impedance is set to obtain a specified reflection coefficient. If this impedance is chosen poorly, reflections back into the structure or filtering may affect the performance of the device in unexpected ways. Hence, care has been taken so that the choice of components maximizes the performance of the device for a given reflection coefficient of the output matching network.

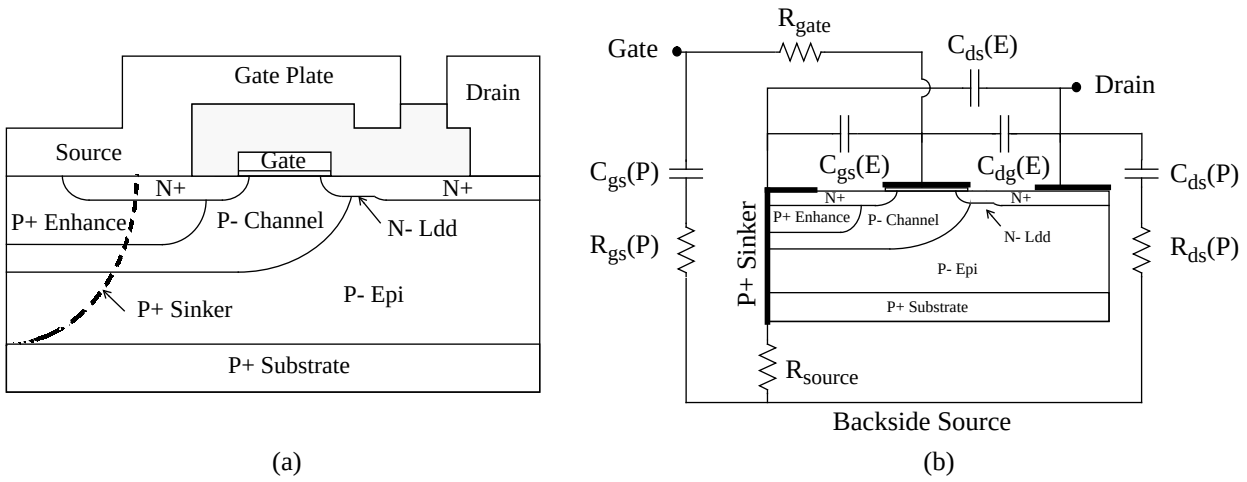
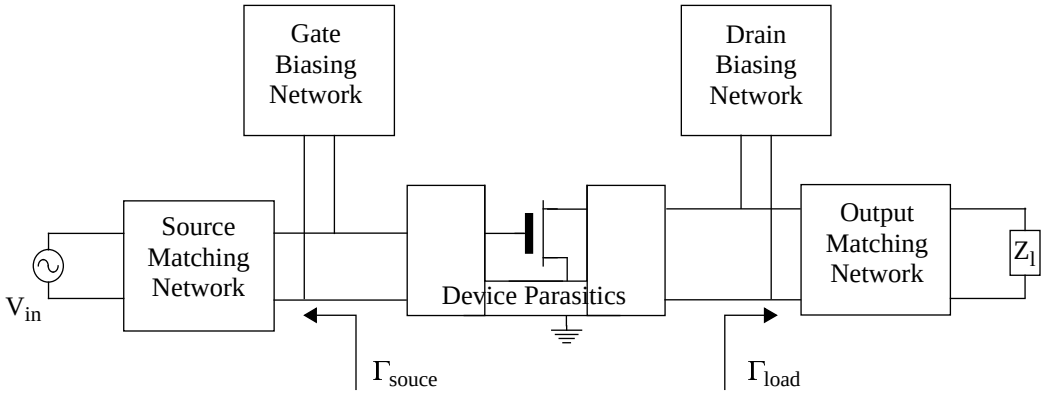


Figure 1: (a) RF LDMOS power device and (b) model showing parasitic components.



3. Modeling of the Device Including Parasitics

The LDMOS de vice is typically embedded among parastics from the package and interconnects. PISCES 2-HB has been enhanced to include linear network extensions for these boundary conditions. The values of these circuit components are determined by one of the follo wing three methods: (1) measured data from test structures (for e xample, the P+ sink ers); (2) simulations of the indi vidual structures (for example, the capacitance of the contact structure); (3) I-V and C-V curv e fit to e xtract the component values (for example, the slope of I_d vs. V_g curve dependence upon R_{source}). In most cases, the values of the components are verified by at least one other method.

Given a calibrated model that matches I-V and C-V characteristics, modeling the RF response of the network in Fig. 2 is the next goal. Input and output matching networks connect the large signal source and load to the de vice which serves as an amplifier where a parallel set of netw orks provide biasing. Fig. 3 shows the important RF responses of gain and efficiency from both measurement and simulation. The gain rolls off at higher po wer levels because the de vice begins to operate in g_m compression and the output power is limited by the saturation current. The ef ficiency is low for small P_{out} because the de vice drains

Design Optimization of RF Power MOSFET's Using Large Signal Analysis Device Simulation of Matching Networks

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Abstract

This paper discusses the modeling and simulation of power MOSFET's using large signal device simulation. In order to provide an accurate representation of an LDMOS MOSFET, a model for the intrinsic device and the extrinsic parasitic components is developed. The RF performance of the model is then verified with experimental data. With the proven model, the effect of parasitic components is analyzed and the matching networks are optimized for the desired response.

1. Introduction

To evaluate the device performance in a realistic applications, RF devices have to be simulated with appropriate biasing/matching circuits included. This paper addresses the analysis/design from a coupled device and circuits point of view using an LDMOS RF power amplifier. Important differences (and trade-offs) in gain and efficiency are clarified and then used for improved design of the overall circuit (bias and matching). Device simulator capabilities are reported for large signal analysis, including linear circuit elements. Simulated I-V and C-V data closely match measurements; proper matching circuitry can be optimized to deliver the maximum output power for practical RF components.

2. Simulation Methodology of Intrinsic Device

The device under analysis is an LDMOS structure from Motorola (Fig. 1a)[1][2]. The channel region is formed by lateral diffusion to exploit the built-in electric field for enhancement of the transconductance and reduction of carrier transit time. A source side p+ sinker connects source and substrate together to eliminate extra bonding wires and provide for a backside contact. An LDD region reduces the peak electric field at the drain region and a metal field plate over the gate (separated by an insulator) reduces the electric field at the edge of the gate.

The device model used in PISCES needs to be configured such that it may be efficiently used in an harmonic balance simulation[3]. Harmonic balance simulation dramatically increases the size of the system matrix. To overcome this limitation, the number of nodes in the device simulation is reduced by removing regions of the device where detailed physics are not essential and replaced by circuit components as shown in Fig. 1b. The surface electrodes are replaced with capacitances since they are assumed constant across all biases. The p+ sinker is replaced by an electrode and resistance to represent the contact from the surface to the backside of the device. By judiciously modeling these areas of the device, the total number of nodes in the system is reduced by 30%.