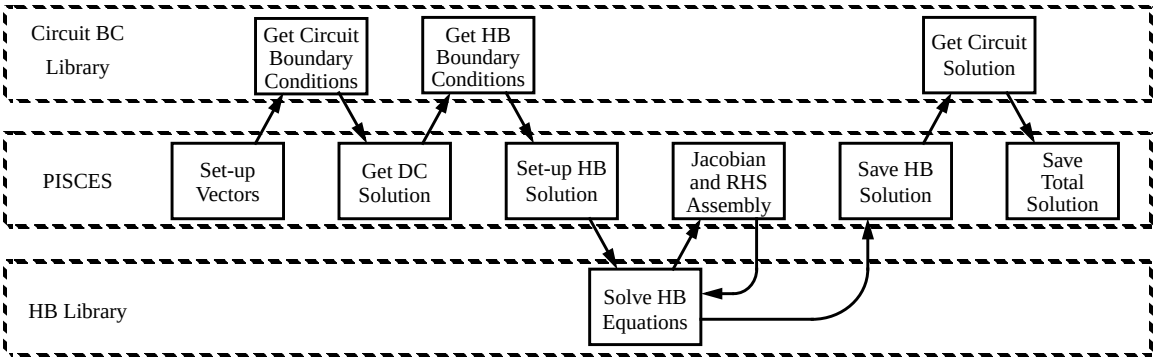


Fig 6. Integration of PISCES with an harmonic balance library and a circuit boundary condition library.

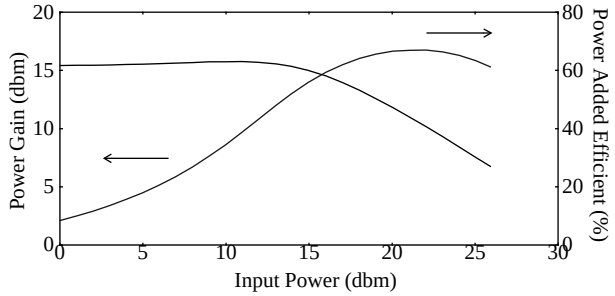


Fig 7. Experimental values for power gain and power added efficiency.

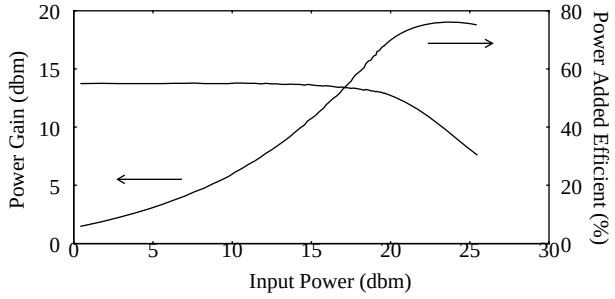


Fig 8. Simulated values for power gain and power added efficiency.

criteria are the power gain and the power added efficiency as shown in Fig. 7. The gain rolls off at higher power levels ($P_{in} > 15dbm$) because the device operates in gm compression region and the output power is limited by the saturation current. The efficiency is low for a small P_{in} because the device drains more power in Class A operation. Efficiency increases until just after the gain starts to decrease. At this point, P_{in} approaches P_{out} resulting in very little power added to the input signal.

The simulation results in Fig. 8 qualitatively follow the experimental results. Further tuning of the mobility models, the device ac/DC characteristics, and the matching network would improve the agreement.

V. CONCLUSIONS

Harmonic balance device simulation is a powerful tool for analyzing many types of RF problems. Coupling the device simulation with circuit parasitics and circuitry extends the capabilities of the simulator to include not only the physical device but also extrinsic components that have bearing on the performance of the structure. This paper demonstrates the power of the tool by analyzing an LDMOS RF power transistor for gain and efficiency given parasitics, bias circuitry, and matching networks.

ACKNOWLEDGMENT

The authors would like to acknowledge the Semiconductor Research Corporation for their support of this research effort. In addition, both Motorola and Hewlett Packard provided technical help and assistance by providing experimental data and in the development of the HB solver, respectively.

REFERENCES

[1] B. Troyanovsky, F. Rotella, Z. Yu, R. Dutton, and J. Sato-Iwanga. "Large Signal Analysis of RF/Microwave Devices with Parasitics Using Harmonic Balance Device Simulation." SASIMI. Fukuoka, Japan: Nov. 1996.

[2] Gordon Ma, Wayne Burger, Chris Dragon, and Todd Gillenwater. "High Efficiency LDMOS Power FET for Low Voltage Wireless Communications." Proceedings of IEDM. San Francisco, CA: December 1996.

[3] Alan Wood, Chris Dragon, and Wayne Burger. "High Performance Silicon LDMOS Technology for 2GHz RF Power Amplifier Applications." Proceeding of IEDM. San Francisco, CA: December 1996.

[4] A. Mujtaba, S.-I. Takagi, and R. Dutton. "Accurate modeling of Coulombic scattering, and its impact on scaled MOSFETs." Technical Digest of Symposium on VLSI Technology. Kyoto, Japan: June 1995.

6V on the g ate and 20V on the drain. The PISCES simulations, using a local mobility model de veloped at Stanford[4], match the e xperimental I_{ds} vs. V_{ds} curv es. Under high g ate and drain biases, a high current generates heat, thus reducing the mobility; however, the device is rarely operated in this region. Fig. 4 shows the good agreement for the I_d vs. V_g curv es in the linear re gion (V_d=0.1V) and saturation region (V_d=6.0V).

III. SIMULATOR ARCHITECTURE

Stanford and HP jointly de veloped a PISCES e xtension that solves the semiconductor equations in the frequenc y domain (Harmonic Balance Simulation) thus enabling large signal sinusoidal simulations. In addition, a mix ed circuit/ device simulation capability allows the inclusion of circuit aspects from parasitics to matching networks was developed to complement the harmonic balance solver.

The harmonic balance approach tak es the semiconductor equations and assumes periodic solutions given that the input signal is periodic or quasi-periodic. Since the de vice is non-linear, inte ger-multiple combination of harmonics to the input frequency(ies) are created. In simulation, the frequency list is truncated to some set of N frequencies such that the excluded values are insignificant.

The independent semiconductor variables, ψ, n, p, at each grid point are represented as sho wn in (1) where k refers to the solution at a specific grid point in the spatial discretization and represents the th frequency.

$$\psi_k(t) = \psi_{k0} + \sum_{i=1}^{N} (\psi_{ki}\cos(\omega_i t) + \psi_{k,\,i+N}\sin(\omega_i t)) \qquad (1)$$

The goal of the analysis is to find the quasi F ourier coefficients ψ_{ki}, , and such that the semiconductor partial differential equations are satisfied. Once those coefficients (i.e. harmonics) for the basic v ariables are computed, the conduction current and displacement current can be computed at the device terminals.

To include the circuit components in the device simulation they are reduced to a set of boundary condition equations. Fig. 5 sho ws a PISCES de vice surrounded by an arbitrary linear network. By assuming unknown voltages and currents at the electrodes of the de vice, the relationship among those voltages and currents are computed (2). F or large signal AC analysis, the boundary conditions become complex and are calculated at each frequency. The $V_{applied}$ vector contains the source vector at DC and the fundamental frequencies. It is zero for the generated harmonics since the surrounding circuity is linear and hence, generates no new harmonics.

$$-(\psi, n, p) = 0 \qquad (2)$$

Circuit boundary conditions and harmonic balance simulation are integrated with PISCES as sho wn in Fig. 6. PISCES calls the circuit boundary condition routines to generate the equations from a SPICE like net list. It then calls the harmonic balance solver passing the boundary conditions and PISCES state v ariables. The harmonic balance solv er uses the PISCES assembly routines to generate the Jacobian and RHS at each frequenc y for each iteration. Once the convergence criteria is met, the solution is passed back to PISCES which calls a circuit solv er to get the complete solution.

IV. SIMULATION RESULTS

This simulator is used to analyze the RF performance of the Motorola LDMOS amplifier at 850MHz. The k ey design

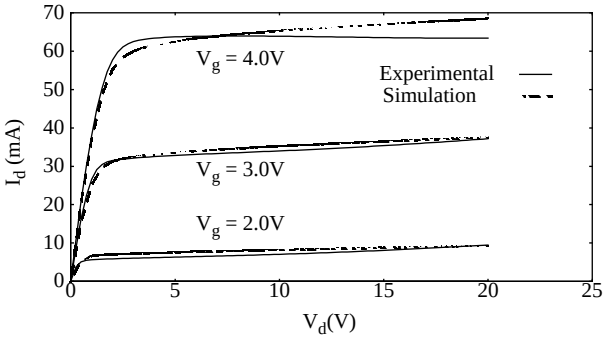
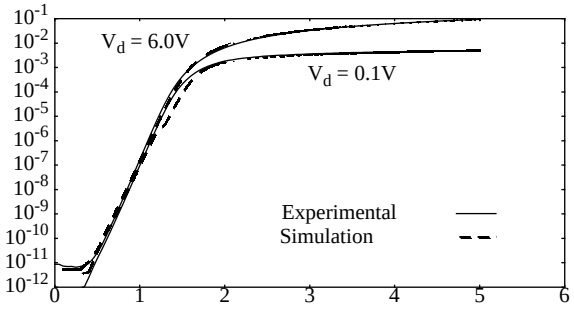


Fig 3. Simulated and experimental drain characteristics.



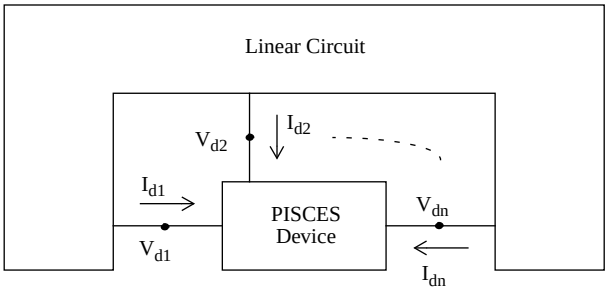


Fig 5. PISCES device surrounded by an arbitrary linear circuit

Harmonic Balance Device Analysis of an LDMOS RF Power Amplifier with Parasitics and Matching Network

Francis M. Rotella, Zhiping Yu, and Robert Dutton
Center for Integrated Systems
Stanford University
Stanford, CA 94305

Boris Troyanovsky
EEsof Division
Hewlett Packard
Santa Rosa, CA 95403
(formerly with Stanford Univ.)

Gordon Ma
Communication Products Laboratory
Semiconductor Products Center
Motorola Inc.
Tempe, AZ 85284

Abstract -- This paper discusses an harmonic balance simulation involving an high power LDMOS device, bias circuitry, and matching network. The paper begins with a discussion of the device and circuit configuration as well as the requirements for simulation. Next the paper describes the simulation algorithms and simulator structure in order to meet the requirements. PISCES is used as the basis and around it are added libraries for harmonic balance simulation and circuit boundary conditions. Finally simulation results are presented. The experimental and simulated response of the power gain and power added efficiency of an RF power amp is shown.

I. INTRODUCTION

In order to accelerate the design phase of new devices, simulation tools provide valuable insight into performance. For RF devices, Stanford and HP jointly developed an harmonic balance simulator for analyzing a device in the frequency domain[1]. However, the performance of RF devices is not restricted to intrinsic effects and can depend upon parasitics from interconnect and packaging as well as the matching networks and bias circuitry used to connect the device to the rest of the circuit. This paper addresses the RF simulation of the external circuit components in conjunction with the intrinsic device. The paper describes a simulation approach and presents an example of practical importance to industry.

II. DEVICE AND CIRCUIT STRUCTURE

The device under analysis is an LDMOS device provided by Motorola (refer to Fig. 1) [2][3]. A laterally diffused graded channel enhances RF performance, prevents punch-through, and increases the device transconductance. A p+ sinker connects source and substrate together to eliminate extra bond wires and provide for a back side contact. An n-LDD decreases the electric field at the drain side of the device and optimizes R_{ds}(on), BV_{dss}, and C_{dg}. A metal field plate reduces the electric fields at the edge of the gate thereby increasing the breakdown voltage and reducing C_{dg}.

Surrounding the device are a large number of circuit parasitics in addition to the biasing circuitry and matching networks. Each of these components is represented in block diagram form in Fig. 2. Nearest the intrinsic device are the parasitics from interconnect resistances and capacitances. In addition, the package bond wires add inductance.

Outside the package, the bias circuitry and matching networks establish a connection to the rest of the circuit. The biasing circuitry is isolated from the input/output by inductors which block high frequencies while the matching networks are isolated with capacitors which block DC. Fig. 3 and Fig. 4 show the experimental and simulated IV characteristics for the device.The device operates with up to

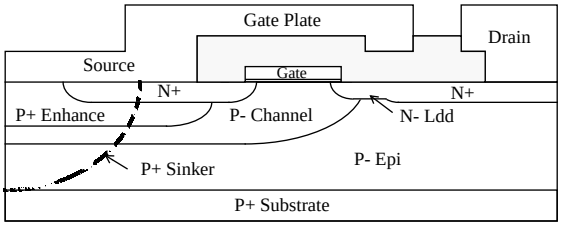


Fig 1. LDMOS device cross section.

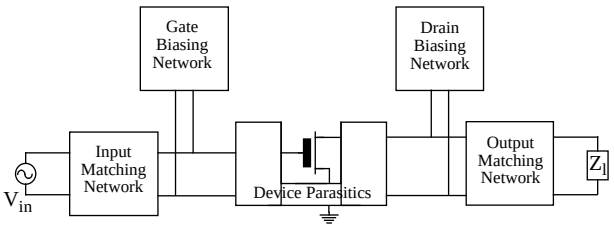


Fig 2. Block diagram of amplifier circuit including biasing circuitry and matching network.