Mixed Circuit and Device Simulation for Modeling, Analyzing, and Designing RF Devices

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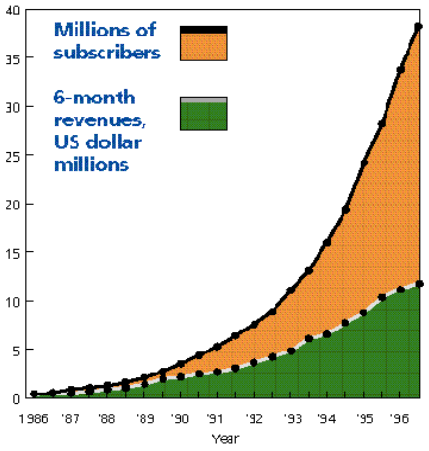
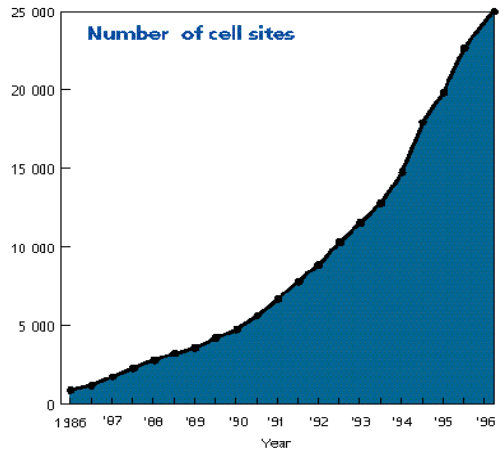
Motivation: Wireless Growth

- Wireless communications and networking in the US have been growing exponentially over the last decade.
- European countries are following the US trend. For example, Scandinavia has almost one mobile phone for every two people.
- However, world wide penetration has reached only 5% with Asia and Africa offering the greatest opportunity for expansion.





Source: Cellular Telecommunication Industry Association.
Published in January 1997 issue of IEEE SPECTRUM Magazine (Vol 34; No. 1).

Motivation: TCAD Tools are Critical

- In order to meet the demands of these expanding markets, next generation semiconductor technology (chip level and discrete RF power devices) need to be developed quickly, produced in high volume, and sold at low cost.

- Over the last decades, to meet the challenges of new technology development TCAD tools such as PISCES (aka Medici from Avant! and Atlas from Silvaco) played a critical role in understanding device design and performance trade-off.

- Recent work and this talk examines the role of PISCES in RF device design in order to meet the challenges of the growing markets in wireless communications.

  a. Development of the harmonic balance solver for the device equations. (Boris Troyanovsky)

  b. Inclusion of circuit components in the device simulation and harmonic balance simulation.

  c. Accurate modeling techniques to develop an RF representation of a device.

Outline of Talk

- **Tools:** Coupling Circuit and Device Simulation
  a. Full-Newton Algorithm
  b. Two-Level Newton Algorithm
  c. Reduction to Boundary Condition Equations
- **Tools:** Harmonic Balance Simulation
  a. Harmonic Balance Simulation
  b. Boundary Conditions for HB Simulation
- **Example:** Modeling RF LDMOS Discrete Transistors
  a. Device Structure and Operation
  b. Model for the Device
  c. Model Verification
- **Example:** Analysis and Design of LDMOS Discrete Transistors
  a. Gain, Efficiency, and Inter-modulation Distortion
  b. Variation in Parasitic Components
  c. Matching Network Effects

Device Simulation

- Provides a way for device engineers to analyze, design, and optimize semiconductor devices before manufacturing them.

- Numerically solves the semiconductor equations:

  Poisson: $\nabla\bullet(-\varepsilon\nabla\psi) = q\left(p - n + N_D^+ - N_A^-\right)$

  Continuity: $\frac{\partial n}{\partial t} = \frac{1}{q}\nabla \bullet J_n - U$, $\frac{\partial p}{\partial t} = \frac{-1}{q}\nabla \bullet J_p - U$,

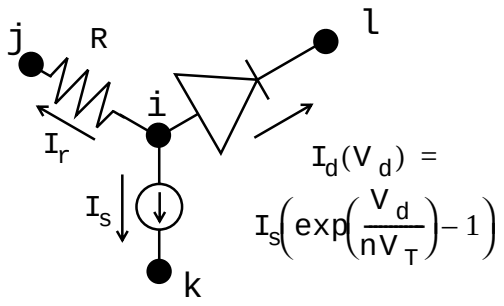
  where $J_n = qD_n\nabla n - q\mu_n n\nabla\psi$ and $J_p = -qD_p\nabla p - q\mu_p p\nabla\psi$.

- The equations are discretized in 1D, 2D, or 3D space on a non-uniform grid. Finite element and finite difference methods are used to obtain a set of non-linear equations and an iterative solution method is applied until a self-consistent solution is found.

- Models are used to represent physical characteristics of the material (mobility, recombination rates, and dielectric constants) at each point.

Circuit Simulation

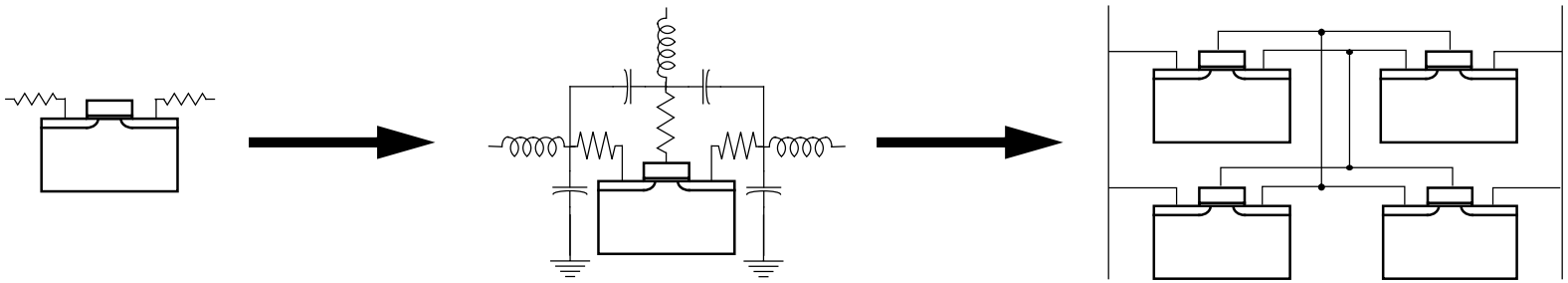
- Based upon KCL at each node and KVL for circuit branches.
- For circuits with no voltage sources, Newton's method is used to obtain a set of equations $[G^n][V^{n+1}] + [I^n] = [0]$ for the (n+1)-th iteration.
  a. $[V^{n+1}]$ is a vector of unknown voltages for the (n+1)th iteration.
  b. $[G^n]$ is the conductance matrix based upon the solution from the n-th iteration.
  c. $[I^n]$ is a vector of nodal currents based upon the n-th iteration.



$$\frac{V_i^{n+1} - V_j^{n+1}}{R} + I_s + I_d(V_i^n - V_l^n) + (V_i^{n+1} - V_l^{n+1})\left.\frac{dI_d}{dV_d}\right|_{V_d = V_i^n - V_l^n} - (V_i^n - V_l^n)\left.\frac{dI_d}{dV_d}\right|_{V_d = V_i^n - V_l^n} = 0$$

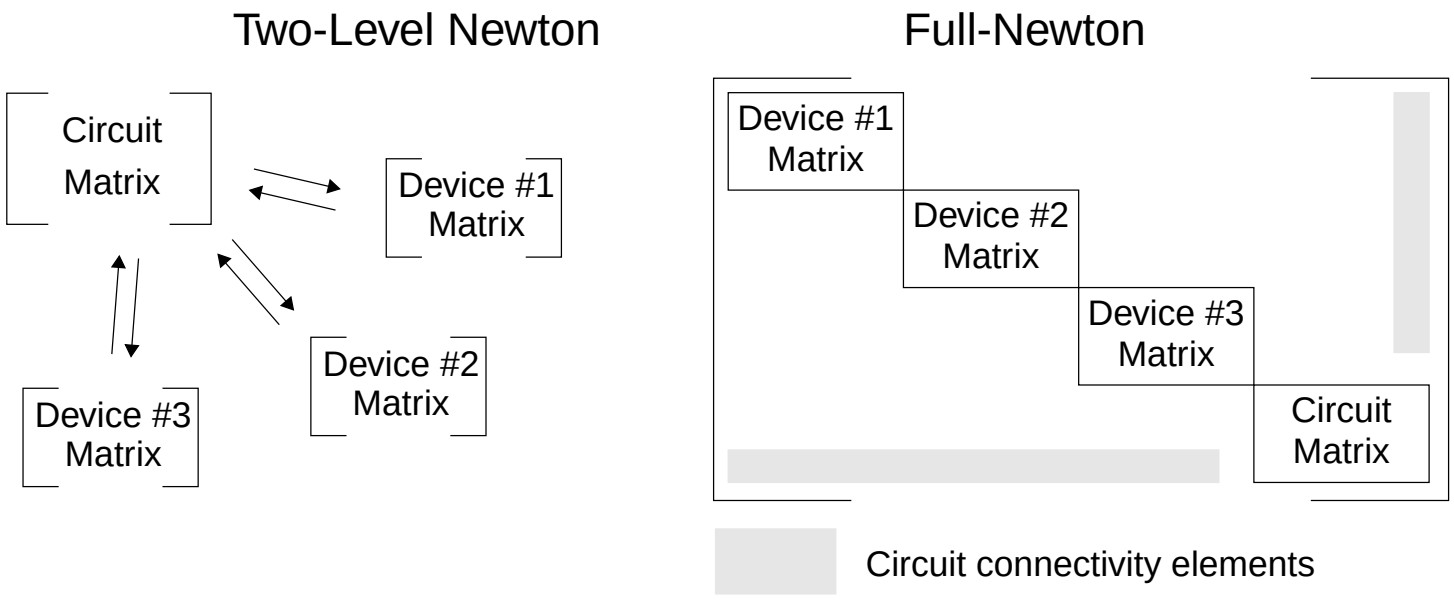
Types of Mixed Circuit/Device Simulation

- ***Intrinsic Device:*** The intrinsic device is surrounded by circuit elements that are limited to contact resistance or interconnect resistance (capacitance).
- ***Discrete Devices:*** Discrete devices contain parasitic components generated by the interconnect, pad, and packaging resistances, inductances, and capacitances.
- ***Sub-Circuit/Unit Cell:*** A unit cell contains multiple devices and/or circuit elements that interact with each other.



Approaches: Two-Level Newton versus Full-Newton

- The two-level Newton algorithm solves the circuit at one level of iterations and the device at a second level. (Multiple device iterations for one circuit iteration)
- The full-Newton algorithm solves the numerical device and the circuit nodes simultaneously in the same matrix. (Same number of iterations for device and circuit)



Comparison of the Two Algorithms

Advantages of the two-level Newton over the full-Newton algorithm:

- Better convergence for DC analysis if node voltages are unknown. The full level Newton requires all circuit node voltages to be specified within a certain percentage; otherwise it fails to converge.

- More modularity in two-level Newton allows many device simulators to be used simultaneously. For example, PISCES may be used for two dimensional devices and Fielday may be used for the three dimensional devices.

- Easier to implement a parallel version of two-level Newton algorithm. Each numerical device simulation can be relegated to a node of a parallel machine whereas the matrix for the full level Newton algorithm has to be partitioned to each node.

- By utilizing SPICE as the circuit simulator, any improvements/ modifications in SPICE automatically benefit the mixed-mode simulations.

Comparison of the Two Algorithms (continued)

Disadvantages of the two-level Newton over the full-Newton algorithm:

- Given a good estimate of all the node voltages, the full-Newton algorithm converges much more quickly than the two-level Newton.

- Likewise, since transient analysis involves small voltage changes from time step to time step making the problem well behaved, the full-Newton method converges much more quickly for this case as well. Mayaram determined a factor of 1.7 times as fast.[1]

Limitations in scope of comparison:

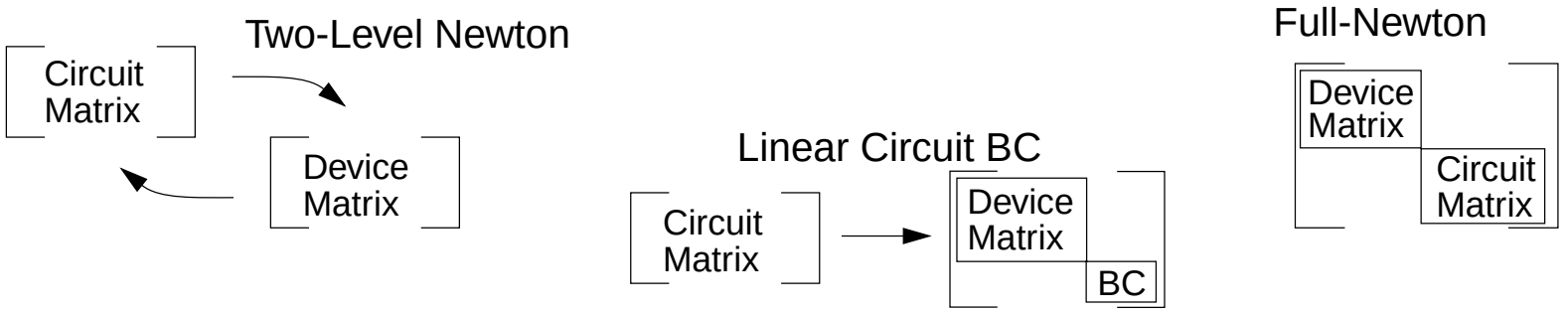
- Mayaram limited his devices to a couple hundred nodes, but as the size of the problem increases, the dynamics change.

  Work not presented in this talk explored the capabilities using devices of many nodes and using parallization.

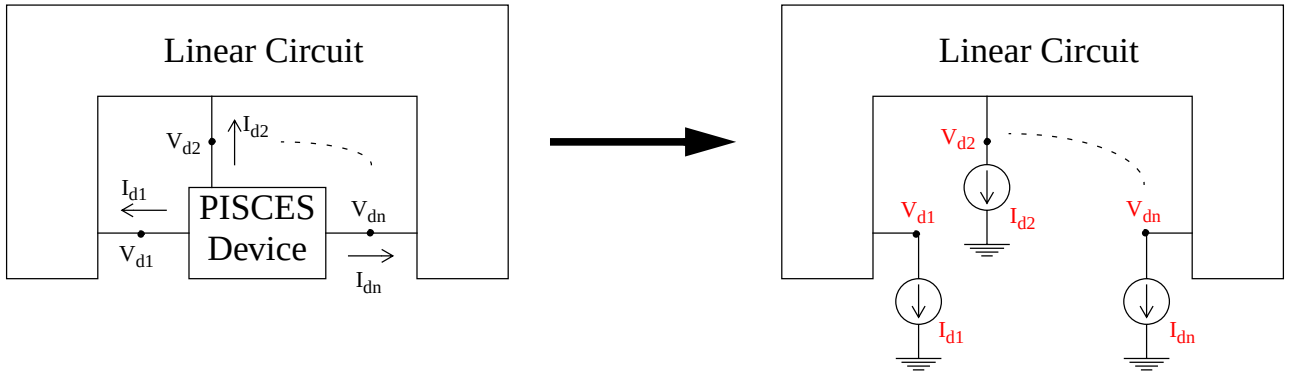
1. Mayaram, Kartikeya and Donald O. Pederson. “Coupling Algorithms for Mixed-Level Circuit and Device Simulation.” *IEEE Transactions on Computer Aided Design*. Vol. II, No 8. August 1992. pp 1003-1012.

Linear Mixed-Mode using BC Equations

- Allows simplified circuit to be simulated with a PISCES device directly. (Discrete component with interconnect, pad, and packaging parasitic elements)
- The algorithm is a cross between the two-level Newton and full-Newton algorithms.
- Does not suffer from disadvantages of two-level Newton algorithm since only one circuit iteration is required.
- Does not increase the size of the device simulators matrix in cases where there are many circuit nodes (i.e. distributed transmission line or substrate resistance mesh)



Linear Mode Mixed Circuit/Device Simulation



- Given a linear circuit with no voltage sources:

$$\begin{bmatrix} F_c \\ F_d \end{bmatrix} = \begin{bmatrix} G_{cc} & G_{cd} \\ G_{dc} & G_{dd} \end{bmatrix} \begin{bmatrix} V_c \\ V_d \end{bmatrix} + \begin{bmatrix} I_c \\ I_d \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$ where V_d, I_d, and V_c are unknown.

- Solving this system yields:

$$\begin{bmatrix} V_c \\ V_d \end{bmatrix} + \begin{bmatrix} G_{cc} & G_{cd} \\ G_{dc} & G_{dd} \end{bmatrix}^{-1} \begin{bmatrix} I_c \\ I_d \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \rightarrow \begin{bmatrix} V_c \\ V_d \end{bmatrix} + \begin{bmatrix} U^{-1} & -G_{cc}^{-1} G_{cd} V^{-1} \\ -G_{dd}^{-1} G_{dc} U^{-1} & V^{-1} \end{bmatrix} \begin{bmatrix} I_c \\ I_d \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

$$U = G_{cc} - G_{cd} G_{dd}^{-1} G_{dc}$$
$$V = G_{dd} - G_{dc} G_{cc}^{-1} G_{cd}$$

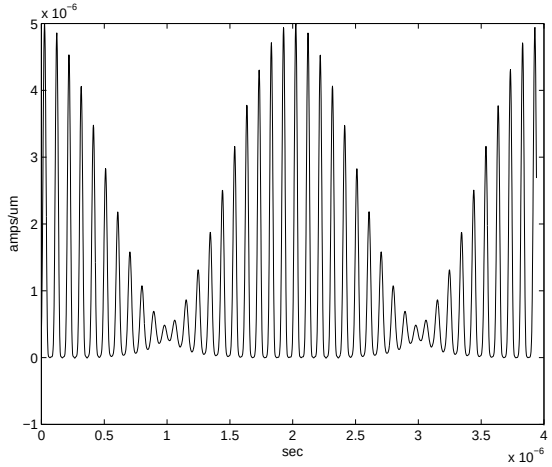
- Extracting the equations at the device nodes yields:

$$V_d - G_{dd}^{-1} G_{dc} U^{-1} I_c + V^{-1} I_d = 0 \quad \Leftrightarrow \quad G_d(E_d - V_d) - I_d(\Psi, n, p) = 0$$

$$E_d = G_{dd}^{-1} G_{dc} U^{-1} I_c \,, \quad G_d = V$$

RF Capabilities: Harmonic Balance Simulation

- Harmonic balance is used to do large steady state sinusoidal simulation and analysis where large single transient analysis may require long simulation time.
- Captures steady state in the presence of potentially long time constants introduced by bias networks, filters, etc.
- Avoids excessive number of small time steps needed in multi-tone analysis.



Diode response to two tightly spaced large signal input tones -- an illustration of the difficulties faced by time-domain methods.

The time step must be small enough to resolve the high frequency yet time must progress forward enough so that the low frequency transients die out.

Harmonic Balance Solution[1]

- Instead of solving for the time samples of each variable, the harmonic balance method expands each variable as a Fourier series and solves for the coefficients:

$$x_n(t) = X_{n0} + \sum_{h=1}^{H} \left(X_{nh}^{R} \cos(\omega_h t) - X_{nh}^{I} \sin(\omega_h t) \right)$$

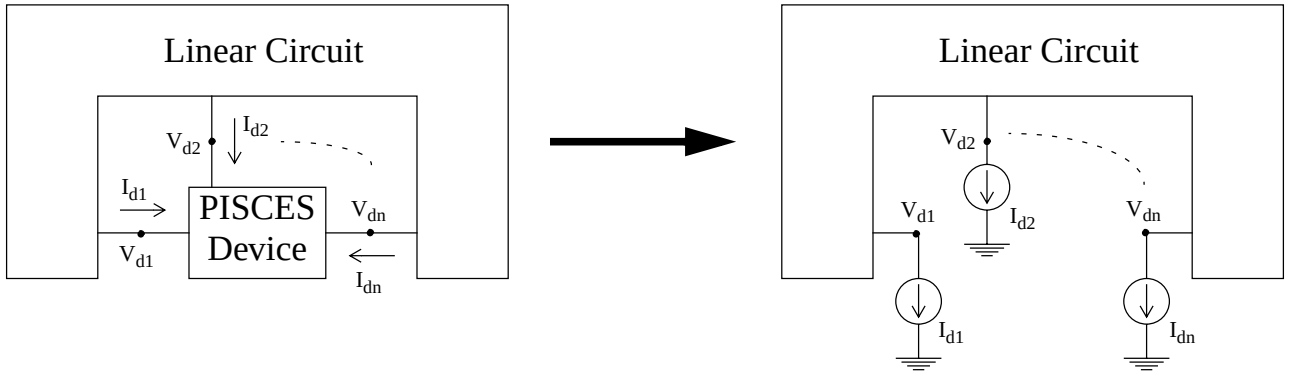
- The number of harmonics is limited to H. Harmonics of higher order are assumed to be insignificant.

- Harmonic balance solves for the real and imaginary coefficients which can then be assembled into a time domain representation of the signal in addition to the computed spectral view of the signal.

- Using basic circuit theory techniques, power can be calculated in the total signal or the individual harmonics.

1. For an in depth discussion of the solution algorithms please refer to the dissertation titled: *Frequency Domain Algorithms for Simulating Large Signal Distortion in Semiconductor Devices* by Boris Troyanovsky.

Boundary Conditions for HB Simulation



- For a generalized linear circuit, we can extract the equations relating the currents I_d and voltages V_d at each electrode.

$$G_d(E_d - V_d) - I_d(\Psi, n, p) = 0$$

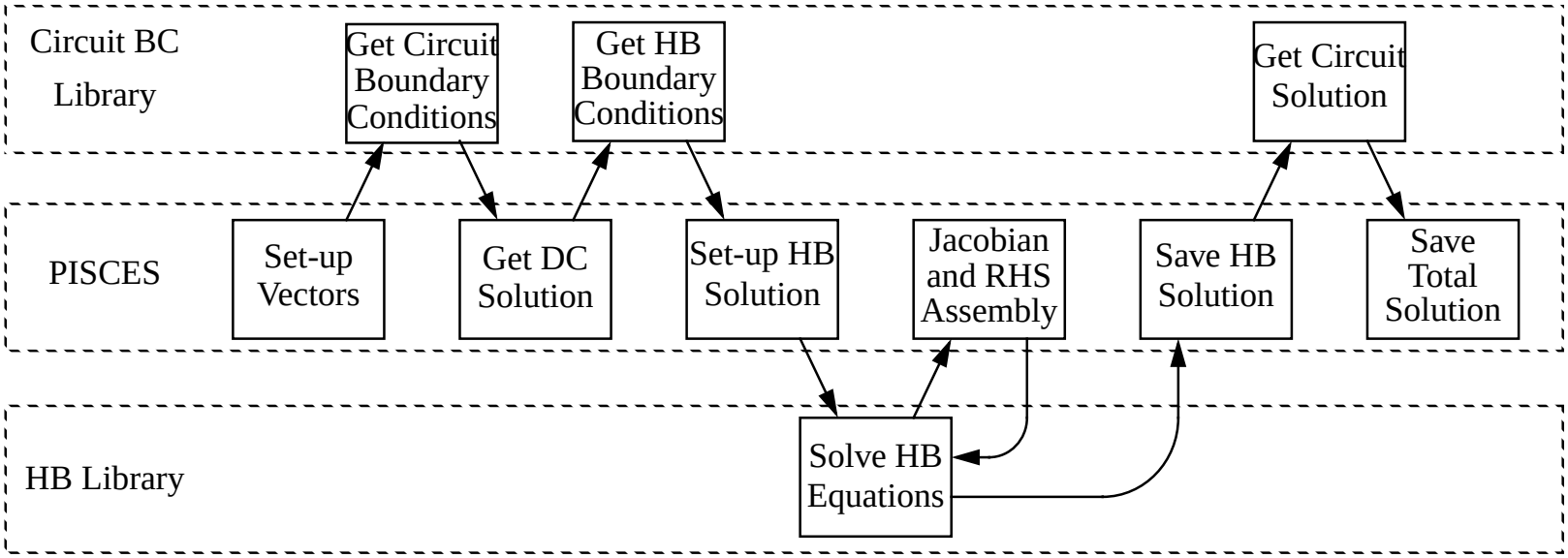
- For harmonic balance simulation, a set of complex equations is obtained for each frequency. Because the circuit is linear, no components are generated except at the fundamental frequency.

DC: $G_{d0}(E_{d0} - V_{d0}) - I_{d0}(\Psi_0, n_0, p_0) = 0$

Fundamental: $G_{d1}(E_{d1} - V_{d1}) - I_{d1}(\Psi_1, n_1, p_1) = 0$

Overtones: $-G_{dh}V_{dh} - I_{dh}(\Psi_h, n_h, p_h) = 0$

Interaction of PISCES with Harmonic Balance and Circuit Boundary Conditions

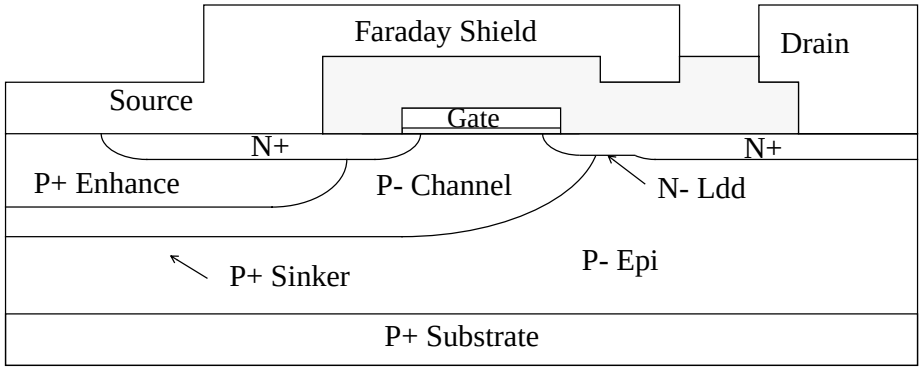


- Two separate sets of libraries exist for executing a simulation with harmonic balance and circuit boundary conditions.
- PISCES is responsible for calling the appropriate library routine in order to obtain the appropriate data.

RF Example: An LDMOS Transistor[1]

Device Structure
- 4 cells
- 56 fingers/cell
- 86µm fingers

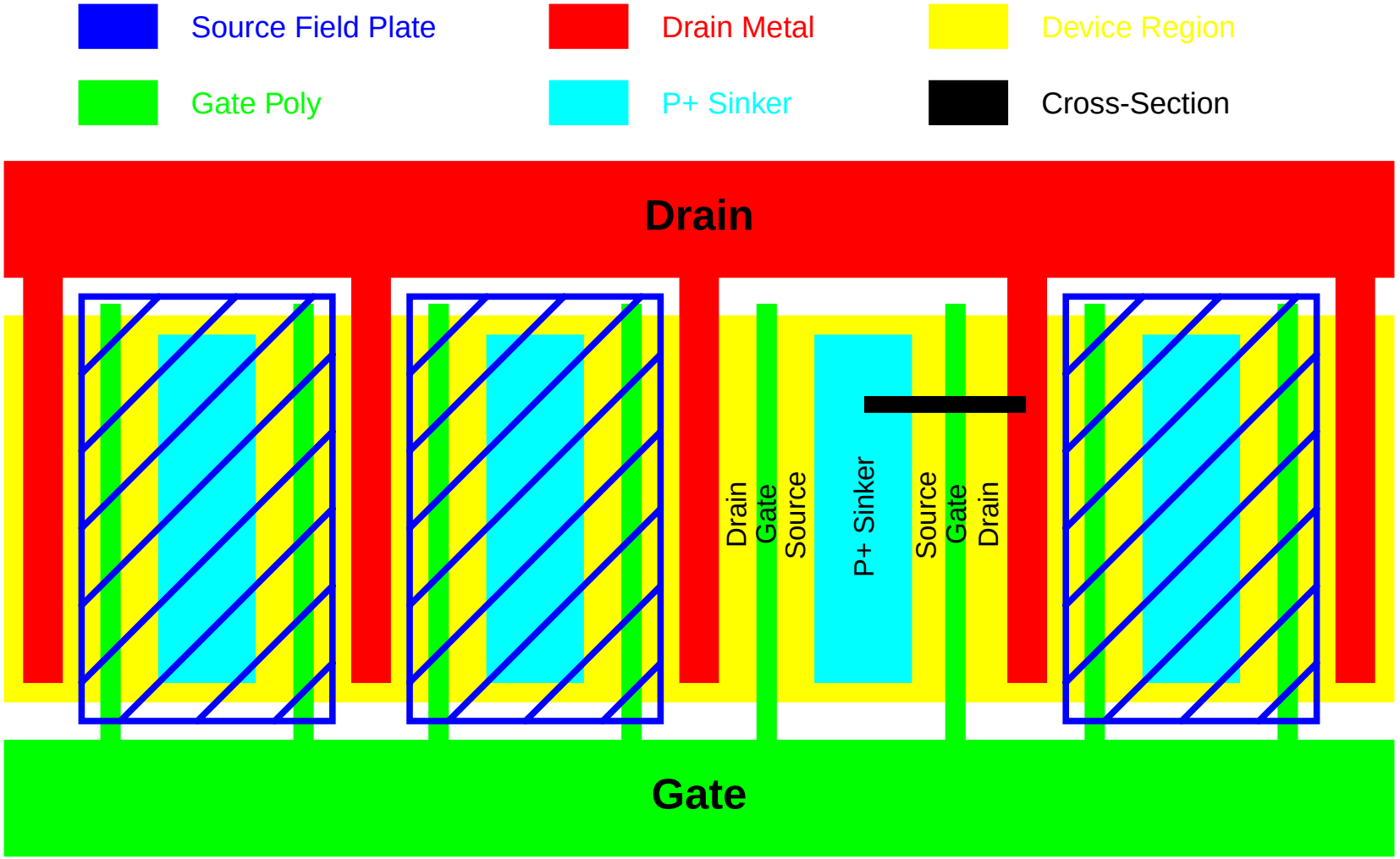
Total Gate Length:
- 19200µm



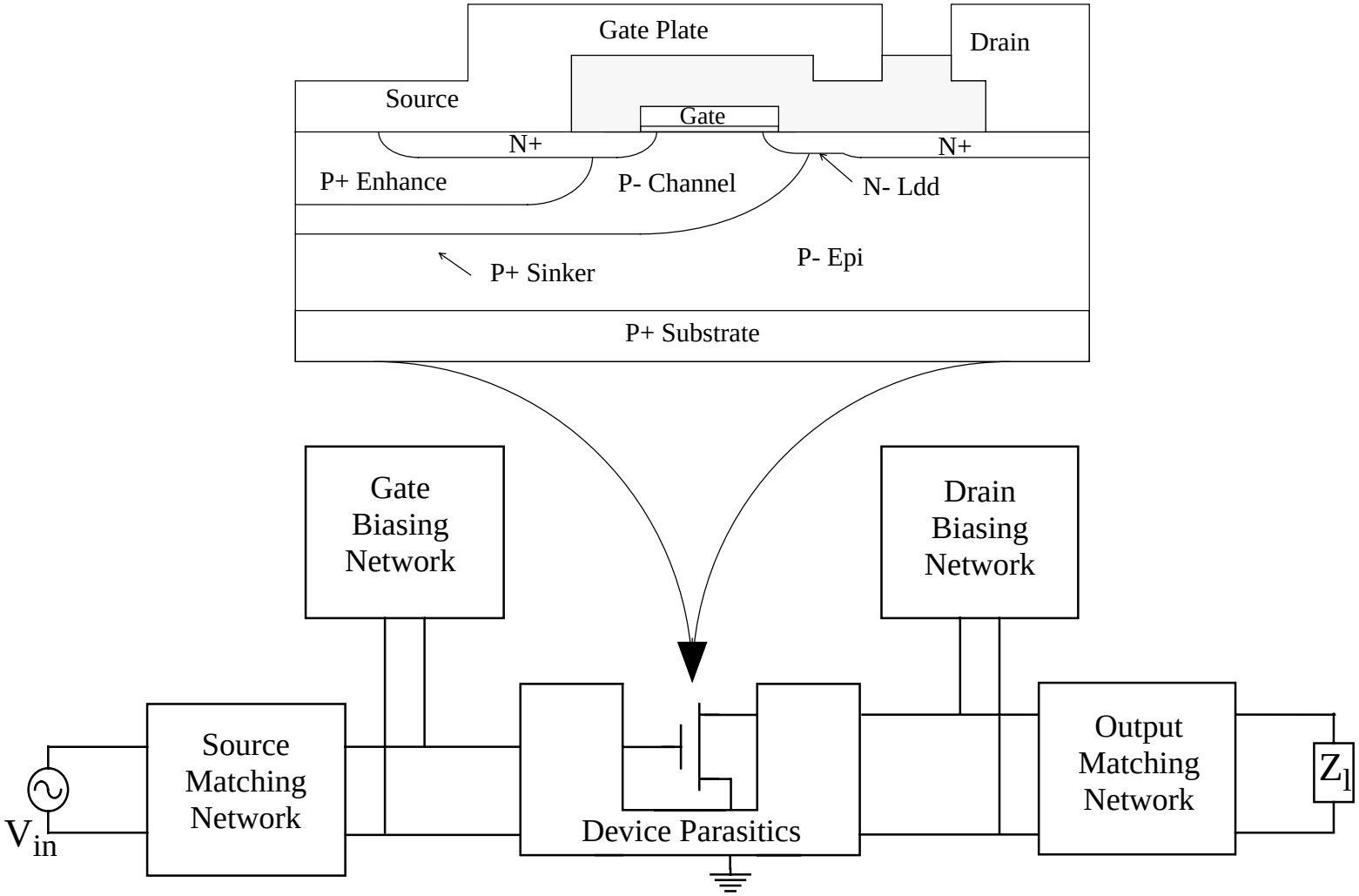
- ***Graded Channel:*** Increases transconductance of device and prevents punch through.
- ***P+ Sinker:*** Provides a source connection to backside contact thus eliminating surface bond wires to the source.
- ***Faraday Shield:*** Provides electric field confinement thus reducing the capacitance between gate (input) and drain (output).
- ***N- Ldd:*** Reduces maximum electric field at the drain thus increasing breakdown voltage.

1. Example is provided by Motorola Inc. in Tempe, AZ.

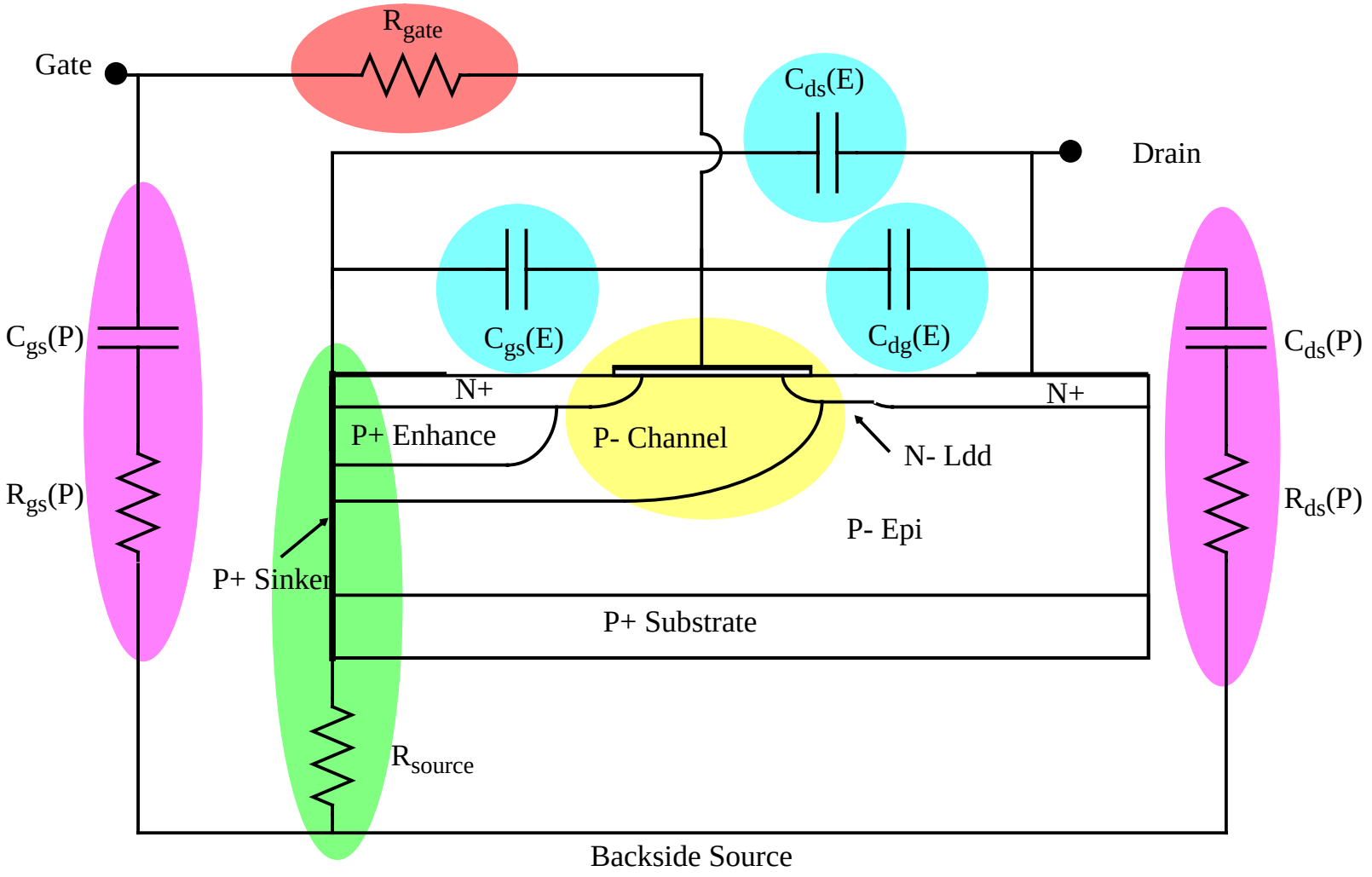
Top View of Structure



LDMOS Power Amplifier (Motorola)

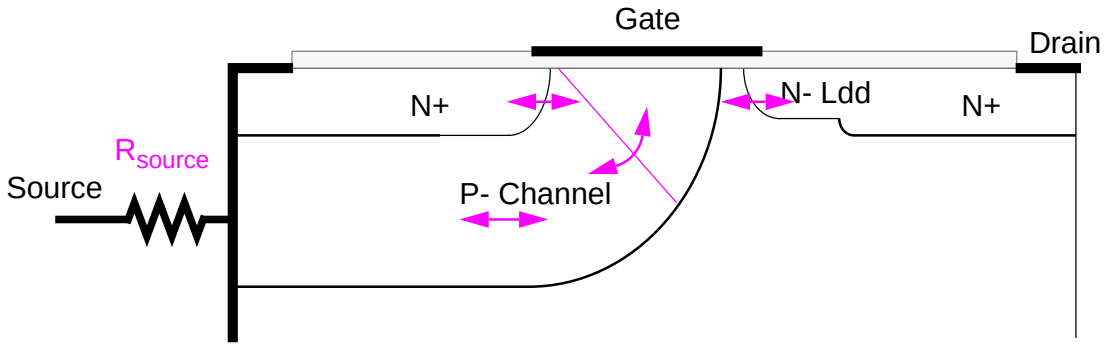


Key Modeling Regions for On Chip LDMOS Device



Device Characteristics: Channel Modeling

- 1D simulation of the process yields calibrated 1D doping profiles, but does not provide information for two dimensions.
- MOSFETs are inherently 2D device and thus it is necessary to understand those effects.
- To model the channel region and understand device design trade-offs a Design of Experiments (DOE) is used to determine an optimum set of parameters for the given variables.



Variables
Source Resistance
Source Location
Drain Location
P- Channel Location
P- Channel Lateral Diffusion

Sensitivity Analysis of Graded Channel Region

- Drain location had no effect on DC characteristics, but later analysis showed there was a significant effect on AC characteristics.

- The measured G_m at high current is affected strongly by source resistance and source location.

  Reason: The internal V_{gs} is reduced by the voltage drop across resistances on the source side of the device.

- The measured V_t is affected strongly by channel location and source location.

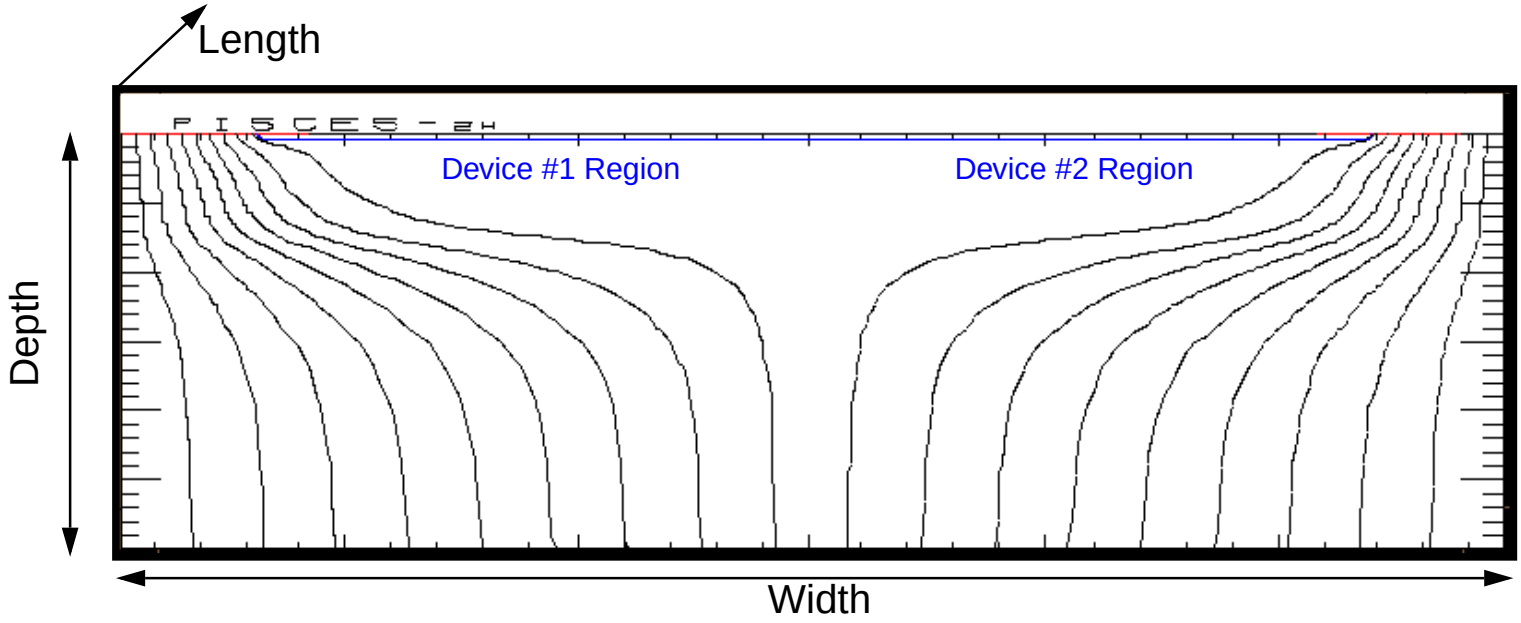
  Reason: Threshold is determined by the inversion of the channel nearest the source side of the device.

- The measured sub-threshold slope is affected strongly by source location and channel location.

  Reason: The slope is determined by the channel length and punch through characteristics.

Parasitic Components: Determination of R_{source}

- The independently measured value of the source resistance is 8Ω per sinker, but the fitted value to match IV characteristics is 45Ω.
- The measured resistance ignores current crowding under a finger of a device as shown in the PISCES simulation result.
- Current crowding prevents spreading beyond the width of a finger.

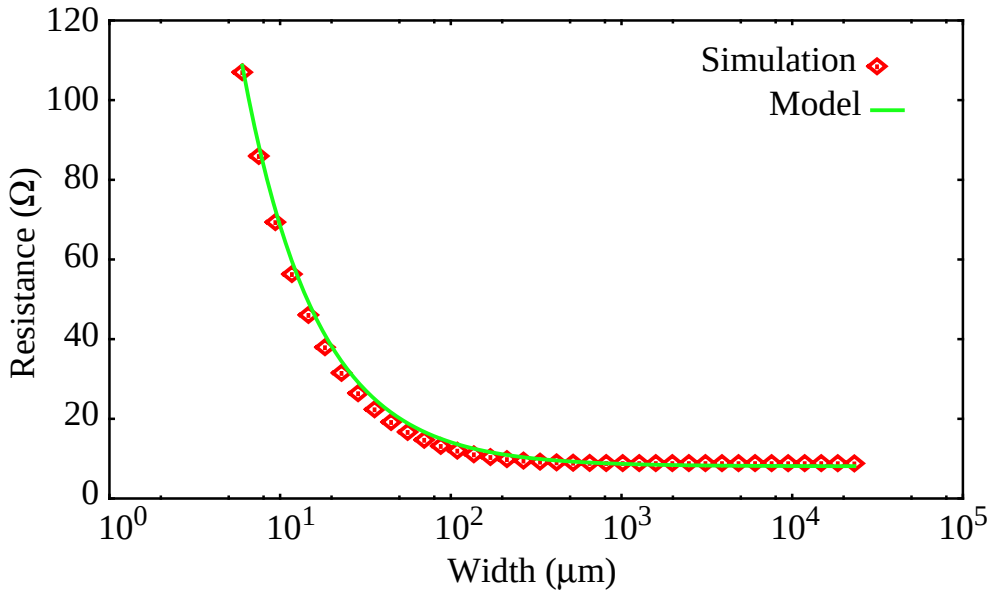


Parasitic Components: Modeling of R_{source}

- Based upon the sinker structure we are able to develop the following model to determine the impact of current crowding:

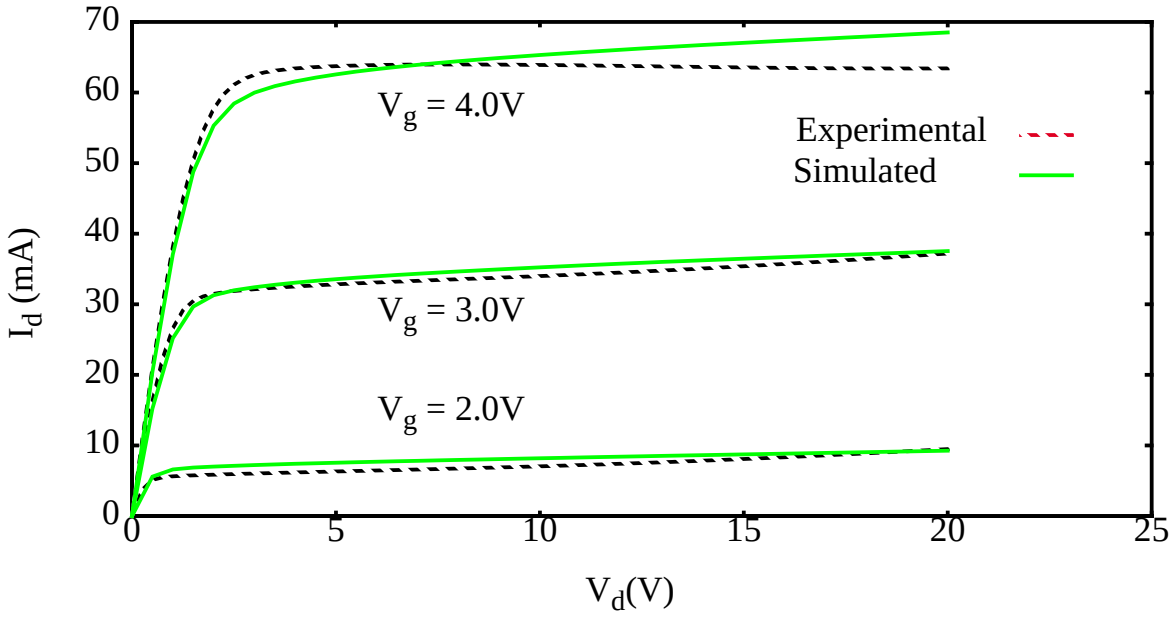
$$R(W) = L_{sinker}\left(\frac{D_{sinker}}{W_{sinker}} + \frac{D_{substrate}}{W_{max}} + \frac{D_{substrate}}{W}\right)\frac{1}{qn\mu_o}$$

- Making the fit from simulated data we get the following graph.



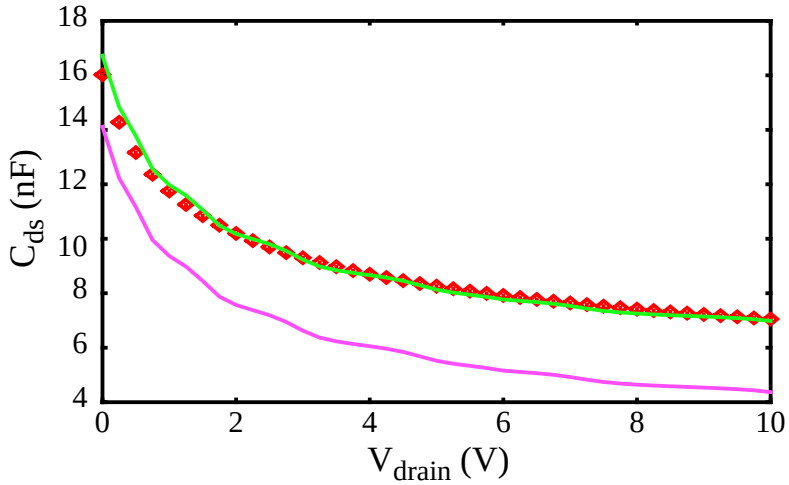
$R(\infty)$	=	8.9
W_{max}	=	232 μm
μ_o	=	134 cm^2 / V-s
Where:		
n	=	$2x10^{18}$ cm^{-3}
$D_{substrate}$	=	220 μm
D_{sinker}/W_{sinker}	=	2.0
L_{sinker}	=	86 μm

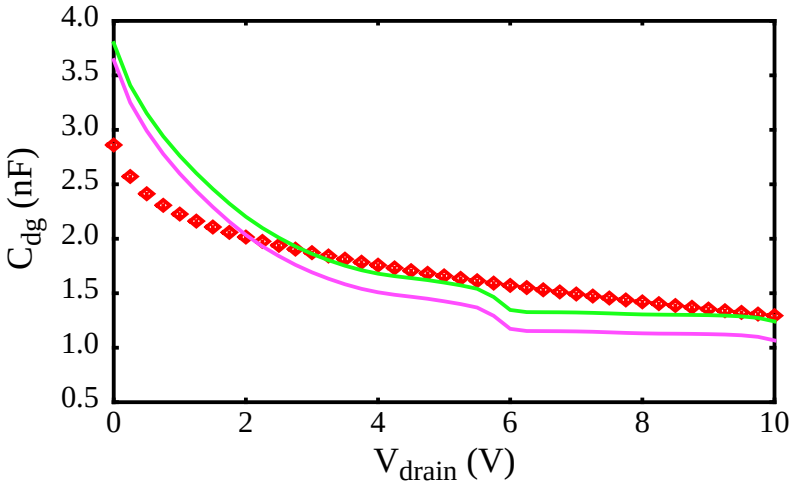
IV Characteristics and Thermal Effects

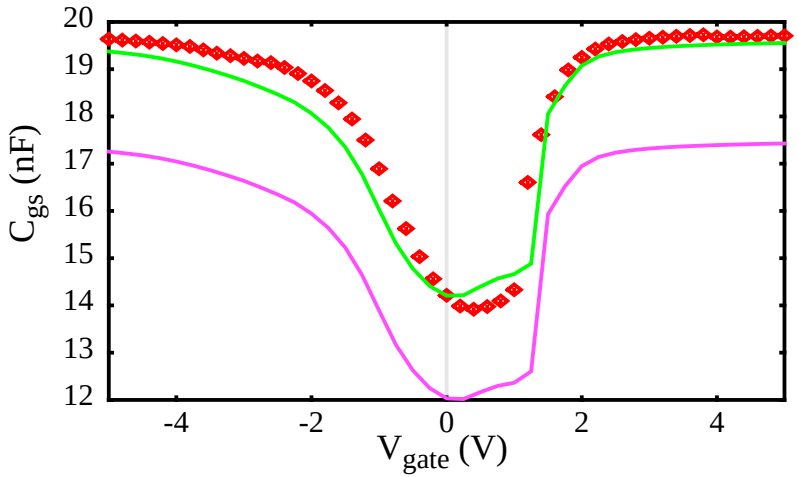


- At high biases, the device exhibits self-heating effects that lead to mobility degradation and ultimately poorer device performance.
- Fortunately, the device rarely enters the region of high currents; thus simulations ignoring self heating should provide an adequate representation of the device.

CV Simulated vs. Measured Data

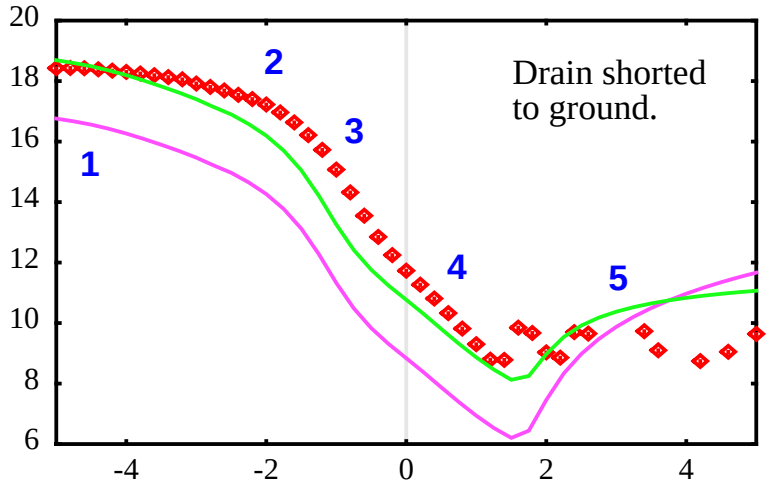


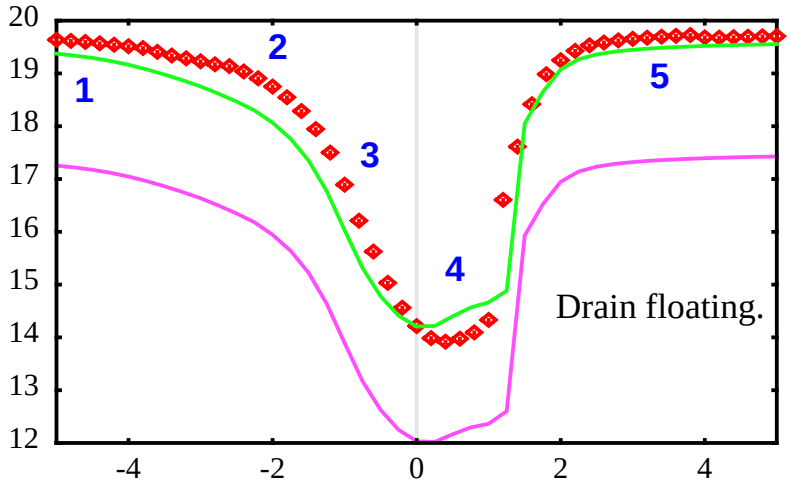


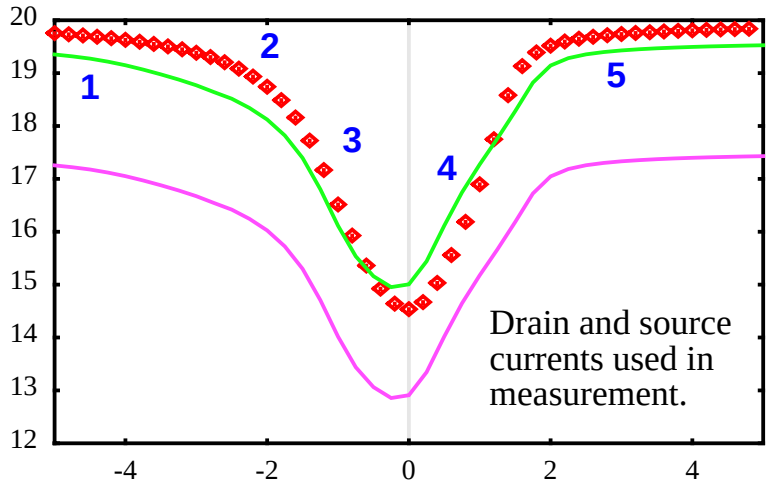


Simulated w/o Parasitics
Simulated with Parasitics
Experimental

CV Plots (C_{gs} vs. V_{gate})





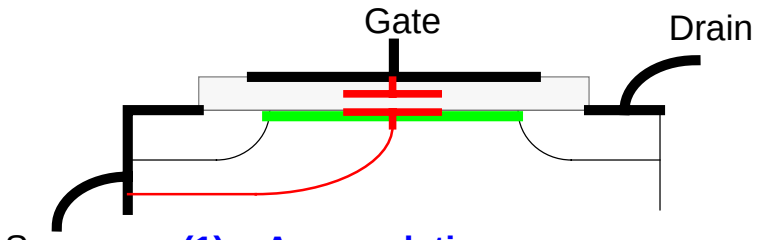


Simulated w/o Parasitics

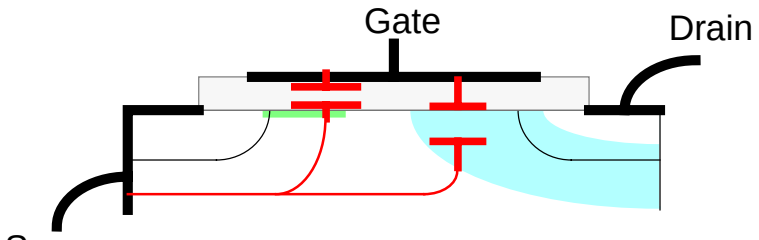
Simulated with Parasitics

Experimental

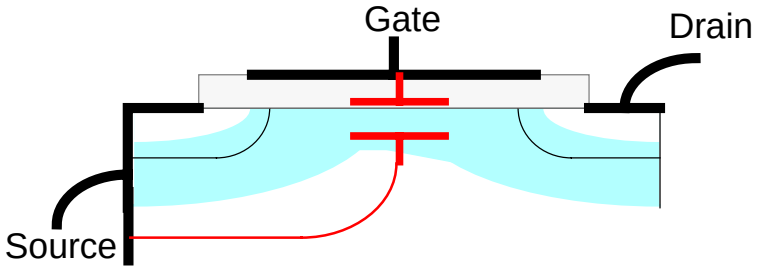
Silicon-Oxide Interface in Graded Channel Device



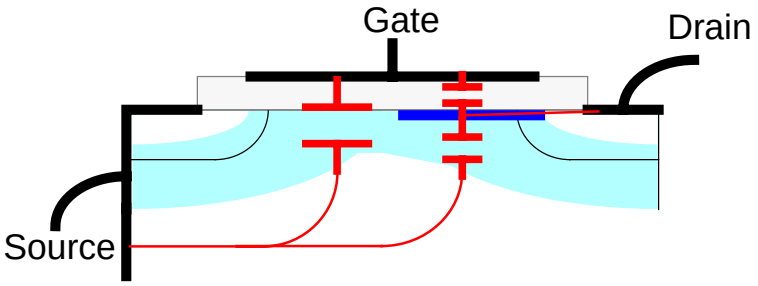
(1) Accumulation



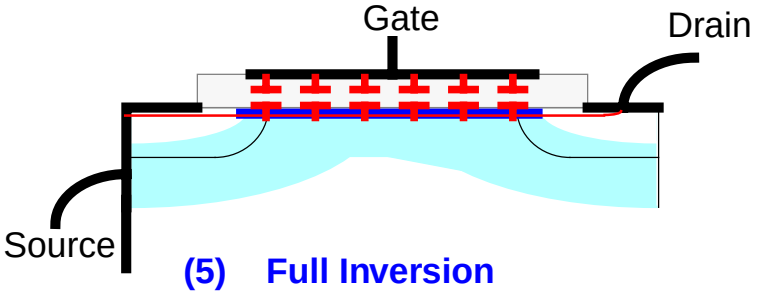
(2) Partial Depletion



(3) Depletion



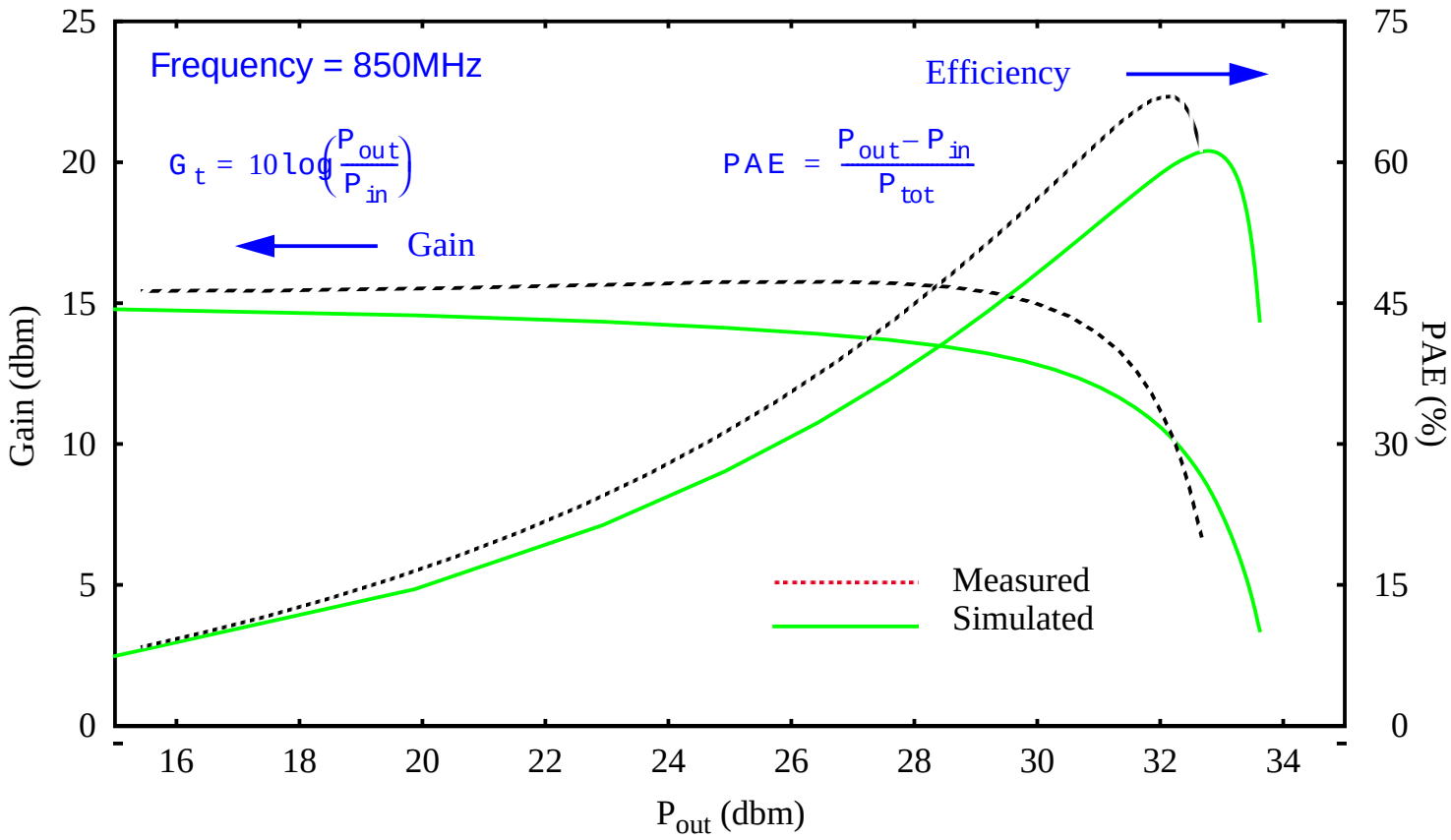
(4) Partial Inversion



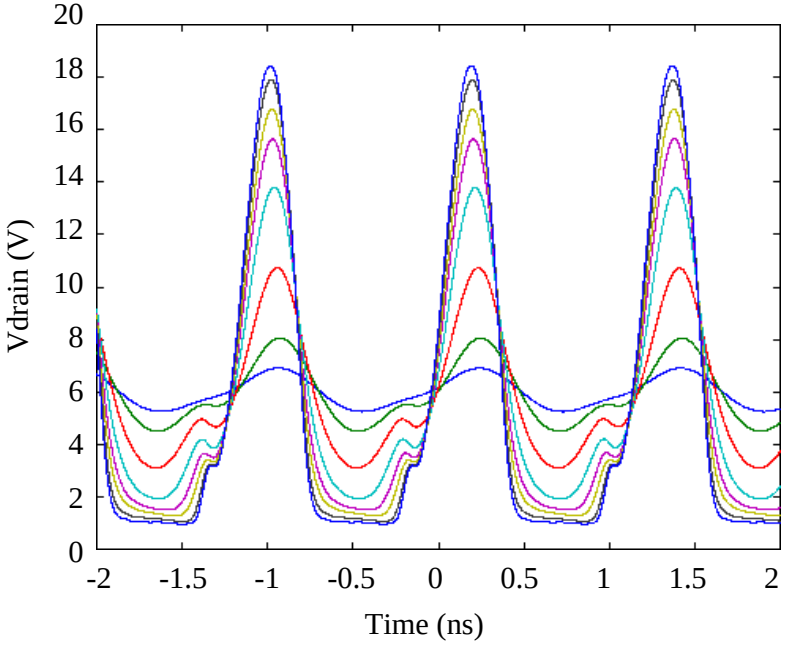
(5) Full Inversion

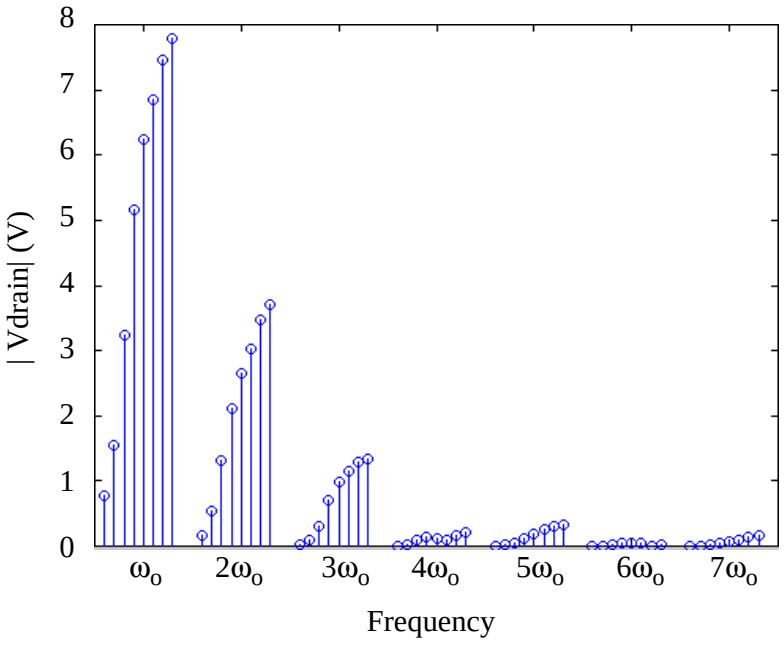
Depletion and inversion track across the channel as the doping increases from a low value (drain side) to a high value (source side).

RF Verification: Gain and Power Added Efficiency



Time Domain / Spectral Analysis (V_{drain})



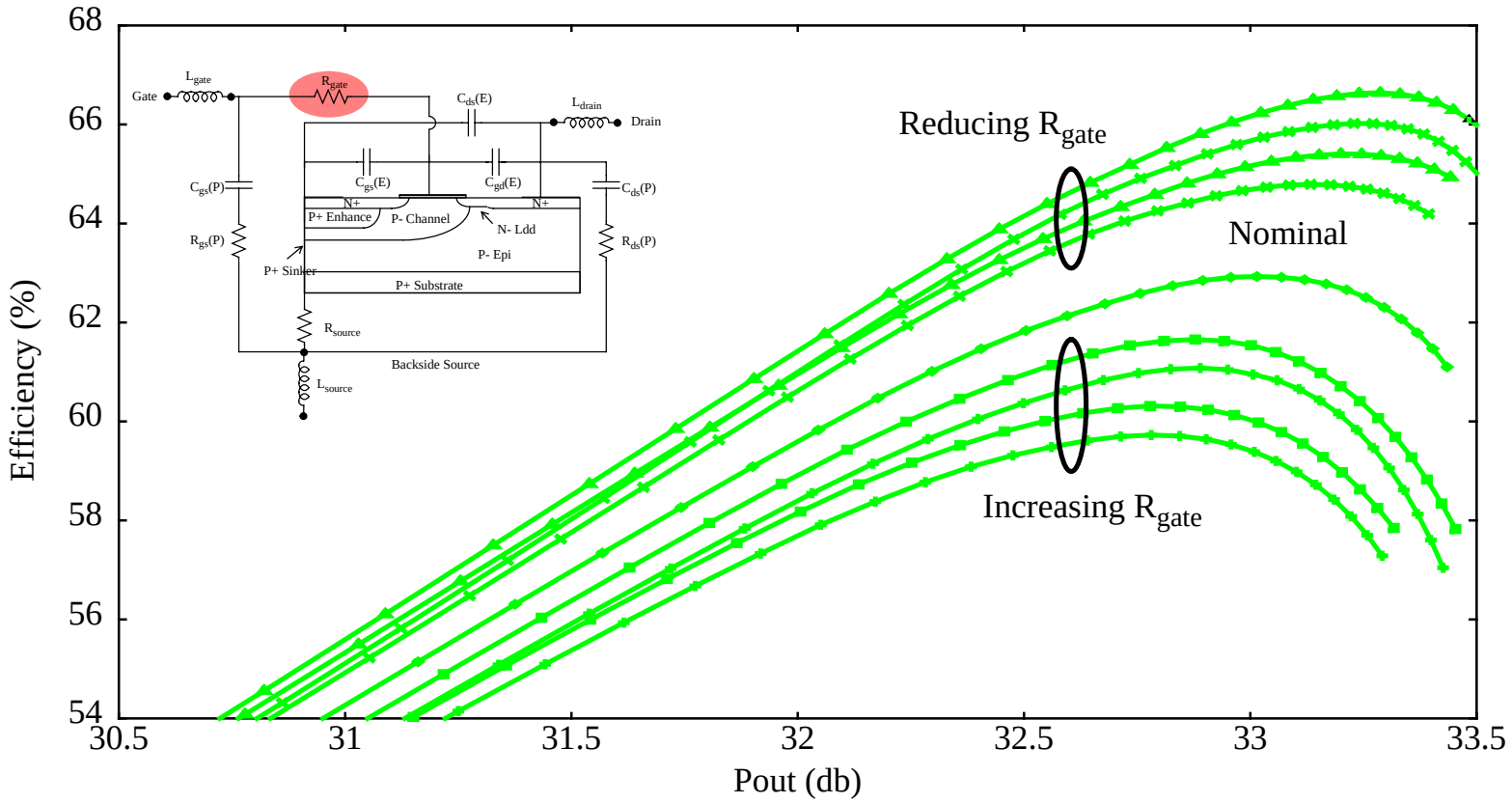


Power is increasing from 13.5dbm out to 33.5 dbm out.

- The device enters G_m compression and the output does not swing below threshold.

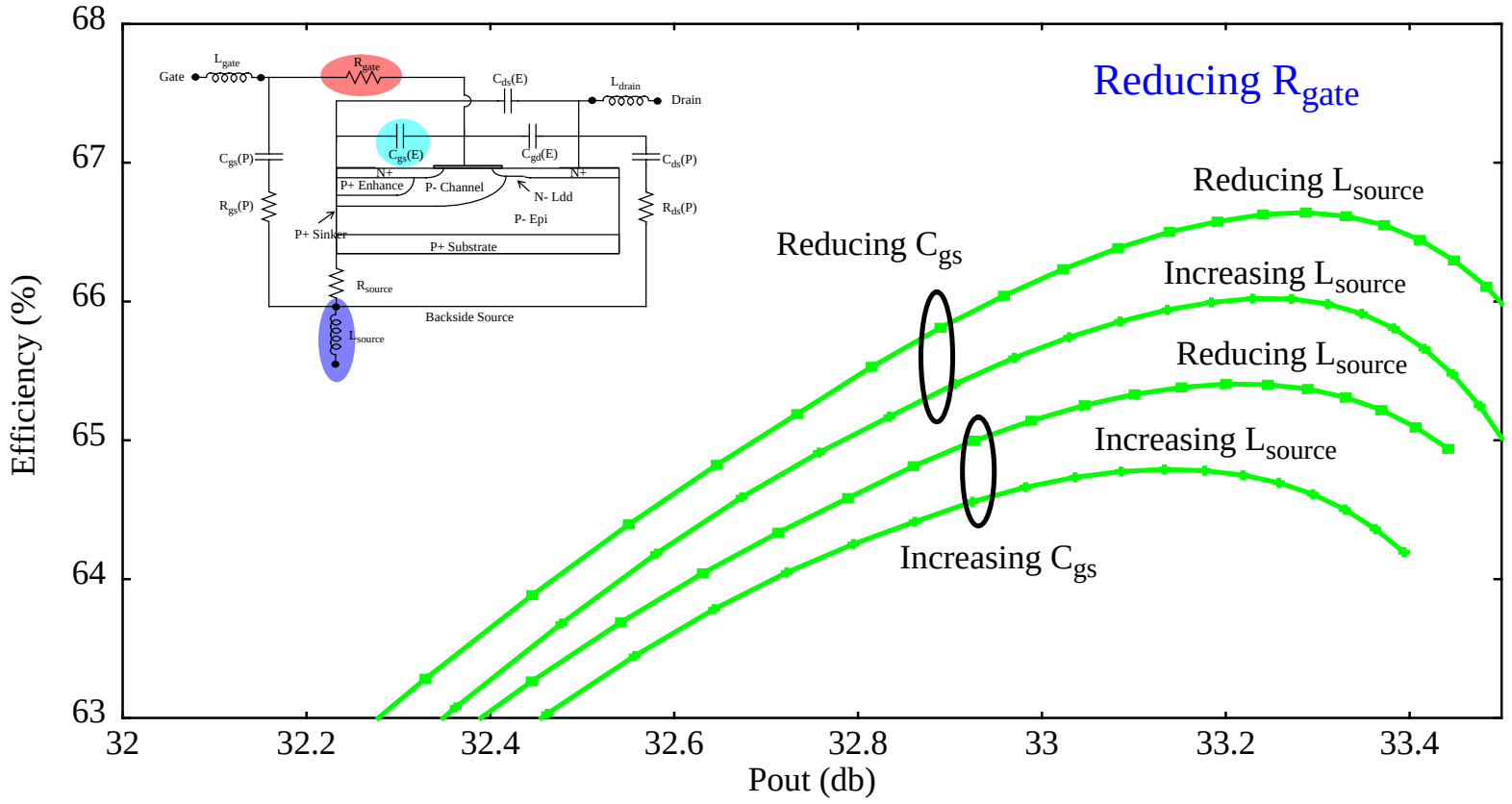
1st Order Parasitic Effects on Efficiency

- Harmonic balance device simulation provides a tool to study the effect of parasitics on the large signal performance of a device.



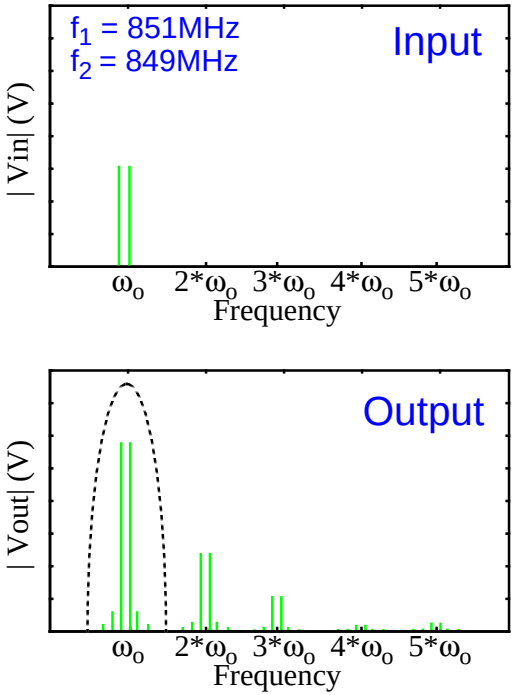
2nd Order Parasitic Effects on Efficiency

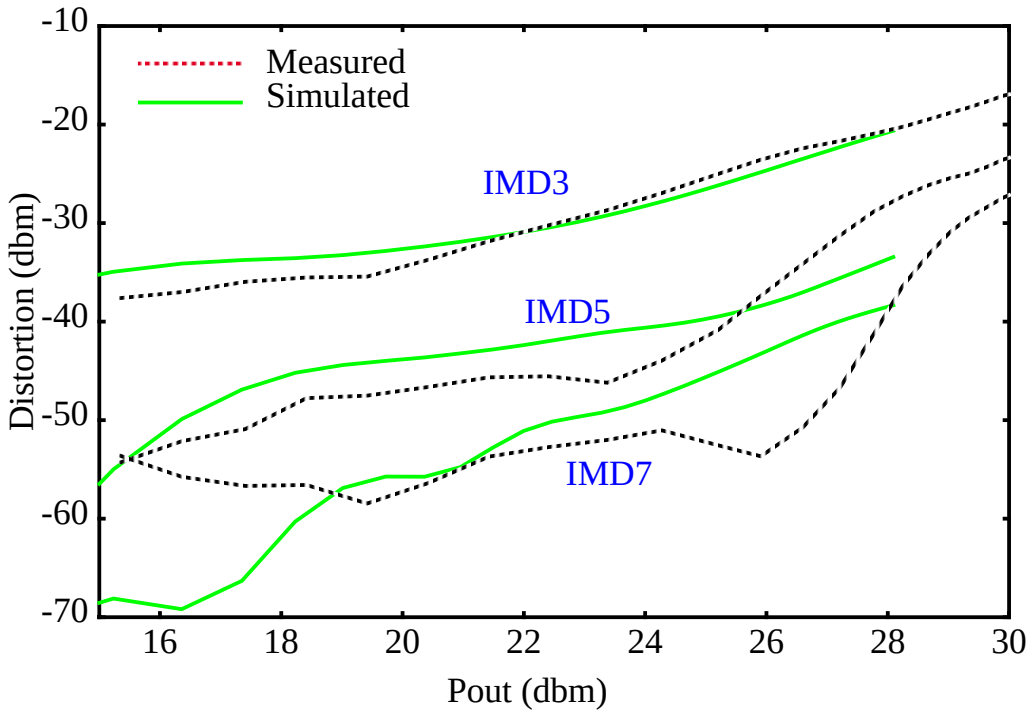
- Examining the curves where R_{gate} is reduced yields an understanding of the second order effects.



Inter-modulation (Comparison to Experiment)

- The interaction of two closely spaced input frequencies generates odd harmonics in the band of interest. (i.e. third order inter-modulation distortion generates {2 x f_1 - f_2} and {2 x f_2 - f_1})



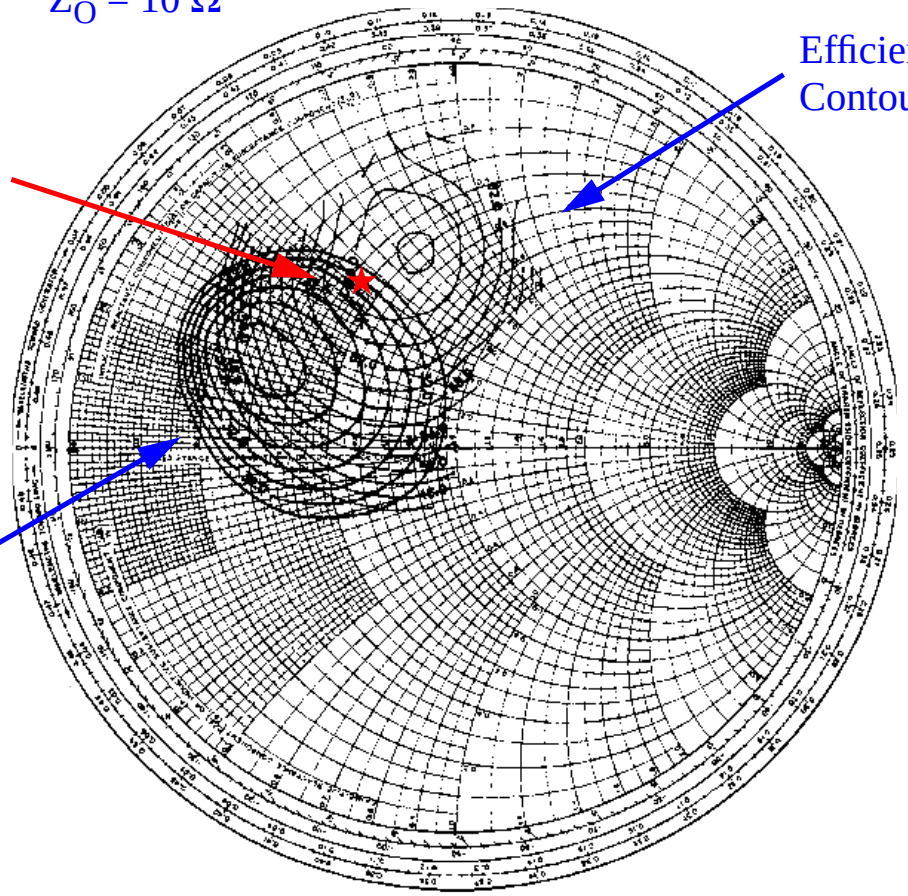


Matching Network Effects

- Matching networks play a critical role in efficiently transferring power from the supply source to the amplifier and from the amplifier to the load.
- The input matching network is designed to reduce reflections back to the supply thus preventing wasted power.
- The output network has multiple functions:
  a. Impedance matching between amplifier output and load to achieve maximum power transfer.
  b. Filter for higher order harmonics.
- A load-pull analysis is used to sweep over multiple matching networks configurations and to calculate gain and efficiency for each of those configurations.
  a. Input power is set to a constant value.
  b. Input matching network is set to minimize reflections.
  c. Output matching network is swept.
  d. Contour plots for gain and efficiency are plotted

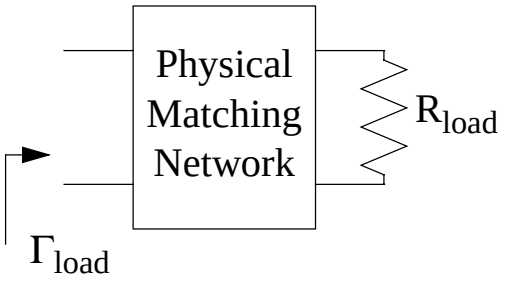
Experimental Load Pull Results

$Z_O = 10\ \Omega$

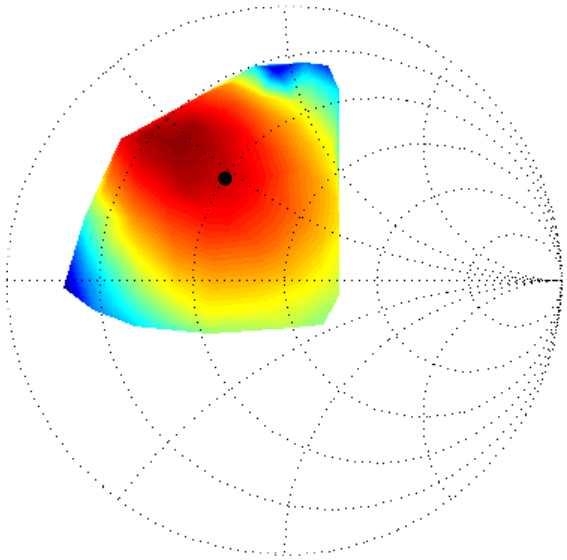


Smith Chart Representation of Γ_{load}

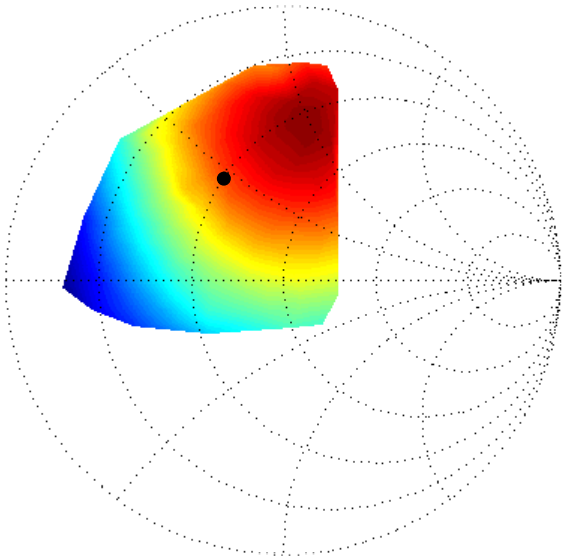
$$\Gamma_{load} = \frac{Z_{load} - Z_o}{Z_{load} + Z_o}$$



Simulated Load-Pull Results



Gain



Efficiency

- The "●" indicates the network used in the gain and efficiency simulations and the one chosen by the experimental measurements.

Contributions

- Extended work on mixed circuit and device simulation for use with larger and more realistic problems. (not presented)
- Parallelized mixed circuit and device simulation so that large problems can be solved on a network of workstations. (not presented)
- Improved PISCES to include a generalized linear circuit through boundary condition equations.
- Integrated PISCES with an harmonic balance solver and developed the boundary condition equations for harmonic balance analysis with circuit components.
- Modeled RF LDMOS devices for use in device simulation to provide predictive analysis.
- **Developed tools and methodologies to aid in RF device design by including the intrinsic physical device with external parasitics and matching networks.**

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