Macroscopic Simulation of Quantum Mechanical Effects in 2-D MOS Devices via the Density Gradient Method

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Abstract—Here, for the first time, are presented results of two-dimensional (2-D) simulations of metal–oxide–semiconductor (MOS) devices, including quantum mechanical modeling throughout the entire device region, calculated using the density gradient method. The importance of quantum mechanical modeling of the entire device structure, including the gate, source, drain, and channel, is demonstrated through one-dimensional (1-D) examples and through analysis of double and single-gated fully-depleted silicon-on-insulator (SOI) devices. A comparison of density gradient results with literature data is also presented.

Index Terms—Capacitance, metal–oxide–semiconductor (MOS) devices, quantum theory, semiconductor device modeling, silicon, silicon-on-insulator (SOI) technology, simulation.

I. INTRODUCTION

G LOBAL, computationally efficient modeling of quantum mechanical effects in metal–oxide–semiconductor (MOS) devices is becoming increasingly important [1], including any semiconductor gate(s) [2], [3]. Previous approaches to treating quantum mechanical perturbations to the solution of classical device equations have included locally applied models such as that of Van Dort [4], and inverse model-based tuning of the physical device parameters [5].

But a macroscopic treatment is clearly superior to one using locally applied specialized models. And distortion of physical device parameters is unable to match behavior over a broad range of biases and parameter values.

II. METHOD

A. Density Gradient Method

The efficiency of two-dimensional (2-D) quantum effect simulation has been improved substantially by the development of the density gradient method [6]. Density gradient simulations up to three dimensions have been published [7], [8]. In two dimensions, results were compared favorably to more rigorous, far more computationally expensive nonequilibrium Green's function calculations [9], [10]. Using the density gradient approach, it becomes for the first time computationally feasible to include macroscopic quantum mechanical modeling in mainstream multidimensional device simulation applications.

For an isothermal system, in the low-field limit where carrier mobility is applicable, flux can be represented in terms of the quasi-Fermi potentials ϕ_e and ϕ_h [11]

$$\boldsymbol{F}_e = \mu_e n \nabla \phi_e \tag{1}$$

$$\boldsymbol{F}_h = -\mu_h p \nabla \phi_h \tag{2}$$

where $\boldsymbol{F}_e$ and $\boldsymbol{F}_h$ are the electron and hole fluxes, μ_e and μ_h are the electron and hole mobilities, and n and p are the electron and hole concentrations.

The quasi-Fermi potentials are related to the "classical" values, ϕ_e^0 and ϕ_h^0, as follows [12]:

$$\phi_e = \phi_e^0 + \frac{2\nabla \cdot (b_e \nabla \sqrt{n})}{\sqrt{n}} \tag{3}$$

$$\phi_h = \phi_h^0 - \frac{2\nabla \cdot (b_h \nabla \sqrt{p})}{\sqrt{p}} \tag{4}$$

where $\psi - \phi_e^0$ and $\phi_h^0 - \psi$ are functions of n or p, according to the appropriate statistics and material parameters, where ψ is the local electrostatic potential. The quantum mechanical influence is controlled by the parameters b_e and b_h, which can be represented

$$b_e = \frac{\hbar^2}{4q m_e N_{dim}} \tag{5}$$

$$b_h = \frac{\hbar^2}{4q m_h N_{dim}} \tag{6}$$

where $m_e \equiv m_e^* m_0$ and $m_h \equiv m_h^* m_0$, with m_0 the free electron mass, are the appropriate electron and hole effective masses. N_{dim} representatives the characteristic dimensionality of the system.[1] In the high-temperature limit, with broad state occupancy $N_{dim} \to 3$. For a one-dimensional (1-D) system, or one in which a single state dominates $N_{dim} \to 1$. This is discussed in [12].

Thus the following system of equations is solved[2] for ψ, $\sqrt{n}$, $\sqrt{p}$, ϕ_e, and ϕ_h

$$\nabla \cdot (\epsilon \nabla \psi) + q(p - n + N_D^+ - N_A^-) = 0 \tag{7}$$

$$\frac{2\nabla \cdot (b_e \nabla \sqrt{n})}{\sqrt{n}} - \left(\phi_e - \psi + \Phi|_{n, kT}\right) = 0 \tag{8}$$

$$\frac{2\nabla \cdot (b_h \nabla \sqrt{p})}{\sqrt{p}} + \left(\phi_h - \psi - \Phi|_{p, kT}\right) = 0 \tag{9}$$

[1]One could use different values of N_{dim} for electrons and holes, but for this work a single value is assumed, and all variation is taken up by the effective masses, m_e and m_h.

[2]The solution is restricted to positive values of $\sqrt{n}$ and $\sqrt{p}$.

$$\nabla \cdot (\mu_e n \nabla \phi_e) + \frac{\partial n}{\partial t} + r = 0 \qquad (10)$$

$$\nabla \cdot (\mu_h p \nabla \phi_h) - \frac{\partial p}{\partial t} - r = 0 \qquad (11)$$

where Φ is the potential function associated with the statistics being used, ϵ is the local permittivity, N_D^+ and N_A^- are the concentrations of ionized donors and acceptors, and r is the net electron–hole pair recombination rate.[3]

The solutions considered here are steady state with zero carrier flux,[4] and thus net recombination is zero. Therefore, $\partial n / \partial t = \partial p / \partial t = 0$; and $\nabla \phi_e = \nabla \phi_h = 0$, except in insulators.

For most of this work, Fermi–Dirac statistics rather than the simpler Boltzmann statistics were used. The latter are inappropriate for carrier concentrations greater than the effective conduction (for electrons) or valence (for holes) band density of states, levels typically exceeded in MOS devices [11].

At contacts, ϕ_e, ϕ_h, ψ, n, and p were fixed.[5] Reflecting conditions were assumed at other simulation domain boundaries. At semiconductor/insulator boundaries, n and p were fixed at $10^{-8}/\text{cm}^3$. Issues associated with boundary conditions in density gradient simulations are discussed in [14].

For extensions to the density gradient theory, see [12].

Throughout this work, the (001) direction is assumed for 1-D solutions, both because it is in this direction that reference data are most readily available, and because MOS devices are typically fabricated with this as the channel plane.

All original simulation data described in this work were generated using Prophet [6].

B. Calibration

1) Introduction: The key parameters in the density gradient method are b_e and b_h, which have variable components N_{dim} and the electron and hole effective masses, m_e and m_h. Due to the implicit simplification of the silicon band structure in the method, and in the low-order approximation involved, the optimal choice of these is nontrivial. Others [7], [15] have used values of $m_e^* = 0.190$ and $m_h^* = 0.490$, with $N_{dim} = 3$. The matter is examined on a limited basis in [16]. Yet justification has not been compelling. One cause for concern is it is known that holes are more strongly affected by inversion-layer quantization than are electrons [17]. If fixed N_{dim} is used, then m_h^* must be less than m_e^* for the model to match this result.

Ancona discusses the choice of b_e in greater depth in [12]. In the low-field limit, for example in weak inversion of a bulk NFET, it is expected that $N_{dim} \to 3$ with $m_e^* \to (m_t^{*2} m_l^*)^{1/3}$, the classical limit, where m_l^* and m_t^* are the m_0-normalized longitudinal and transverse conduction band effective masses. As inversion becomes stronger, the spacing between eigenstates becomes large in comparison to the thermal energy $k_B T$, and

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[3]As is discussed in [13], The treatment of SRH-recombination in the density gradient method is nontrivial, as it is no longer the case in equilibrium that $np \to n_i^2$.

[4]Simulation of carrier transport with the density gradient method presents no difficulties. However, the simulator used in this work lacked implementation of high-field transport models.

[5]Quasi-neutrality with $np = n_i^2$ was assumed for n and p. Thus, contacts could not abut semiconductor/insulator boundaries.
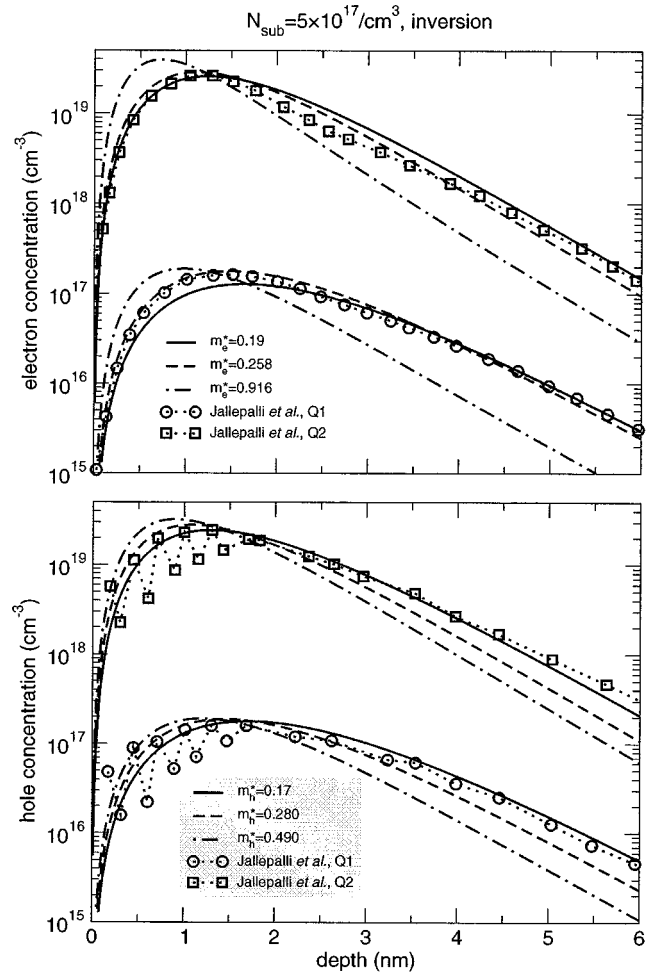

Fig. 1. Electron and hole concentrations in the channel compared for roughly the same peak concentrations in inversion. Density gradient profiles are shown for three choices of electron and hole effective mass. Reference data are from full-band calculations in [19].

thus the lowest-energy state dominates; $N_{dim} \to 1$ and $m_e^* \to m_l^*$.

The result is that b_e stays relatively constant. The values from [17], $m_l^* = 0.916$, and $m_t^* = 0.19$ yield $m_e^* N_{dim}$ varying from 0.96 in the low field limit to 0.916 in the high field limit. Ancona [12], after comparing density gradient calculations to self-consistent Schrödinger–Poisson calculations in one dimension, still advises allowing b_e to be treated as a fitting parameter due to the influence of "higher order terms" neglected in the density gradient formulation used here.

Wettstein *et al.* [18] follows this approach, fitting b_e to 1-D Schrödinger-simulated C–V curves, yielding a result equivalent to $m_e^* = 0.28$ for $N_{dim} = 3$. They also show some brief results of bulk and dual-gate NMOS simulations. However, neither true 2-D effects nor silicon gate effects are considered.

Holes are not addressed in these works, and therefore, the relevant parameters also need to be calibrated against literature data.

2) Inversion: Fig. 1 compares the electron and hole profiles in substrates doped uniformly at $5 \times 10^{17}/\text{cm}^3$, p or n type, for two approximate net areal carrier concentrations. Three values of each effective mass are considered. For electrons, the
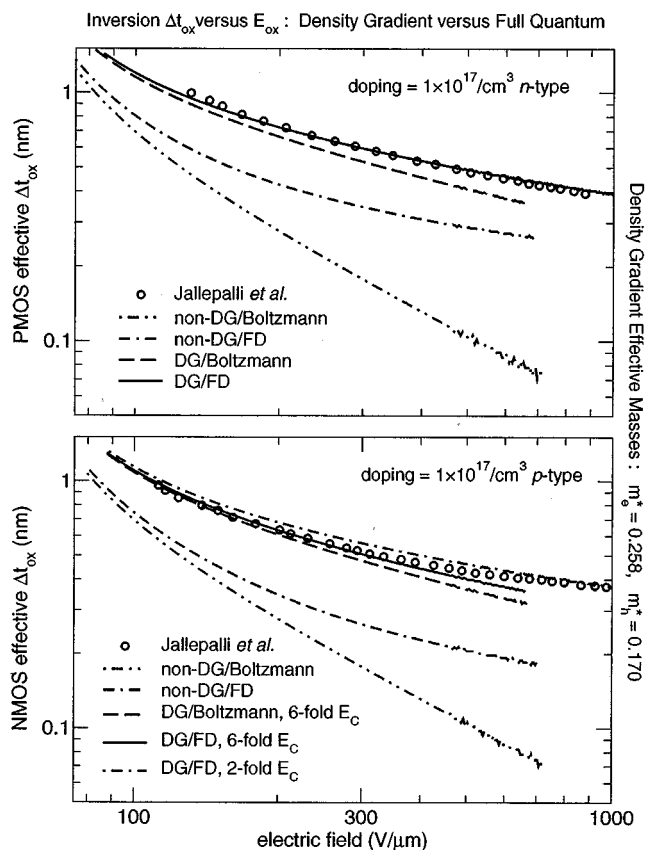
Fig. 2. Effective oxide thickness associated with electron (NMOS) and hole (PMOS) inversion layers in $10^{17}/cm^3$-doped MOSCAPs, plotted as a function of SiO_2 electric field. Density gradient simulations with both Fermi–Dirac and Boltzmann statistics are compared with self-consistent Schrödinger–Poisson simulation from [19], as well as classical simulations. For holes, note the excellent fit afforded by the density gradient approach with Fermi–Dirac. For electrons, the full quantum solution is consistent with the DG–FD approach with a transition from sixfold to twofold conduction-band degeneracy.

Fig. 3. Fit to data reported by [20] using the density gradient method with Fermi–Dirac statistics.

transverse effective mass $m_t^* = 0.19$, the longitudinal effective mass $m_l^* = 0.916$ [17], and $m_e^* = 0.258$ which is somewhat less than the theoretical values discussed earlier for electrons, $(m_t^{*2}m_l^*)^{1/3}$ and $m_l^*/3$ for $N_{dim} = 3$. $m_e^* = 0.258$ fits the data the best, especially near the peak where it is most important to do so.

Using these and other values of the electron effective mass, the values interpolated to match the mean electron position in the data from [19] for matching integrated electron profiles were $m_e^* = 0.254$ and $m_e^* = 0.274$ for the two curves. Thus, the value $m_e^* = 0.258$ is considered adequate for this work.

For the holes, values used include the heavy hole mass 0.49 [7], a value approximating the light hole mass 0.17, and the geometric mean 0.28. Again, $N_{dim} = 3$ is assumed. There is considerable variation in the data from [19] near the interface, but for the rest of the profile, $m_h^* = 0.17$ yields a good match. While this mass is characteristic of light holes, a similar value of b_h is achieved with heavy holes with $m_h^* = 0.49$ and $N_{dim} = 1$.

The effect on capacitance is demonstrated in Fig. 2. Effective masses used are taken from the values shown to have the best match to the profiles in Fig. 1. Data from the full-band model due to [19] is used as a reference. Note the excellence of the fit achieved when Fermi–Dirac statistics are used. For electrons,
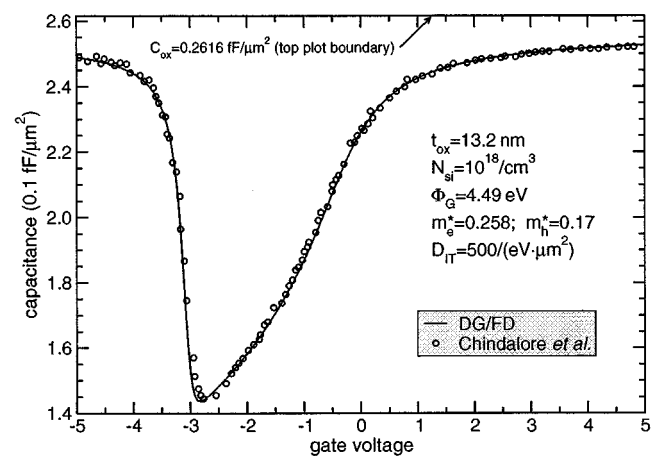
the result is consistent with a shift between sixfold and twofold conduction band degeneracy as the field is increased. To thus model the electron-inversion layer with maximal accuracy, a variable conduction-band effective density of states should be used, perhaps via an approach similar to the "nonlinear density gradient" method described by [12]. For simplicity in this work, a sixfold conduction band degeneracy is generally assumed.

3) Accumulation: A 1-D C–V simulation was done with the density gradient method and Fermi–Dirac statistics to check the validity of $m_e^* = 0.258$ in accumulation. Data were taken from [20], on what was reported to be a metal gate capacitor with $t_{ox} = 13.25$ nm on a $10^{18}/cm^3$ n-type substrate. The effective gate workfunction[6] and interface state density were set to optimize the fit, and the gate oxide thickness was reduced by 0.05 nm,[7] a 0.4% change, to improve the fit further. The result, shown in Fig. 3, captures the measured behavior in both inversion and accumulation.

For holes, things are more complicated. It has been observed that using a value characteristic of the heavy hole band, $m_h^* = 0.49$, works better in accumulation than the $m_h^* = 0.17$, which better matched inversion carrier profiles. One explanation is that the weaker confinement associated with the accumulation layer results in a transition from $N_{dim} = 1$ to $N_{dim} = 3$, while the value of m_h^* remains close to 0.49. However, the details of the valence band physics are beyond the scope of this work. Assuming $N_{dim} = 3$, m_h^* will be taken as 0.17 in inversion or other states of strong confinement and 0.49 in accumulation.

4) Calibration Conclusion: For holes, $m_h^* = 0.49$ will here be used in regions of weak confinement (e.g., accumulation in a bulk device), while $m_h^* = 0.17$ will be used in regions of strong confinement (including inversion). For electrons, $m_e^* = 0.258$ showed itself to produce excellent fits to both accumulation and inversion-mode data. These values assume $N_{dim} = 3$, an assumption not valid in all conditions. For the purposes of the density gradient method, the important thing is the values of b_e and b_h.

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[6]This includes a contribution from fixed charge in the oxide and at the silicon interface.

[7]This is consistent with [20], who inverse-modeled the reported oxide thickness value.
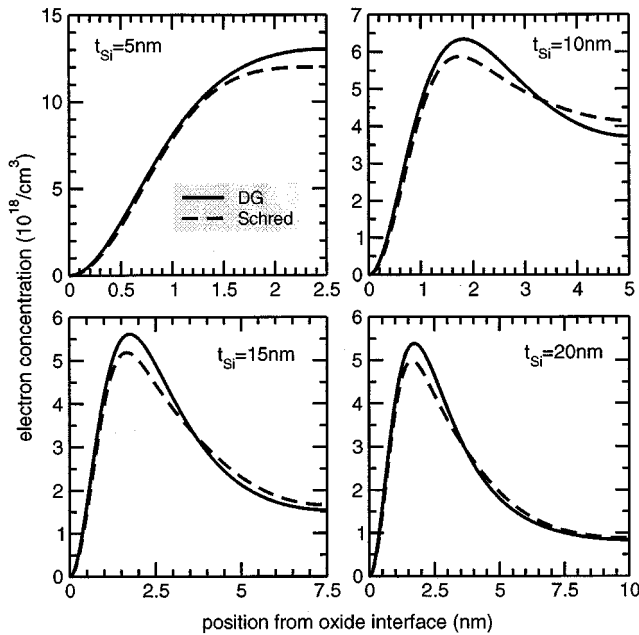
Fig. 4. Comparison of simulations of 1-D fully depleted dual-gate SOI structure, comparing density gradient method to the *Schred* Schrödinger–Poisson solver for different values of the silicon thickness. In all cases, the gate oxides are 1.5 nm, the channels are essentially undoped at $10^{14}/\mathrm{cm}^3$ p-type, and the system is in equilibrium. For the density gradient calculations, $m_e^* = 0.258$, $m_h^* = 0.17$, $N_{dim} = 3$, and the gate workfunction was 4 eV. A slightly different workfunction was used in *Schred* to accommodate its different silicon electron affinity.
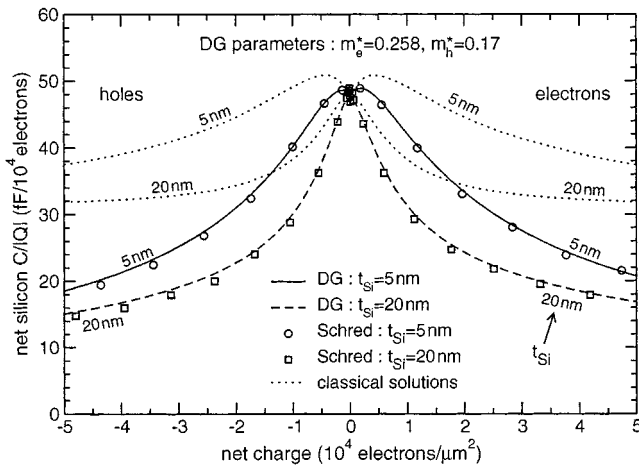

Fig. 5. Comparison of net charge-normalized silicon capacitance from simulations of 1-D fully depleted dual-gate SOI structure from Fig. 4. Channel charge was modulated with gate workfunction, as this is a one-terminal device.

III. ONE-DIMENSIONAL MODELING

A. Dual-Metal-Gate Fully-Depleted MOSFET

Among the simplest devices which exhibit the effects of quantum confinement is the 1-D dual-metal-gate fully depleted SOI MOS device. With the two metal gates at the same potential, one need simulate only half the structure, and assert a reflecting boundary condition in the middle of the silicon layer. This device was simulated in equilibrium[8] for different values

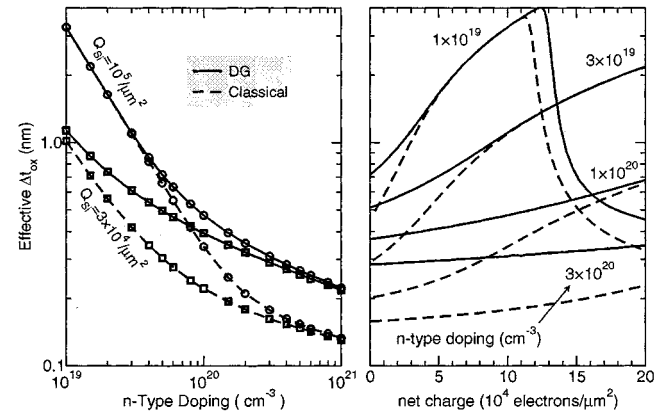[8]Quasi-Fermi levels in silicon match those on gates.

Fig. 6. Modeled effective SiO_2 thickness increase associated with heavily doped silicon gates analyzed with density gradient method and classical analysis.
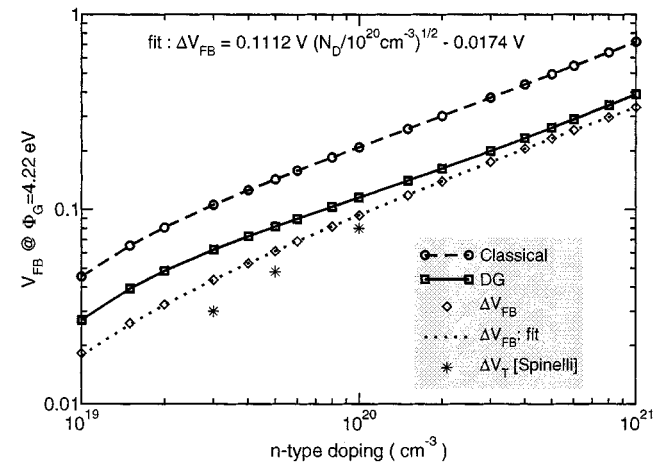

Fig. 7. Modeled effect on flatband voltage versus doping for heavily doped silicon MOSCAP with a metal gate of workfunction 4.22 eV. Some threshold voltage data from [2] are also shown.

of the silicon thickness and gate workfunction. A comparison of results using the density gradient approach to those using *Schred 2.0*, a Schrödinger–Poisson solver due to [21], are shown in Fig. 4. Note that as the silicon thickness is decreased from 20 nm to 5 nm, the electron profile goes from two distinct peaks to a single peak at the symmetry point.

The net silicon capacitance is plotted versus net silicon charge in Fig. 5. The deviation from the classical result matches quite well. Note despite the fact the holes represent a state of accumulation, the b_h associated with inversion in the bulk device was used. This is because the confinement is considered strong in this device due to the thinness of the silicon layer.

B. Bulk Si-Gate MOS Capacitor

1) Gate: Despite the fact that amorphous or polycrystalline silicon has been used as the gate electrode in CMOS technology for decades, only recently is the importance of quantum mechanical modeling of the gate being recognized. For example, consider the work of Spinelli *et al.* In [2], the effect of quantum exclusion of carriers from the oxide–polycrystalline silicon interface on capacitance and on threshold voltage is discussed, with the effect on inverse modeling of the gate doping profile
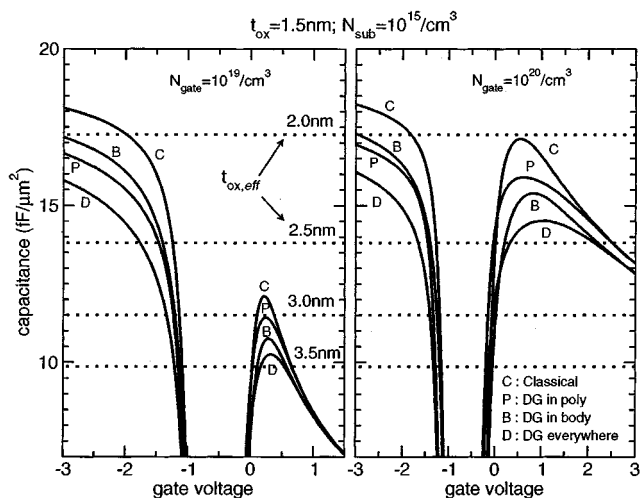
Fig. 8. One-dimensional (1-D) modeling of silicon-gate MOS capacitors with substrate doping of $10^{15}/cm^3$ p-type, a 1.5 nm-thick gate oxide, and gate doping levels of $10^{19}/cm^3$ and $10^{20}/cm^3$ n-type. Curves are labeled according to where, if anywhere, the density gradient method was applied. ϵ_{ox}/t_{ox} values for various values of t_{ox} are labeled on the graph to give a feel for the degree of net capacitance degradation.
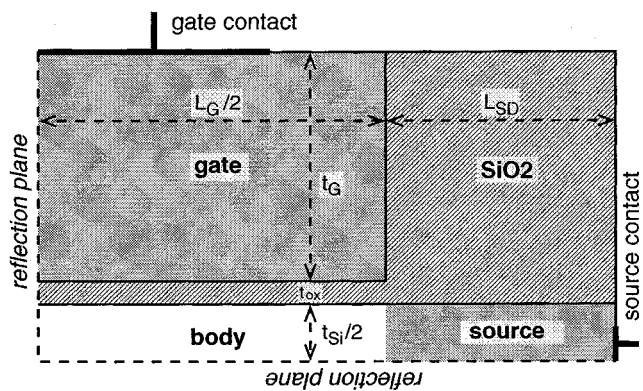

Fig. 9. Simulated region schematic of 2-D dual-gate fully depleted SOI MOSFET. Only a quarter of the full device is rendered: the remainder is captured via the symmetry planes.

analyzed in [3]. Unfortunately, the work is limited to 1-D analysis, and thus is not readily integrated into 2-D simulation.

One-dimensional (1-D) analysis does have the advantage of simplicity of interpretation, however. Some results calculated using the density gradient method are presented here. In all cases, the gate material was modeled as (001) silicon. This is not an accurate representation of the polycrystalline material found in the gates of most technologies, in which the surface orientation varies between grains. Furthermore, no modeling of grain boundary states or of bandgap narrowing from either the grains or from high dopant concentrations is done here. Nevertheless, the results do provide qualitative insight into the effect of the quantum exclusion. Spinelli's work also modeled the gates as single-crystal silicon.

Fig. 6 shows the effective SiO_2 thickness increase associated with a silicon gate, comparing results from density gradient and classical simulation. The effect of doping for a fixed net charge (and therefore fixed oxide field) and the effect of net charge for fixed doping are both shown. In the low-doping and high-field regimes, where depletion is substantial, the effect of the quantum mechanical exclusion on the capacitance is negligible. However, for a regime typical of modern devices, with doping near $10^{20}/cm^3$ and charge densities up to $10^5/\mu m^2$ (oxide field of 1 volt/2.1 nm), the disparity can exceed 0.1 nm.

Fig. 7 shows the result on flatband shift. A metal–SiO_2–silicon capacitor was modeled, assuming a metal workfunction of 4.22 eV. Plotted is the resulting flatband voltage[9] versus doping level. As is discussed in [2], the exclusion of free carriers from the Si–SiO_2 interface results in the formation of a charge dipole which shifts the effective workfunction of the silicon. This shift, plotted in the figure, is roughly proportional to $\sqrt{N_D}$ for large N_D. Also plotted are some data extracted[10] from Fig. 9 in [2] of the "threshold

voltage" shift due to the quantum mechanical modeling relative to classical modeling. The threshold condition represents more depletion than the flatband condition, so that the magnitude versus doping is a bit less is expected.

2) Full Device: A full device was simulated with the density gradient method applied either in the body, the gate, both, or neither. Results are shown in Fig. 8 for gate doping levels of $10^{19}/cm^3$ and $10^{20}/cm^3$ n-type. For large negative gate biases, with both the gate and the body in accumulation, quantum mechanical modeling of both the gate and body is clearly important. In moderate inversion both again play a role. As the gate bias increases further and gate depletion becomes substantial, the quantum mechanical effects in the gate become less important. There remains an effective threshold voltage shift due to the quantum mechanical modeling of the gate, however.

IV. TWO-DIMENSIONAL MODELING

A. Dual-Si-Gate Fully-Depleted MOSFET

As was previously discussed, the fully-depleted silicon-on-insulator (SOI) transistor is among the simplest structures to investigate the effects of quantum effects on device modeling. Here, some 2-D results will be considered.

The simulated region is shown schematically in Fig. 9. Only a quarter of the device was actually simulated, exploiting the symmetry of the structure. This results in the constraints that gates be biased together, and the source and drain be biased together. The gate and source were each uniformly doped n-type. The source doping had a lateral Gaussian extension into the body with $\sigma = 0.5$ nm. The silicon body was doped $10^{12}/cm^3$ p-type. The edge of the uniformly doped source region is aligned with the edge of the gate.

Gate charge is balanced by charge in the silicon. This is partitionable into two components—the "channel charge" and the "fringe charge." The channel charge is determined by assuming the fringe region fails to extend to the center-channel (the left reflection plane in Fig. 9). The channel charge for the quarter-device is then the areal charge density at center-channel times the half gate length. The remainder of the net charge is the fringe charge.

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[9]V_G, yielding zero net silicon charge.

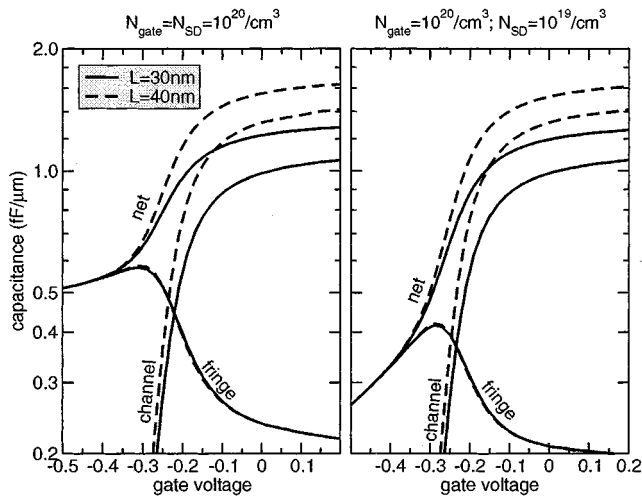[10]The approximate resolution of the extraction is ± 1 mV.

Fig. 10. Capacitance components for two channel lengths, two source dopings, for full dual-gate FDSOI device. Device parameters include $t_{ox} = 1$ nm, $L_{SD} = 10$ nm, $t_{Si} = 5$ nm, $t_G = 50$ nm, and $N_{body} = 10^{12}/\text{cm}^3$ p-type.
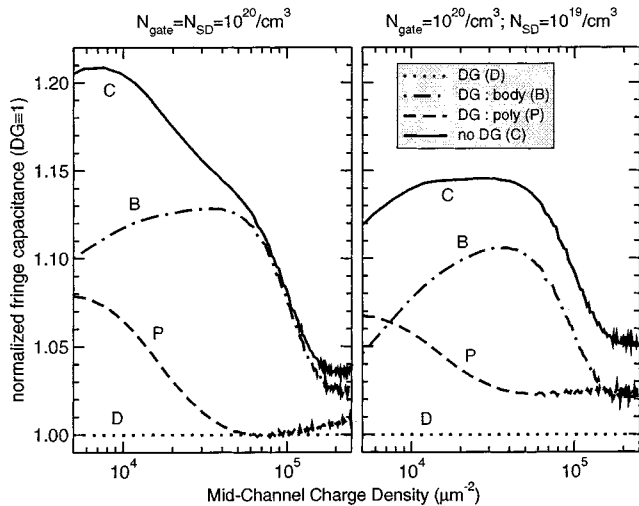

Fig. 11. Fringe capacitance normalized to density gradient value versus midchannel net body charge for $L_G = 30$ nm device from Fig. 10. Some of the fine structure in the plots is due to numerical noise.
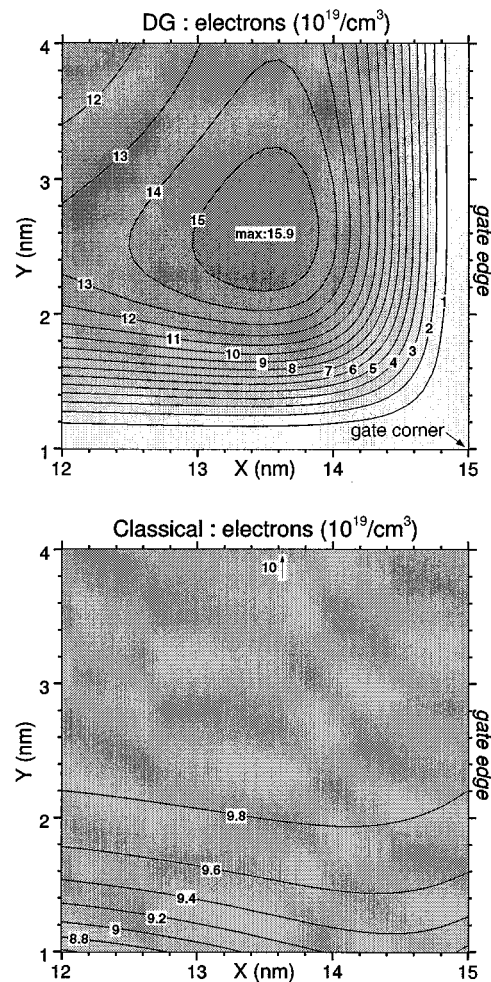

Fig. 12. Electron concentration near the gate corner for a dual-silicon-gate FDSOI device. Device parameters include $t_{ox} = 1$ nm, $L_G = 30$ nm, $N_{gate} = 10^{20}/\text{cm}^3$ n-type. Note the significant "pileup" of electrons near the corner in the density gradient case.

The baseline structure simulated had a gate length of 30 nm (simulated region 15 nm), a silicon thickness of 5 nm (simulated 2.5 nm), a gate oxide thickness of 1 nm, a gate thickness of 5 nm, and a source length of 10 nm. Gate doping was $10^{20}/\text{cm}^3$.

An example of these capacitance components is shown in Fig. 10. Results are shown for source dopings of $10^{19}/\text{cm}^3$ and $10^{20}/\text{cm}^3$, channel lengths of 30 nm and 40 nm. Capacitance represents the whole device (front and back, source and drain). The fringe capacitance is effectively gate-length-independent over this gate length range. Over the regime where channel capacitance is small, essentially all capacitance is fringe capacitance. When the electron concentration in the channel becomes appreciable, a component of the capacitance [11] call the "inner fringe" capacitance is shielded by the channel, leaving only the "outer fringe" and "overlap" components. The reduction of fringe capacitance with reduced source doping is clear, especially in the subthreshold regime, where inner fringe capacitance is significant.

Of primary interest to this work, however, is the effect the density gradient method has on the result. The fringe capacitance, normalized to the density gradient value, is plotted in Fig. 11 versus the midchannel charge density. Plotting in this fashion eliminates the effect of simple threshold shifts. As can be seen, quantum mechanical modeling both in the gate and in the body is important for accurate determination of the fringe capacitance.

Electron concentration profiles near the gate corner, as simulated under zero bias for 30 nm n-type gates with classical or density gradient analysis, are shown in Fig. 12.

With an identical mesh and gate voltage step, the full density gradient solution required 29.4% more time to generate than the classical solution for the baseline device. The density gradient approach increases the required mesh and bias point densities somewhat, so proper benchmarking requires more care. Nevertheless, it is clear the density gradient approach offers enormous speed advantages relative to more traditional quantum mechanical approaches such at that used in [1].

One can improve the fit of the classical device simulation considerably by treating the oxide thickness and silicon thickness as adjustable parameters, then adjusting oxide/silicon fixed charge
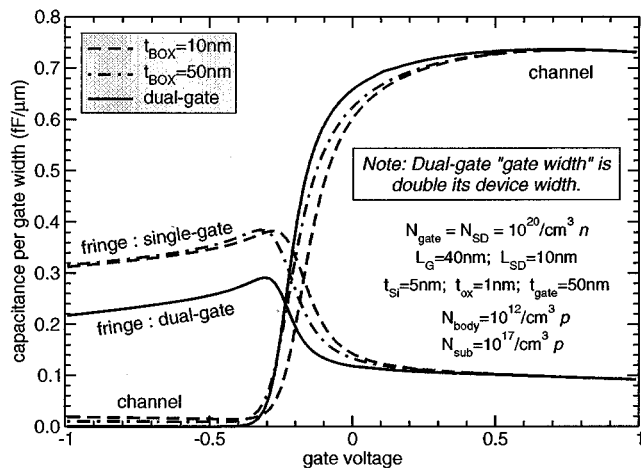
Fig. 13. Fringe capacitance of dual gate and single gate device, normalized per unit gate width, as calculated using the density gradient method. The single-gated device is simulated for two values of the buried oxide thickness, each on a $10^{17}/\text{cm}^3$ p-type substrate.

to compensate the error in threshold voltage. However, the Δt_{ox} to use is bias, geometry, and doping dependent, and thus this approach is clearly inferior for predicting the effect of device design changes. Furthermore, while the approach is feasible in one dimension, in multiple dimensions the problem grows in complexity, and the geometry changes needed to mimic quantum mechanical effects throughout the device become highly nontrivial. And of course, effects like those shown in Fig. 12 will not be predicted.

B. Single-Si-Gate Fully-Depleted MOSFET

Results of a similar analysis of a single-gated device are shown in Fig. 13. Capacitance is plotted per unit gate width, and thus represents twice the device width for the single-gated structure as it does for the dual-gated one.

The fringe capacitance shows a marked difference. In depletion and weak inversion, the inner fringe capacitance is larger in the case of the single-gated device. The gate can couple to the full depth of the source/drain, while in the dual-gated device, the opposite gate provides some shielding. In strong inversion, the inner fringe capacitance is screened by the inversion layer, leaving the overlap and outer fringe capacitances, which are quite similar in the two devices.

The two values of the buried oxide simulated represent a "thick" value of 50 nm, and a "thin" value of 10 nm such as might be chosen to improve the short channel margin on thicker-silicon FDSOI [22]. The difference is primarily a threshold shift. The only notable capacitance effect is increased gate-to-substrate coupling for the thinner buried oxide. Fringe capacitance values are not strongly affected.

V. CONCLUSION

The density gradient method, despite its relative simplicity, effectively captures many of the important quantum mechanical effects important to devices in the decananometer regime. The great advantage it has over some other approaches is its global application, including all regions of a multidimensional device, and computational efficiency.

In MOSFETs, quantum mechanical effects in the channel have received a lot of attention. Yet quantum mechanics in a silicon gate are also important to device operation and must be modeled to accurately predict the electrostatic behavior.

In the example of a dual-gate fully-depleted SOI MOSFET, quantum modeling of the gate and of the body are of comparable importance in predicting the fringe capacitance. The gate modeling also results in a shifted device threshold voltage prediction. A comparison with single-gate MOSFETs at a 5 nm silicon thickness shows reduced fringe capacitance in the subthreshold regime due to screening of the inner fringe capacitance by the opposite gate.

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