Quantum Simulation of Nanoscale Surround-Gate MOS Devices

Daniel Connelly (djconnel@ieee.org); Acorn Technologies, Palo Alto, CA
Zhiping Yu (yu@gloworm.stanford.edu); Stanford University, Palo Alto, CA
Dan Yergeau (yergeau@gloworm.stanford.edu); Stanford University, Palo Alto, CA

***Abstract*—Three techniques for the modeling the effect of quantum mechanical exclusion of carriers from oxide/semiconductor interfaces are examined, using a cylindrical MOS device as a test structure to show two-dimensional effects. Classical modeling , but adjust physical device parameters to "effective" values. Another approach is to perturb the silicon bandstructure near oxide interfaces, as demonstrated by Vande Voorde's extension of the Van Dort model. A final approach is a macroscopic quantum model, the density gradient method, which has been shown to have excellent matching to more rigorous approaches. The superiority of the density gradient approach is demonstrated for these structures in the two-dimensional regime.**

***Index Terms*—Capacitance, MOS devices, Quantum theory, Semiconductor device modeling, Silicon, Simulation**

I. Introduction

In their conceptually simplest form, surround-gate MOS devices are a cylinder of silicon (the body) surrounded by gate oxide covered with the gate electrode. Contact(s) to the silicon body are made at one or both ends of the cylinder.[1] The gate thus controls the silicon from all sides, minimizing charge sharing effects, and increasing control at short channel lengths relative to even planar dual-gate designs of comparable silicon thickness/diameter [1][2].

In addition to being useful for circuit integration, these devices are an excellent test vehicle for two-dimensional quantum mechanical effect modeling.

In bulk, planar homostructure FETs, where carrier confinement is well characterized by the electric field near the channel surface, heuristic approaches to improving fitting of C-V curves have been proposed. The most famous of these is the method of Van Dort *et al.* [3]. An extension to this method is due to Vande Voorde *et al.* [4]. In both of these, the quantum mechanical effect of the interface is modeled as an effective bandgap broadening which depends on electric field and on distance from the interface.

But for ultra-thin fully-depleted SOI structures, there need not be a local electric field for the effects of confinement to be significant; carriers may "feel" the influence of multiple interfaces simulateously as these interfaces come into close proximity. Thus the above models are expected to be inadequate in this regime.

One remarkably simple approach is the density gradient method of Ancona and Iafrate [5]. Model coefficients were calibrated against one-dimensional data and applied to one and two-dimensional MOS devices in [6]. Previously, analysis of field emitter tips, a strongly three-dimensional device, was presented by Ancona [7]. Asenov *et al.* used three-dimensional density gradient modeling to analyze the effects of local variation in MOSFETs [8][9]. But while true multi-dimensional effects were considered in these works, validation against more rigorous approaches in two or more dimensions wasn't done.

[1] A transistor or gated diode would need two contacts, while a capacitor could be formed with only one.

II. Details

The simulated structure is shown schematically in Figure 1.

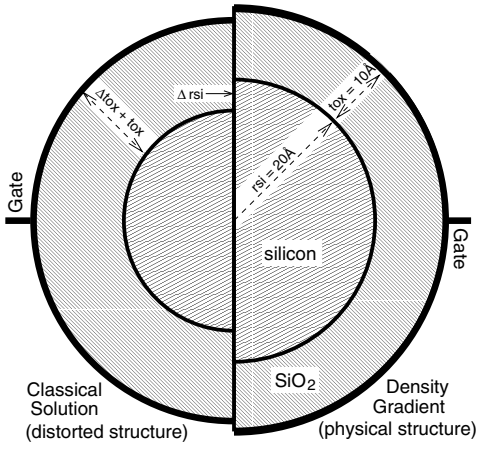

Fig. 1. Schematic of cylindrical FET structure. The physical structure is shown in the right half of the cross-section, while the left shows a perturbed structure, such as might result from inverse modeling, used for classical simulations to better fit the quantum mechanical results.

Simulations were done with Prophet [10] (including all of those using the density gradient model) or Medici by Avanti Corporation [11] (including all of those using the Vande Voorde model). No calibration of any models was done specifically for the structures examined in this work.

Axial symmetry was exploited by simulating the devices in a one-dimensional domain, using cylindrical coordinates. Since there was no explicit source with which to effect a fermi level separation between the gate and the body, the "bias" was controlled by changing the gate workfunction from the "baseline" value of 4.1 eV. This works exactly as long as the oxide is modeled as a perfect insulator, as was done here.

The baseline oxide thickness was 1.0 nm. An SiO_2 permittivity of $3.9\,\epsilon_0$ was assumed in all cases, where ϵ_0 is the vacuum permittivity. Silicon was assigned a permittivity

of $11.7\,\epsilon_0$, a bandgap of 1.1245 eV, an effective conduction band density of states of $2.8 \times 10^{19}/\mathrm{cm}^2$, an effective valence band density of states of $1.02 \times 10^{19}/\mathrm{cm}^2$, and an electron affinity of 4.17 eV. The system temperature was 300 K. Fermi-Dirac statistics were used in all cases.

For the density gradient simulations, values calibrated to one-dimensional full-band quantum mechanical data on (001) surfaces were used : $m_e = 0.258m_0$ and $m_h = 0.17m_0$, where m_0 is the free-space electron mass [6].[2] A six-fold conduction band degeneracy was assumed[3].

III. Silicon Capacitance

The silicon capacitance as a function of surface area-normalized charge is shown for $r_{Si} = 1\,\mathrm{nm}$ devices in Figure 2. Classical and quantum results are shown for both simulators. In principle, the classical results should agree exactly. The quantum results were generated using different models (density gradient in Prophet *versus* Vande Voorde in Medici), and therefore exact agreement isn't expected. Qualitatively, the quantum mechanical effect on capacitance predicted by the density gradient simulation is captured quite nicely by the Vande Voorde model.

It is common practice when doing classical device simulation to set the oxide thickness to match measured electrical data, rather than using a "physical thickness" determined using other methods, to accomodate quantum mechanical effects, among other phenomena. This approach, however, cannot match results over anything but a very limited range of biases. Figure 2 also shows the effective oxide thickness which would need to be added to the "classical device" to make the capacitance match that of the "quantum device" across a range of silicon area-normalized charge values. The value is strongly dependent on silicon charge, and therefore is also strongly dependent on gate bias. The Δt_{ox} predicted by the Vande Voorde method is qualitatively similar to that predicted by the density gradient method.

IV. Charge-Radius

Device charge at a bias of $V_G = 0.5\,\mathrm{V}$ (reference $\Phi_G = 4.1\,\mathrm{eV}$), normalized by channel surface area, is plotted in Figure 3.[4] Results are also shown for the gate bias yielding the same magnitude but opposite sign of total silicon charge.

For the classical model, carriers in the semiconductor are generally closer to the oxide interface than they are for the density gradient case. To match the scaling behavior, an effective offset in silicon radius, as well as the offset applied to oxide thickness, is thus needed. The oxide thickness offset was established to match the density gradient and classical charge at the 0.5 V bias for $r_{Si} = 1\,\mu\mathrm{m}$. For the hole intensive case, at the same density gradient charge magnitude, a different oxide thickness was needed. The silicon thickness offsets for the two biases were then extracted to match the radius scaling behavior of the classical and density gradient simulations, for moderate radii. Area normalization is done using the physical radius, which differs from the simulated radius in the case of the classical simulation.

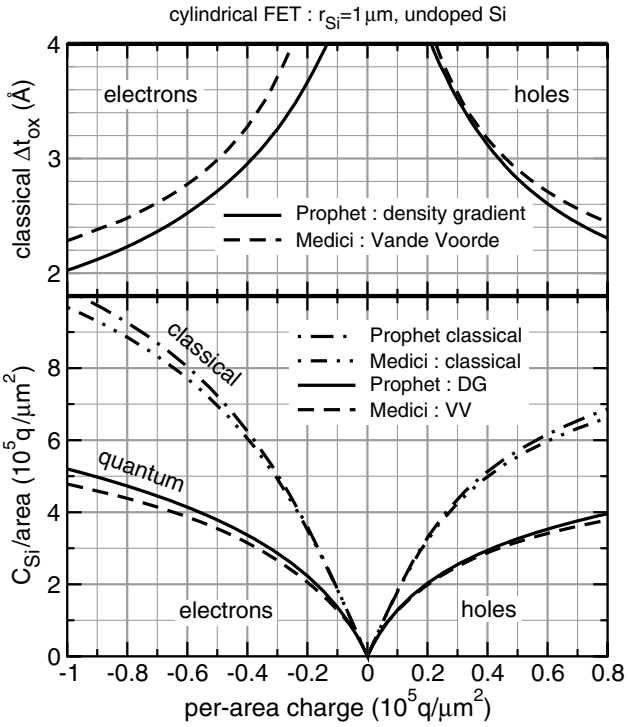

Fig. 2. C-Q characteristics of silicon surface for $r_{Si} = 1\,\mu\mathrm{m}$ devices. Results are shown for both Medici and Prophet, with the former giving a slightly greater prediction of capacitance for both quantum and classical cases. The Vande Voorde model qualitatively captures the quantum effect on capacitance predicted by the density gradient model. Also shown is the effective oxide thickness associated with the difference in capacitances between the classical and quantum models. The result is strongly Q-dependent, and therefore V_G-dependent in a gated device. For $|Q| < 10^4/\mu\mathrm{m}^2$, numerical noise dominates.

The classical and density gradient results diverge at approximately a 2 nm radius. Below this value, the approximation that there's a fixed difference in silicon radius and oxide thickness clearly breaks down.

No physical structure offsets were applied for the Vande Voorde calculation – a key motivation to using quantum models is to directly simulate the physical device structure. Yet the radius scaling is poor, as the quantum exclusion effect of small radii isn't sufficiently treated. To the contrary, the electric field focusing dominates, and the charge per unit area increases, rather than decreases, as the radius falls below 4 nm, especially for the electron-dominated case.

[2] For cylindrical structures, the (001) surface is not necessarily an optimal reference, as surface orientation varies across the interface. Yet the dependence of the quantum mechanical offset on effective mass is weak [12], and so the effect of more rigorously derived effective mass values is not profound.

[3] As was shown in [6], effective conduction band degeneracy can be reduced by quantization.

[4] On this scale, the Prophet and Medici classical results were quite close, all classical results from here onward are from Prophet.

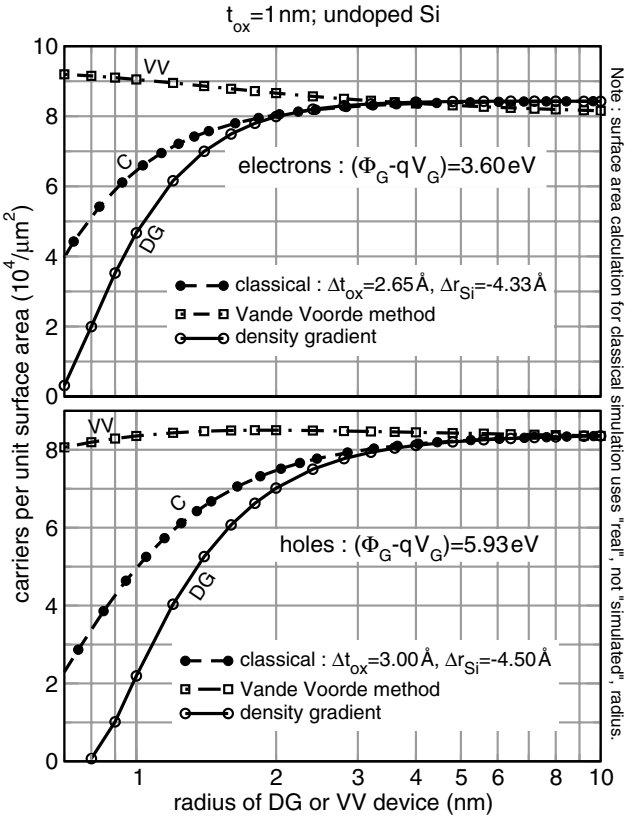

Fig. 3. Dependence of total charge on device radius, as predicted by the three methods considered here, for positive bias. Physical dimensions are adjusted only for the classical method, with different offsets needed for the different bias values.

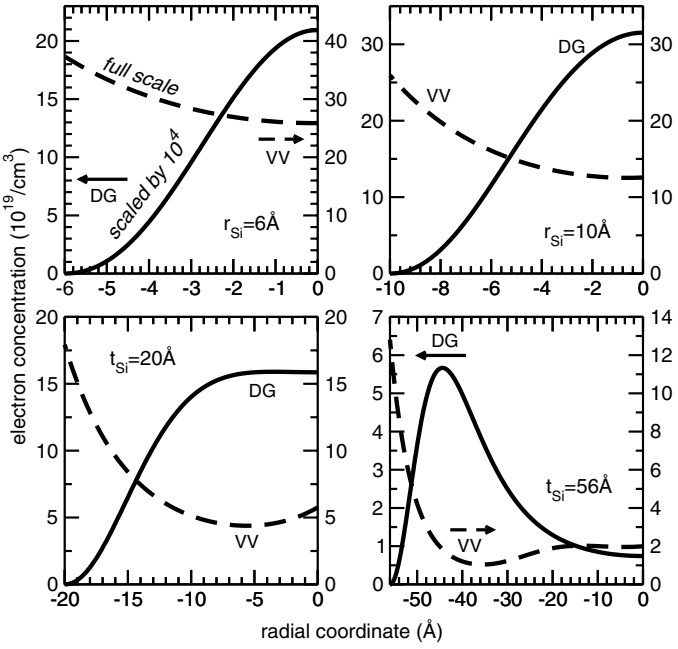

Fig. 4. Carrier distribution with respect to radial coordinate for the density gradient method and the Vande Voorde method. Note the transition of the peak in the density gradient carrier profile to the center of the device as the radius drops to 2 nm, the point at which the classical approach with dimension offsets deviates from the density gradient method (Figure 3). The Vande Voorde approach fails to model the quantum mechanical effect on the charge distribution.

V. Electron Distribution

The electron distribution for the density gradient simulation and the Vande Voorde methos are shown in Figure 4. With the density gradient approach, the peak in the carrier profile moves to the cylinder center at a radius near 2 nm. This is also the radius at which the modified-dimension-classical and density gradient approaches diverged. Essentially at this radius and below, the device stops behaving like a planar surface mapped onto cylinder, and behaves more as an intriniscally two-dimensional structure.

In contrast to the density gradient result, the profile peak from the Vande Voorde approach remains at the oxide interface for all plotted radii. Additionally, there's a "∇n" singularity at the origin, as the derivative of n with respect to the radial coordinate r is non-zero in the limit of zero r. This is due to the empirical position-dependent bandgap narrowing used in the model. Also note the approximately 10^4 difference in predicted carrier density for the $r_{Si} = 0.6$ nm device; the small-radius quantum exclusion predicted by the density gradient model is neglected by the Vande Voorde model.

The substantial difference in the predicted carrier profile explains the lack of agreement in the radius scaling of the two models. This shows the unsuitability of approaches such as the one of Vande Voorde and Van Dort in modeling strongly two-dimensional structures. One could extend these methods by integrating the influence of multiple oxide interface points, but this would add complexity, and the charge distribution would still not match.

VI. Conclusion

Of the three methods considered, only the density gradient method showed itself to be suitable for true multidimensional structures. Both the modification of physical device parameters, and the use of the quasi-one-dimensional approach of Vande Voorde failed to track the density gradient result when the dimension reached a point such that the device deviated from quasi-one-dimensional behavior. Previous work has shown that multidimensional quantum effects are an important factor in the behavior of more conventional devices [6][7][8][9].

VII. Acknowledgments

Schred was acquired through the Purdue University Nanohub (`http://nanohub.purdue.edu/`). Thanks to Dan Grupp (Acorn Technologies), Bryan Biegel (NASA), Mario Ancona (Naval Research Labs), and Robert Dutton (Mixed Technology Associates) for their contribution to this project.

References

[1] A. Kranti, Rashmi, S. Haldar, and R.S. Gupta, "Design guidelines of vertical surrounding gate (VSG) MOSFETs for future ulsi circuit applications," in *2001 Topical Meeting on Silicon*

Monolithic Integrated Circuits in RF Systems. Digest of Papers, September 2001, pp. 161–165.

[2] R. Li, Y. Zhang, Y. Lu, D.S. Choi, M. Luo, and K.L. Wang, "50 nm vertical surround gate MOSFET with S-factor of 75 mv/dec," in *Device Research Conference Digest*, June 2001, pp. 63–64.

[3] M.J. van Dort, P.H. Woerlee, and A.J. Walker, "A simple model for quantisation effects in heavily-doped silicon MOSFETs at inversion conditions," *Solid-State Electronics*, , no. 3, pp. 411–414, 1994.

[4] P. Vande Voorde, P.B. Griffin, Z. Yu, S.-Y. Oh, and R.W. Dutton, "Accurate doping profile determination using TED/QM models extensible to sub-quarter micron nMOSFETs," in *1994 IEEE IEDM Technical Digest*, 1996, pp. 811–814.

[5] M.G. Ancona and G.J. Iafrate, "Quantum correction to the equation of state of an electron gas in a semiconductor," *Physical Review B*, vol. 39, no. 13, pp. 9536, 1989.

[6] D. Connelly, Z. Yu, and D. Yergeau, "Macroscopic simulation of quantum mechanical effects in 2-dimensional MOS devices via the density gradient method," *IEEE Transactions on Electron Devices*, vol. 49, no. 4, pp. *tbd*, April 2002.

[7] M.G. Ancona, "Density-gradient analysis of effects of geometry on field-emitter characteristics," in *IEEE IEDM Technical Digest*, 1992, pp. 383–386.

[8] A. Asenov and S. Kaya, "Effect of oxide interface roughness on the threshold voltage fluctuations in decanano MOSFETs with ultrathin gate oxides," in *2000 IEEE SISPAD Proceedings*, 2000, pp. 135–138.

[9] A. Asenov, G. Slavcheva, A.R. Brown, J.H. Davies, and S. Saina, "Increase in the random dopant induced threshold fluctuations and lowering in sub-100nm MOSFETs due to quantum effects : A 3-d density gradient study," *IEEE Electron Device Letters*, vol. 48, no. 4, pp. 722–729, April 2001.

[10] C.S Rafferty, Z. Yu, B. Biegel, M.G. Ancona, J. Bude, and R.W. Dutton, "Multi-dimensional quantum effect simulation using a density-gradient model and script-level programming techniques," in *1998 IEEE SISPAD Proceedings*, 1998, pp. 137–140.

[11] Avanti Corporation TCAD Business Unit, Fremont, CA, *Medici : Two Dimensional Device Simulation Program User's Manual*, 2000.2 edition, July 2000.

[12] S. Takagi, M. Takayanagi-Takagi, and A. Toriumi, "Accurate characterization of electron and hole inversion layer capacitances and its impact on low voltage operation of scaled MOSFETs," in *1998 IEEE IEDM Technical Digest*, 1998, pp. 619–622.

Daniel Connelly attended Massachusetts Institute of Technology and Stanford University. He then spent three years at Motorola in Austin, TX, before in October 2000 beginning at Acorn Technologies in Palo Alto, CA. His graduate work was on MOS devices in the Ge-Si system. Since then he's been doing design and analysis of silicon-based SOI and bulk CMOS devices.

Zhiping Yu graduated from Tsinghua University, Beijing, China, in 1967 with B.S. degree. He received his M.S. and Ph. D degrees from Stanford University, Stanford, CA, U.S.A. in 1980, and 1985, respectively.

He is presently a Senior Research Scientist at Dept. of Electrical Engineering in Stanford University, and also holds a full professorship in Tsinghua University. His research interests focus on IC process, device, and circuit simulation, and in particular, the numerical techniques and modeling of RF and heterostructure devices. He has been involved in efforts to develop a simulation package for optoelectronic devices and 3D solid modeling for ICs. His current research efforts include the development of next generation of device simulator and advanced transport models for sub-100 nm CMOS technology, including quantum mechanical effects.

Dr. Yu is a senior member of IEEE and is currently serving as the Associate Editor of IEEE Trans. CAD of IC & Systems, responsible for TCAD related field. He has published one book and more than 110 technical papers, all related to Technology CAD (TCAD).

Dan Yergeau Dan Yergeau graduated from Rose Hulman Institute of Technology in 1989 with a B.S. in Electrical Engineering and Computer Science. He received his M.S. and Ph.D. degrees from Stanford University in 1990 and 2000, respectively.

His research is concentrated on the development of a simulator supporting user specification of device and process models.