Analysis and Optimization of Distributed ESD Protection Circuits for High-Speed Mixed-Signal and RF Applications

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Abstract--Electrostatic discharge (ESD) protection devices can have an adverse effect on the performance of high-speed mixed-signal and RF circuits. This work presents a detailed s-parameter based analysis of the performance of these circuits with special attention to the *distributed* ESD protection designs. It has been shown that a 4-stage distributed ESD protection can be beneficial at frequencies greater than 3 GHz. Two generalized design optimization methodologies using coplanar waveguides are developed for the distributed structure to achieve a better impedance match over a broad frequency range. By using this optimized design, an ESD device with a parasitic capacitance of 200 fF will attenuate the RF signal power by only 0.27 dB at 10 GHz. A design strategy is also suggested for high-speed mixed-signal ICs.

I. Introduction

As the demand for wireless (RF) and high-speed mixed-signal systems continues to increase rapidly, providing sufficient ESD protection for these systems poses a major design and reliability challenge. This is due to the fact that in applying ESD protection to these systems, the protection system must be transparent--the protection circuit must not affect the signal under normal operating conditions [1, 2]. The on-chip protection circuit is placed between the signal pin and the core circuit, as shown in Figure 1. The protection circuit may be composed of various devices, such as diodes, transistors, or silicon controlled rectifiers (SCRs), but in all cases, these devices shunt ESD current coming from the signal pin to the power supply rails and away from the core circuit [3]. However, under normal operating conditions, these protection devices present capacitances and resistances to the signal path, and at sufficiently high frequencies, the capacitances look like short circuits to ground. Thus a poorly designed protection system can generate impedance mismatches, causing reflections of signals, corruption of signal integrity, and inefficient power transfer between the signal pin and the core circuit. In addition to these problems, both the incident and the reflected signals can interfere with signals on adjacent wires through crosstalk. Also, while the operating

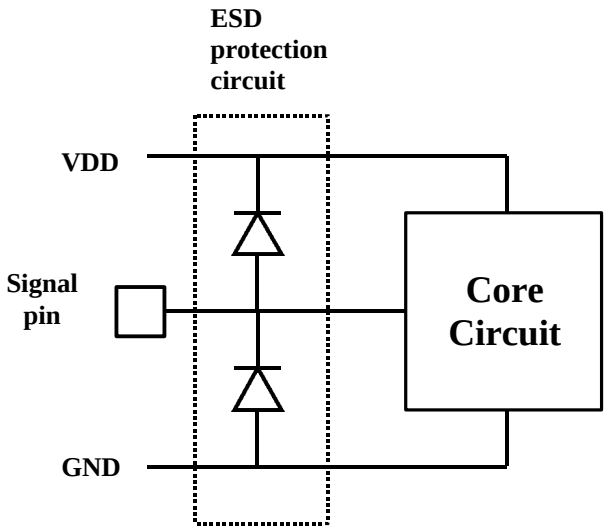

Figure 1. A simple ESD protection system example. The diodes shunt excess current applied to the signal pin towards VDD or GND to protect the core circuit.

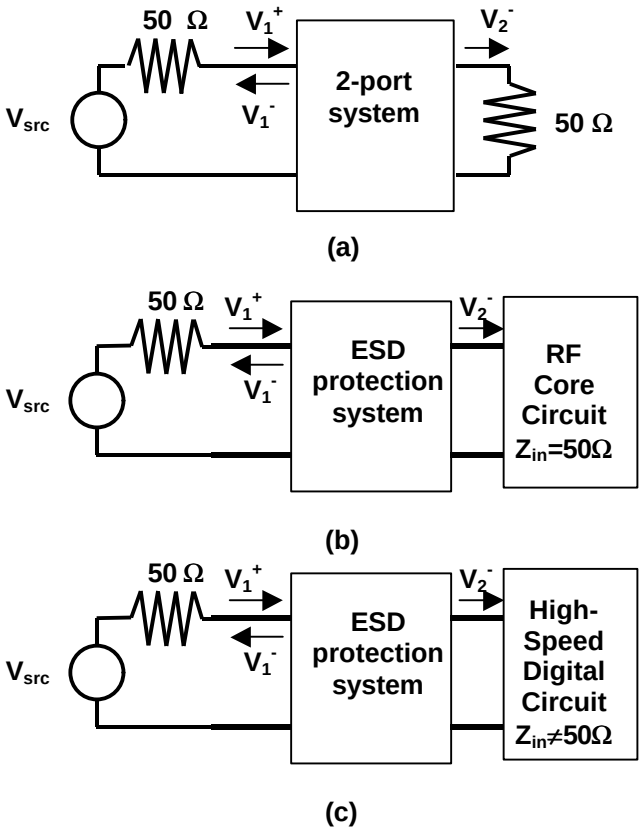

Figure 2. (a) General 50 Ω 2-port system showing the incident, reflected and transmitted voltages. The 50 Ω voltage source (V_{src}) drives the system, and after passing through the 2-port system, power is transferred to the 50 Ω load at the right.
(b) 2-port model of an RF system with an ESD protection system. Note the analogy between (a) and (b).
(c) With a high-speed digital circuit as the load, the impedance of the load is no longer at 50 Ω, and the situation differs from that of (a) and (b).

frequency continues to rise, the size of the protection circuits and their associated capacitances are not decreasing as rapidly, resulting in increasingly inefficient power transfer. The simple approach of minimizing capacitance while maintaining high protection levels is becoming increasingly infeasible as the operating frequency rises beyond a few GHz [4]; alternate protection schemes such as the distributed transmission line ESD protection system may be necessary [5, 6]. Recent work has focused on comparison of ESD protection strategies for RF applications at 2 GHz [7]. However there is little published information that provides performance analysis of RF circuits with various ESD protection design options, particularly of the distributed protection scheme, which is attractive for operations in the multi-GHz regime [8]. In this paper, we introduce two design methodologies to quantify the impact of the parasitic capacitance and resistance associated with various distributed ESD protection circuit designs and to optimize the number and length of coplanar waveguides (CPW) separating the distributed ESD elements. Also, it is demonstrated that a 4-stage distributed ESD protection with coplanar waveguides can be employed to provide excellent RF performance for frequencies as high as 10 GHz.

II. Distributed ESD Protection System

As the operation frequency of systems rise, the parasitics associated with ESD protection systems become more significant in limiting bandwidth and power transfer. One method in minimizing the effects of these parasitics is to utilize a distributed protection scheme. A distributed ESD protection system is a modification of the distributed amplifier proposed by Ginzton [9], where ESD protection devices replace the amplifier elements. As proposed in [6], and as shown in Figure 3c and 3d, by incorporating the parasitic capacitance of the device into a discrete transmission line structure, the loading of the system by the ESD devices may be prevented.

In [6], ESD analysis of such a configuration was performed, whereby it was shown that each element of the distributed protection scheme does indeed turn on under HBM and CDM stress, but the impact of the protection scheme on the RF signal under normal operation was not quantified. The following sections show the effect of such ESD protection on high-speed signals and propose a methodology in designing distributed ESD protection systems to minimize their effects on the integrity of high-speed signals.

III. S-Parameter Performance Analysis

In RF systems, the s-parameter matrix is often used to represent the characteristics of the network. As the system operating frequency increases such that the wavelength becomes comparable to the device dimensions, the wave-nature of signal propagation cannot be ignored. Also, generating pure open and short loads to calibrate the network measurement equipment becomes increasingly difficult at higher frequencies, as small parasitics greatly affect the impedances. The s-parameter

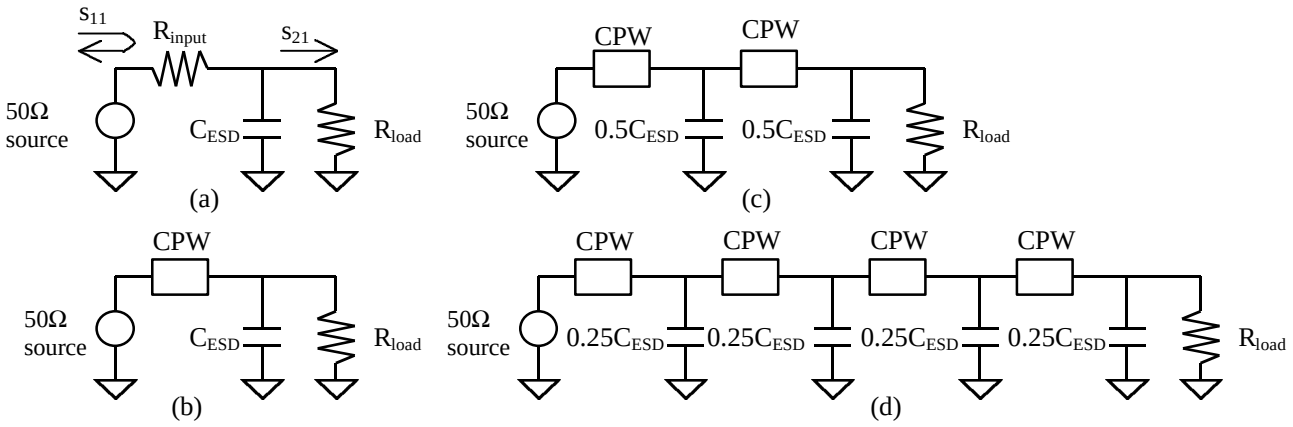

Figure 3. (a) Equivalent circuit with a general ESD protection device between the source and the load. (b) A length of CPW is added to the previous circuit, to improve impedance matching. (c) Two-section transmission line structure formed by CPW and the protection devices. (d) Four-section transmission line structure.

matrix, which consists of ratios of outgoing to incoming signals measured with resistive terminations at each network port, satisfies the requirements for accurate high-frequency characterization [10]. Most often, RF networks are standardized to 50 Ω input and output impedances for maximum power transfer. S-parameter measurements are then taken as the reflection at, and transmission between ports with 50 Ω termination at each port.

Figure 2a shows the measurements required for a general 2-port system. When a voltage is applied from a 50 Ω source, the ratio of the reflected signal to the incident signal is the input reflection s-parameter, s_{11}, which is also equal to the reflection coefficient Γ as shown in equation (1).

$$s_{11} = \frac{V_1^-}{V_1^+} = \Gamma \qquad (1)$$

$$s_{21} = \frac{V_2^-}{V_1^+} \qquad (2)$$

The forward transmission s-parameter, s_{21}, is the ratio of the outgoing signal at port 2 to the incident signal at port 1 as shown in equation (2). These two parameters characterize how much signal is reflected by the system, and how much signal is transmitted to the 50 Ω load.

A generalized RF system with an ESD protection network is shown in Figure 2b. S-parameters may be used to quantify the impact of the ESD protection system on the signal transmission between the input and the core circuit. The s_{11} of the ESD protection system shows how much signal is reflected back to the input, and s_{21} shows how much of the signal applied at the input reaches the core circuit. Thus the goal of the ESD protection circuit is to protect the core circuit while minimizing s_{11} and maximizing s_{21} of the system.

Since both the input and output impedances are standardized to 50 Ω in RF circuits, an analogous situation exists for ESD protection at the RF outputs. However, digital systems do not have standardized input and output impedances as shown in Figure 2c, therefore modifications will be necessary in analyzing high-speed digital circuits, and this will be discussed in section V.

Starting with a standard 50 Ω system as is commonly found in RF systems, four different implementations of ESD protection are investigated, as shown in Figure 3. A 50 Ω signal source drives the input to the protection circuit, and the output of the protection circuit is connected to the system to be protected, as modeled by a 50 Ω load (R_{load}). In each circuit, the protection device is modeled as a capacitance and input resistance, and interconnects between the pin and ESD circuit or between distributed ESD elements are modeled by a resistance or a CPW. Initially, the capacitance is assumed to be 200 fF, a value sufficient to provide a 2 kV ESD protection level [1]. Figure 3a, which represents the most general ESD protection, consists of the source, load, a resistor representing interconnect and device loss (R_{input}), and the protection device and pad parasitic capacitance (C_{ESD}). Figure 3b introduces a CPW between the source and the protection device to provide a better impedance match. The required CPW length was calculated using Smith Charts and

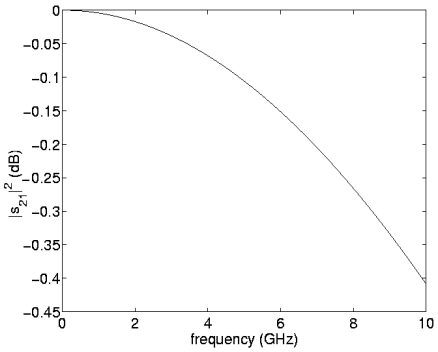

Figure 4. Plot of signal power loss vs. frequency for the circuit in Figure 3a, with an ESD device capacitance of 200 fF and R_{input} of zero.

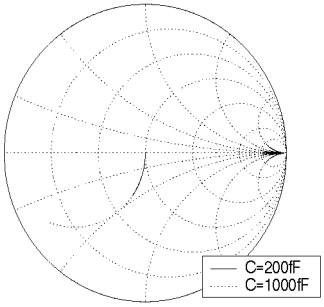

Figure 5. Smith Chart representation of the effect of C_{ESD} on s_{11} for Figure 3a, with zero series resistance (R_{input}=0).

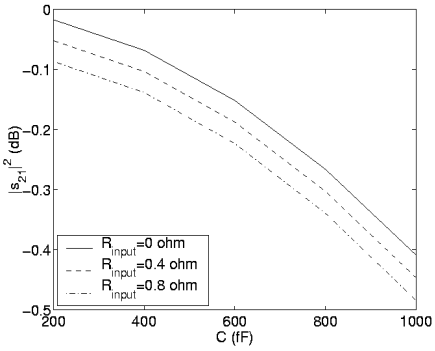

Figure 6. Performance vs. capacitance with varying R_{input}. Note the increase in loss with increased resistance.

impedance transformations to minimize reflections. This methodology is discussed in detail in Section VI. Figures 3c and 3d show series circuits with smaller sections for better broadband match as the circuit approaches an ideal transmission line made of infinitesimal sections. For the purpose of this study, transmission lines with a maximum of four sections were examined. Although more sections may yield better performance, any further gain would be marginal. Also, the added complexity of having more sections may be undesirable, and depending on the layout topology, it may be unreasonable to further divide the ESD device and pad capacitances into smaller elements. S-parameter simulations over the frequency range 0-10 GHz are performed on these circuits using the microwave circuit simulator ADS [11], to generate the reflection parameter s_{11}, and the transmission parameter s_{21}. As shown in Figure 3a, s_{11} corresponds to the amount of signal that is reflected at the input, and s_{21} corresponds to the amount of input signal that reaches the load. The objective of the system designer is to minimize s_{11} and maximize s_{21}. This study uses $|s_{11}|^2$ and $|s_{21}|^2$ as performance metrics since these coefficients are then directly proportional to power.

Next, the simulations are repeated for a set of capacitances, thus modeling different protection devices with different protection levels. The data from these simulations can be used to provide designers with insight into how much complexity is required in the protection system to obtain the desired ESD protection along with sufficient high-speed performance at the operating frequency of interest.

IV. Results & Discussion

Figure 4 shows the results from the simulation of the simplest case from Figure 3a, with the input resistance set to zero and C_{ESD}=200 fF. Since the whole system is lossless, all the power loss is due to signal reflection caused by impedance mismatch. While most of the power reaches the load at low frequencies, the capacitance loads the circuit at higher frequencies. Using a larger protection device in the same circuit gives s_{11} like that in Figure 5. It can be observed that the magnitude of

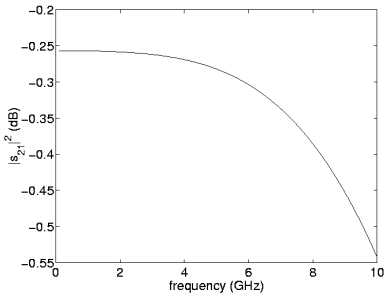

Figure 7. Plot of signal power loss vs. frequency for Figure 3b, with C_{ESD}=200 fF.

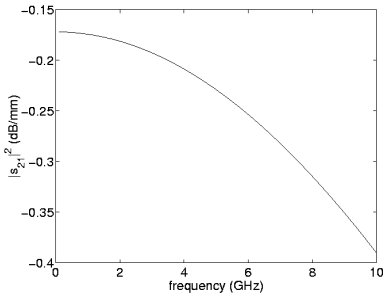

Figure 8. CPW loss per mm vs. frequency, showing the inherent loss found in the CPW due to resistive and dielectric loss.

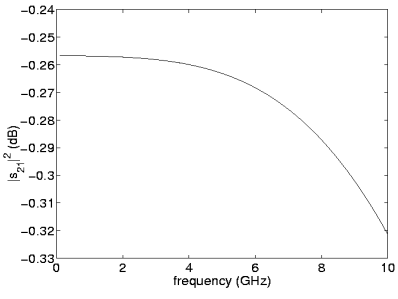

Figure 9. Plot of signal power loss vs. frequency for Figure 3c, with C_{ESD}=200 fF. Note the better loss characteristics compared to Figure 7.

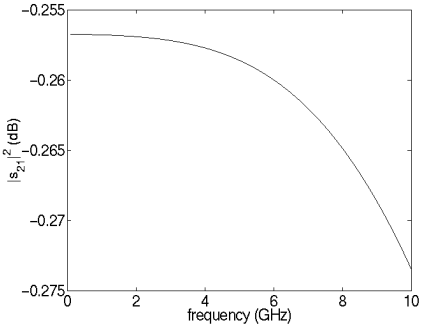

Figure 10. Plot of signal power loss vs. frequency for Figure 3d, with C_{ESD}=200 fF. The loss is now less than 0.275 dB at 10GHz.

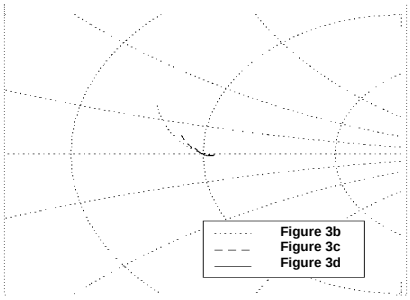

Figure 11. Smith Chart representation of s_{11} for Figures 3b, 3c, and 3d, over the frequency range 0-10 GHz, with C_{ESD}=200 fF. The reflection decreases with increasing number of sections.

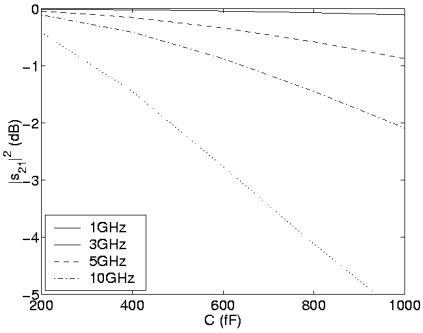

Figure 12. Signal power loss vs. parasitic capacitance, for a set of frequencies for the circuit in Figure 3a.

the reflection becomes large, thus little power is delivered to the load. Also, with increasing input resistance, the loss increases, as shown in Figure 6.

The effect of employing CPWs in the ESD protection is also examined. Figure 7 corresponds to the circuit in Figure 3b, where the CPW is added to provide some impedance match. In this case, the loss is due to the CPW loss and the mismatch loss. With a CPW length of 1.3 mm, there is a 0.25 dB loss even at low frequencies. As shown in Figure 8, this CPW has a loss of 0.18 dB/mm at low frequencies, with the loss becoming worse with increased frequency, to 0.39 dB/mm at 10 GHz. At higher frequencies, this CPW loss worsens, while the mismatch loss also becomes larger. Comparatively, this result is worse than that of Figure 4, but since Figure 4 shows an ideal case where there is no resistive loss at all, this is to be expected. Note that if the CPW were lossless, the results with the CPW would be better than that of Figure 4.

Figures 9 and 10 show the results from simulating the circuit in Figures 3c and 3d, respectively. The losses observed are less than those seen in both Figures 4 and 7 at higher frequencies. At low frequencies, the CPW losses are again observed. Figure 10 shows loss characteristics that decrease by less than 0.02 dB between 0 and 10 GHz, with the maximum loss of 0.273 dB at 10 GHz, thus demonstrating good broadband characteristics.

Figure 11 shows the reflection parameter s_{11} corresponding to Figures 3b, 3c, and 3d. Note that the reflection observed becomes smaller with increased number of CPW sections.

The impact of the protection level is analyzed next by varying the size of the protection device (C_{ESD}). Figures 12-15 plot the power loss as represented by $|s_{21}|^2$ in the protection systems in Figure 3, against the parasitic capacitance posed by the protection devices. It is clear that higher frequencies and larger capacitances generate larger

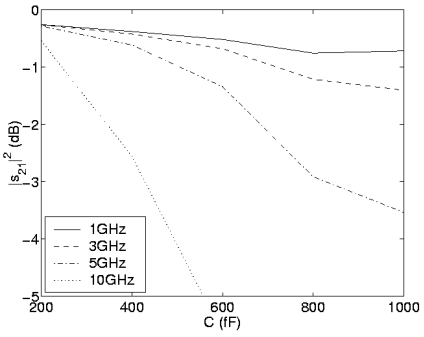

Figure 13. Performance vs. capacitance plot for the circuit in Figure 3b.

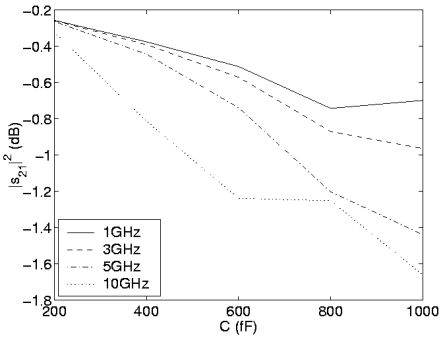

Figure 14. Performance vs. capacitance plot for the circuit in Figure 3c. Note that the curves start to converge for all frequencies.

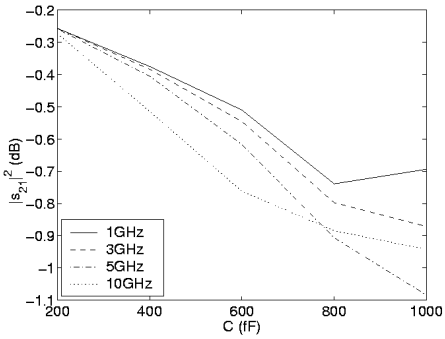

Figure 15. Performance vs. capacitance plot for the circuit in Figure 3d. Note that the variation of the loss over all measured frequencies and capacitances is only 0.85 dB.

losses. The ideal case (R_{input}=0) in Figure 12 shows that at low frequencies, the loss is minimal irrespective of the device capacitance. The single CPW case of Figure 13 shows resistive loss in the CPW, resulting in poor performance at all frequencies. However, a more distributed protection system can minimize the loss for a wider frequency range, as shown in Figures 14 and 15. Also, Figure 15, which represents the four-segment distributed protection, shows that the loss will only vary by 0.85 dB for all capacitances, thus showing immunity to variations in ESD device depletion capacitance due to changes in DC bias levels.

The above results indeed show that dividing the ESD protection device into a few smaller sections provides better broadband RF performance. But for high-speed digital systems, there are differences in the circuit characteristics that prevent the use of s-parameter analysis. These differences are addressed, and a solution towards designing effective distributed ESD systems, even in a high-speed digital environment, is proposed in the next section.

V. Modifications for Applications to High-Speed Digital Circuits

In the case of high-speed digital circuits, the impedance termination conditions are not as well defined as in the RF case. Input buffers present a capacitive load due to the gate capacitance of the devices, and output buffers present a capacitance due to the drain junction capacitance in parallel with the on-resistance (R_{on}) of the conducting device. These terminal impedances vary depending on the buffer sizes, and therefore transmission and reflection from a transmission line would also be variable.

In order to facilitate the design of the distributed ESD protection system, we propose terminating these digital terminals resistively, as suggested in [12]. By applying a 50 Ω termination resistor for the input buffer as shown in Figure 16a, and for the output buffer as shown in Figure 16b, s-parameter analysis may then be performed on these digital circuits as well. The capacitances presented by the buffer transistors themselves may be absorbed into the ESD protection system capacitance for design purposes.

In addition to allowing s-parameter analysis, application of termination resistances prevents intersymbol interference (ISI) by not generating any reflections at the terminals. Also, crosstalk that generates reverse-traveling noise will no longer affect the forward-traveling signal because of proper termination at the terminals. The price that is paid for these benefits is additional die area, and perhaps an increase in power consumption.

With 50 Ω terminations both in RF and high-speed digital systems, effective signal transmission may be achieved by applying a distributed ESD protection system. Thus the next section will demonstrate methodologies in designing distributed ESD protection systems.

VI. Design Methodologies for Optimized Distributed ESD Protection

Prior to determining the proper CPW characteristics, three parameters must be fixed. They are the maximum operating frequency f_{max}, the equivalent ESD capacitance C_{ESD}, and the CPW

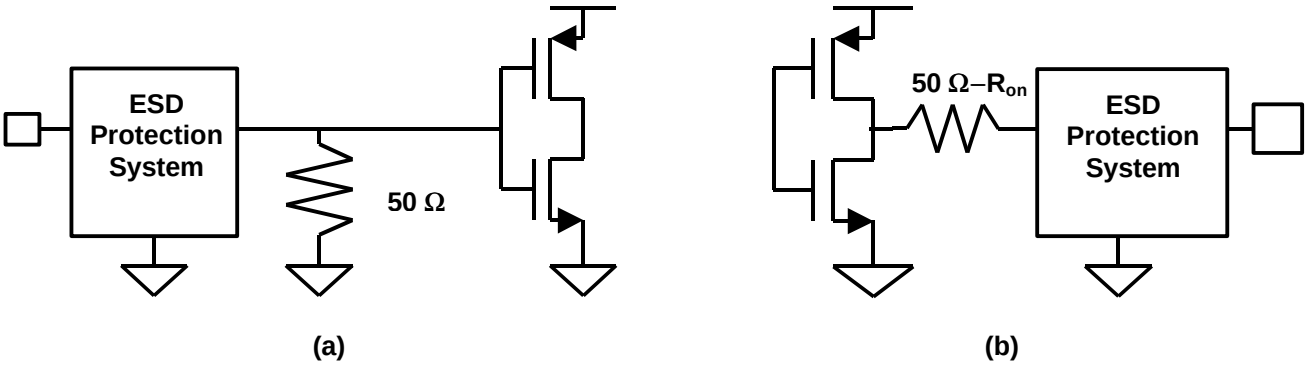

Figure 16. (a) Modified high-speed digital input buffer with a 50 Ω parallel resistive termination to prevent reflections. (b) Output buffer with a series resistive termination. Note that the series termination resistor would be less than 50 Ω depending on R_{on}, but since R_{on} should be small for a well-designed device, 50 Ω is a good approximation for the termination resistance.

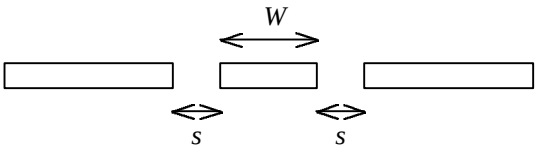

Figure 17. Cross-section of a coplanar waveguide. The lines are configured ground-signal-ground, with the key dimensions being the line width *W* and the spacing *s*.

characteristic impedance Z_{CPW}. Selecting f_{max} should consist only of determining the maximum frequency specification for the core circuit. C_{ESD} should be calculated after determining the proper ESD device size required for a particular protection level in a given technology. The equivalent capacitance may then be calculated from the device junction areas, or obtained through simulations.

The appropriate dimensions for the CPW as shown in Figure 17 must then be determined. The minimum width (*W*) must be such that given a line thickness, which is technology dependent, the maximum possible ESD current can flow without causing open circuit failure of the line. The calculation for this width is shown in [13].

Once the CPW signal line width is defined, the signal-to-ground spacings (*s*) of the CPW need to be determined from the desired characteristic impedance. In general, high characteristic impedance is desirable to minimize the required CPW length, but losses, which tend to be higher for higher impedance lines, need to be minimized. The exact relationship between *W*, *s*, Z_{CPW}, and loss is a complex one that is beyond the scope of this study. In this work, it is assumed that a high characteristic impedance CPW line with loss as shown in Figure 8 is available.

For the following example, f_{max} was set at 10 GHz, C_{ESD} was chosen to be 200 fF for a 2 kV protection level [1], and Z_{CPW} was chosen to be 100 Ω, a high-impedance, low-loss line according to [14]. Along with calculating the CPW length, the number of distributed sections to be created is also determined. The equivalent circuit used to achieve this is shown in Figure 18. First, factors of the ESD capacitance are determined (in this case, 200 fF, 100 fF, 67 fF, 50 fF, 40 fF...) and are represented in the circuit as C. Then Z_1 is determined for each capacitance at f_{max}, and R is the 50 Ω load resistance. These impedances correspond to points on arc A on the Smith Charts (Figures 19 & 20). From the impedance Z_1, the reflection coefficient G_1 is calculated using the formula given by (3).

$$\Gamma_1 = \frac{Z_1 - Z_{CPW}}{Z_1 + Z_{CPW}} \qquad (3)$$

Gamma, like s_{11}, represents the coordinate on the Smith Chart planes in Figures 19 & 20, with the center as the origin, and the outside circle being unity. Converting G_1 into polar coordinates gives the magnitude r and phase f. By adding some length of CPW, we attempt to bring the phase to 180 degrees (point B). For a CPW with characteristic impedance of Z_{CPW}, the locus that

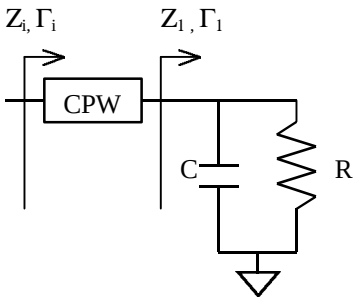

Figure 18. Circuit diagram for the example calculation in Section VI. *R*=50 Ω and f=10 GHz. The values of C and lengths of CPW vary. The impedances (Z) and reflection coefficients (*G*) are used to calculate the optimal C, CPW length, and number of distributed sections.

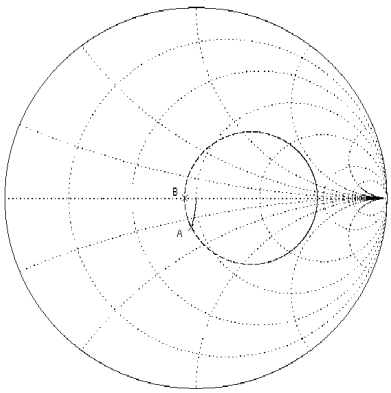

Figure 19. 50 Ω-normalized Smith Chart. Point A shows G_1 for 200 fF at 10 GHz. Point B shows G_i. The dotted circle shows the locus for different lengths of CPW.

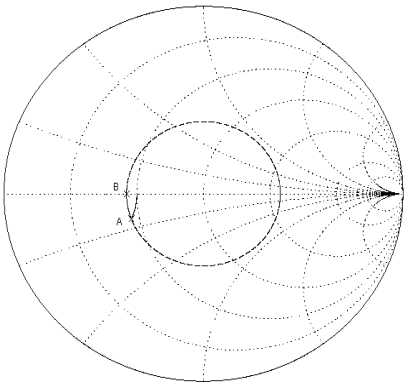

Figure 20. 100 Ω-normalized Smith Chart. Point A shows G_1 for 200 fF at 10 GHz. Point B shows G_i. The dotted circle shows the locus for different lengths of CPW.

results from adding CPW to Z_1 is a circle centered about the origin in Figure 20 (the dotted circle). Note that when this is viewed on a Smith Chart normalized to 50 Ω, the circle is not centered at the origin (Figure 19). Since a full circle around requires a CPW which is a half-wavelength ($l/2$), the correct CPW length can be calculated from equation (4).

$$\text{CPW length} = \frac{(f-p)}{2p}\frac{l}{2} \tag{4}$$

Adding the correct CPW length should yield G_i with magnitude $r_i=r$ and f_i=180 degrees. This can then be transformed into impedance with equation (5).

$$Z_i = \frac{(1+\Gamma_i)}{(1-\Gamma_i)} Z_{CPW} \tag{5}$$

As a measure of how close Z_i comes to the system impedance (Z_o) of 50 Ω, the standing wave ratio (SWR) can be calculated, as shown in equation (6).

$$SWR = \frac{1+\left|\frac{Z_i - Z_o}{Z_i + Z_o}\right|}{1-\left|\frac{Z_i - Z_o}{Z_i + Z_o}\right|} \tag{6}$$

A Z_i of 50 Ω results in an SWR of unity, and the closer the SWR is to unity, the better the match that is obtained. All the values calculated for this example are summarized in Table 1.

Now given the ESD capacitance and the maximum allowable SWR, the number of sections required to achieve those specifications can be readily calculated using the methodology above. Note that this is valid because R=50 Ω, and we try to bring Z_i to 50 Ω for each section. Thus the next section to be added can regard Z_i of the present section as just a 50 Ω load.

One last consideration is to determine whether this analysis, performed for a system operating at f_{max}, is valid when the system operates at a frequency lower than f_{max}. It can be shown that at a lower frequency, the capacitance has a larger impedance, thus the arc on the Smith Chart becomes smaller, and r decreases, resulting in a smaller SWR. Thus the f_{max} case is the worst case, and if the performance there is satisfactory, then the performance at any lower frequency will be at least as good as that seen at f_{max}.

While the above methodology relies on some geometrical concepts regarding the Smith Chart, there is an alternate, more mathematical methodology by which the same results may be obtained. This methodology uses ABCD-matrices, which, like the s-parameter matrix, is a matrix set that describes the characteristics of a 2-port network. The ABCD-matrix has the characteristics that when multiple 2-port networks are cascaded, the system response is characterized by the product of the ABCD-matrices of the component 2-port networks. This property of ABCD-matrices will be used to calculate the correct CPW length. The general form of the ABCD-matrix for a transmission line with characteristic impedance Z_{o1} and length l, and for a shunt impedance Z, are shown in equations (7) and (8), respectively.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\frac{2p}{l}l & j\frac{Z_{o1}}{Z_o}\sin\frac{2p}{l}l \\ j\frac{Z_o}{Z_{o1}}\sin\frac{2p}{l}l & \cos\frac{2p}{l}l \end{bmatrix} \tag{7}$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{Z_o}{Z} & 1 \end{bmatrix} \tag{8}$$

In our example, the system impedance Z_o is 50 Ω, while Z_{o1} is 100 Ω. Looking again at Figure 18, the cascading of the CPW with the shunt impedance Z_1 gives the ABCD-matrices for the system as shown in equation (9).

Table 1. Summary of results from the example case. Note that with increased sections, Z_i and SWR approach 50 Ω and 1.00, respectively.

C (fF)	# sections	Z_1	Γ_1	ρ	ϕ	Length (rad)	Z_i	SWR
200	1	35.85-22.52j	-0.43-0.24j	0.494	-2.64	0.502	33.9	1.48
100	2	45.51-14.30j	-0.36-0.13j	0.385	-2.79	0.355	44.4	1.13
67	3	47.88-10.88j	-0.35-0.092j	0.358	-2.88	0.259	47.3	1.06
50	4	48.80-7.66j	-0.34-0.069j	0.348	-2.94	0.200	48.4	1.03
40	5	49.22-6.19j	-0.39-0.056j	0.343	-2.98	0.163	49.0	1.02

$$\begin{bmatrix} A_i & B_i \\ C_i & D_i \end{bmatrix} = \begin{bmatrix} \cos\frac{2p}{l}l & j2\sin\frac{2p}{l}l \\ j0.5\sin\frac{2p}{l}l & \cos\frac{2p}{l}l \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 50\left(\frac{1}{R} + jwC\right) & 1 \end{bmatrix} \quad (9)$$

The product of the ABCD-matrix for the CPW and for the parallel RC combination gives the system response. From the product, the input impedance Z_i may be calculated by taking A_i/C_i of the matrix. By setting the imaginary component of this impedance to zero, since we desire the impedance to be a resistance close to 50 Ω, the CPW length may be calculated to be as shown in equation (10).

$$\frac{l}{l} = \frac{1}{4p}\tan^{-1}\frac{2wC}{\frac{Z_{o1}}{Z_o^2} + Z_{o1}(wC)^2 + \frac{1}{Z_{o1}}} \quad (10)$$

Using this length, the input resistance may be shown to be as shown in equation (11).

$$R_i = \cos^2\left(\frac{2p}{l}l\right) + \left(\frac{Z_o}{Z_{o1}}\sin\left(\frac{2p}{l}l\right) + wCZ_o\cos\left(\frac{2p}{l}l\right)\right)^2 \quad (11)$$

Repeating the calculations for the different capacitances, this method yields the same result as that of the Smith Chart method, identical to Table 1.

VII. Conclusion

In conclusion, detailed s-parameter analysis of RF circuits with different ESD protection design options has been presented. The effect of the interconnect and device losses, together with the parasitic device capacitances on RF performance has been quantified. Terminations schemes for high-speed digital circuits have also been proposed to allow this analysis to be applicable for high-speed digital and mixed-signal systems. It has been shown that a 4-stage distributed ESD protection can be beneficial at frequencies greater than 3 GHz. Two generalized design methodologies have been developed to optimize the number and length of coplanar waveguides separating the distributed ESD elements. By using these methodologies, an ESD protection scheme with a parasitic capacitance of 200 fF will attenuate the signal power by only 0.27 dB at 10 GHz.

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