Performance Improvement in Larger RF LDMOSFET Power Amplifiers

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Abstract **While larger transistors are used to deliver more power in RF transmitter power amplifiers, it has been observed that the performance per unit gate width decreases with increasing width. In this work, a major cause of this performance degradation in RF LDMOSFET power amplifiers is identified as the mutual inductance in the system, and a field solver and circuit simulator are used to quantify the mutual inductance. Circuit simulations show that the characteristics of devices with larger widths may be mimicked by models of smaller devices with increasingly larger inductances added to the terminals. In order to prevent the performance degradation caused by the mutual inductance, the use of baluns is proposed to apply phase-inverted signals to adjacent cells within the power amplifier device. Simulations comparing systems with and without baluns show that using baluns allows recovery of performance that is otherwise lost due to source degeneration caused by mutual inductance, as seen by the 7.8W output power with baluns as compared to 5.2W without for a W=64mm device at 900MHz.**

1. Introduction

The proliferation of wireless communications systems worldwide has increased the demand for better performance in these systems. The power amplifier subsystem consumes a large amount of the available power, and improving its efficiency should significantly improve the performance of the overall system. Currently, the method by which more output power is derived from RF LDMOSFET power amplifier devices consists of using devices with larger channel widths (W). However, previous work has shown that with increasing W, the RF performance per unit device width decreases [1]. This decrease has been quantified in the form of decreasing maximum output power for constant input power per unit width as shown in Figure 1. It shows measurement results of Hitachi L4B LDMOSFET transistors operating at f=900MHz, Pin=7dBm/mm, Vg=1.2V, and Vd=3.5V. Here, the width-related effects can be observed, as at 64mm, proper scaling should yield an output power of 8W, while only 3W is obtained.

Practically, higher performance have been extracted from larger power amplifier systems through the use of equal phase, equal amplitude power dividers/combiners as suggested by Wilkinson [2]. A similar divider/combiner system was implemented with LDMOSFETs in [1]. However, previous work has not clearly identified the mechanism behind the width-related performance degradation. Thus the goals of this work are to identify the cause of width-related performance degradation in RF power amplifier devices through measurements and simulations, and to develop remedies to counter this degradation.

2. RF Measurements and Simulations

Investigation in the small-signal RF regime utilized Root MOSFET models that were extracted using the HP85124A Pulsed Modeling System from Agilent Technologies [3, 4, 5]. For this work, models were generated for the Hitachi L4B LDMOS devices [6, 7] at three gate widths (4mm, 8mm, and 16mm), with 1, 2, and 4 unit cells placed in parallel, respectively.

If the parallel fingers and unit cells have no interaction between them, they should all act identically, and the system should scale with width. But interaction in the form of inductive coupling exists in both the bondwires and the fingers, and must be considered. As RF current runs through the gate and drain bondwires, and through the gate, drain, and source fingers, magnetic fields are generated, which affect current flow in other parts of the device. This magnetic coupling is quantified as mutual inductance, and is a function of the conductor length (l), and separation (d), as shown in equation (1).

$$M = \frac{\mu_o l}{2\pi}\left(\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right) \quad (1)$$

After extracting the bondwire structure at the gate and drain terminals from SEM photos shown in Figure 2 using the software of [8], the field solver FASTHENRY was used to estimate the mutual inductances between bondwires at 900 MHz [9]. But when this method is applied to the fingers on-chip, the distributed nature of the device prevents our determining the exact current paths within the device, thus the FASTHENRY output was not expected to yield exact inductance values for the fingers, but rather only a rough estimate of the mutual inductance values.

The circuit simulator Advanced Design System (ADS) [10] from Agilent was then used to see if the extra inductance generates the observed changes in s-parameters. The Root model for a 4mm device was entered into ADS, along with the FASTHENRY results to see whether the s-parameters for the larger devices can be replicated by simulating the 4mm unit cell with external mutual inductances. The mutual inductance values were then optimized so that the 4mm simulation results agreed with s-parameter measurements for devices with widths of 8mm, 16mm, 36mm, and 64mm.

The devices were biased at a gate voltage of 1.2V, and a drain voltage of 3.5V. Figures 3 and 4 show the results of the s-parameter simulations between 0.5GHz and 4.5GHz, and Table 1 shows the extra inductance values required by the 4mm model to simulate the performance of the larger devices. It can be seen that increasing the terminal inductances allows the 4mm device model to mimic the degradation caused by placing more unit cells in parallel. The s-parameter results for the W=16mm and 36mm devices show similar agreements, but are not shown due to space limitations.

Then, using the 4mm Root model with the extra inductance values, large-signal load-pull simulations were performed in ADS to see what degradation in maximum output power may be observed. The conditions were set the same as for the measurements. The maximum output power plot of Figure 5 shows that the simulation results show a sub-linear increase in output power. It can be seen that at W=64mm, a linear increase in output power should yield 8W, but the simulation with inductance shows only 5.2W. This result shows the same trend as that from experimentally measured results shown in Figure 1, although the saturation in output power is not as severe in the models. This discrepancy is likely due to some layout-dependent resistive and capacitive effects, as seen in the decrease in low-frequency $|s_{21}|$ with increased W (Figure 3 vs. Figure 4). It should also be noted here that while mutual inductance appears at the gate, drain, and source terminals of the device, the extra inductance at the source terminal affects the performance most severely, as this impedance acts as a series feedback, degeneration impedance.

It was thus shown that adding external inductances modeling the mutual inductance yields small-signal s-parameters and large-signal load-pull simulation results that mimic measurements, providing further evidence that mutual inductance between cells causes significant decrease in RF LDMOSFET performance.

3. Using Baluns to Prevent Performance Degradation

In order to prevent performance degradation, the effect of mutual inductance between unit cells must be minimized. One such solution would require the use of baluns at the gate and drain to split and combine signals that have opposite phases, as shown in Figure 6. By feeding inverted signals in alternate unit cells, the largest mutual inductance component, generated by the closest unit cell, now has a negative effect, thus decreasing the inductance at the terminals. By generating negative mutual inductance, the degeneration at the source terminal may be prevented. Also, by having baluns at both the input and output, the signals at the output would be in-phase again.

Starting with the mutual inductance values in Table 1, and applying them to the circuit shown in Figure 6, simulations in ADS were performed. In addition to the circuit seen in Figure 6, larger devices were simulated by placing more 4 mm unit cells in parallel, with alternating connections to the in-phase or inverted signals.

Figure 7 shows the results from the devices (W=8, 16, 32 and 64mm) with baluns at the input and output. For these simulations, Vg=1.2V, Vd=3.5V, and the frequency ranged between 0.6GHz and 3.0GHz. With the baluns, all the curves in Figure 7 lie on top of one another, indicating that the baluns cancel the mutual components, and proper scaling is observed. It can be seen that the transmission parameters do not degrade for larger W.

Using the same devices at the same biases, load-pull simulations were run in ADS at 900MHz. The results are summarized in the form of a maximum output plot in Figure 8. It can be seen that the devices with baluns have output powers roughly proportional to W, while the curve for the devices without baluns, as already shown in Figure 5, shows output powers that increase sub-linearly. Now the output power at W=64mm approaches 8W, as expected from the linear scaling of Figures 1 and 5. These simulations thus show that baluns may be used at the input and output to cancel the mutual inductance from the nearest neighbor cell and recover RF performance that would otherwise be lost.

4. Conclusion

Measurements and simulations were performed to determine that the width-related performance degradation observed for RF LDMOS power amplifier devices correlates well with the effects of mutual inductance. By placing additional device fingers in parallel to increase output power, the magnetic coupling arises between the fingers, impeding current flow. The mutual inductance appearing at the source terminal of the device affects the performance most severely, and causes the sub-linear increase in output power for increasing device width to the extent that simulated output power at 900MHz drops from an expected 8W to 5.2W for W=64mm. Suggestions to prevent this degradation were made, and it was shown through simulation that by adding baluns to the input and output of the devices and feeding inverted signals to alternating unit cells, the effects of mutual inductance may be canceled, and the output power restored.

References

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W (mm)	Mg (nH)	Md (nH)	Ms (pH)
4	0	0	0
8	1.2	1.4	50
16	3.4	3.9	200
36	3.4	3.3	500
64	3.4	4.3	700

Table 1. Through s-parameter simulations, values of mutual inductance at the gate (Mg), drain (Md), and source (Ms) terminals were determined for each 4mm section of a device. As W increases and the number of parallel units increase, the mutual inductance tends to increase.

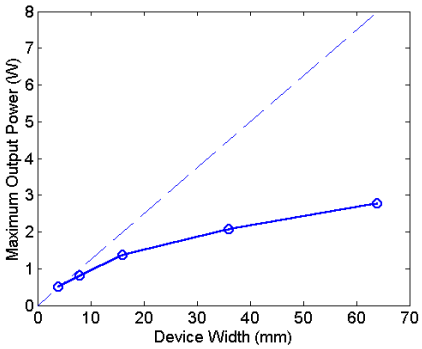
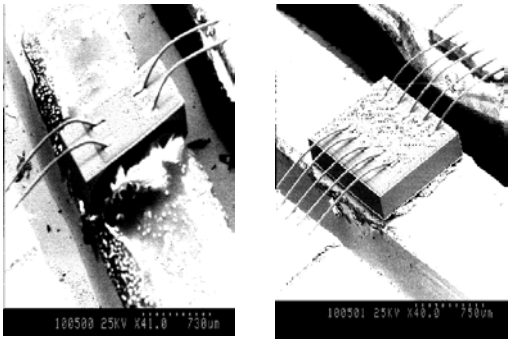
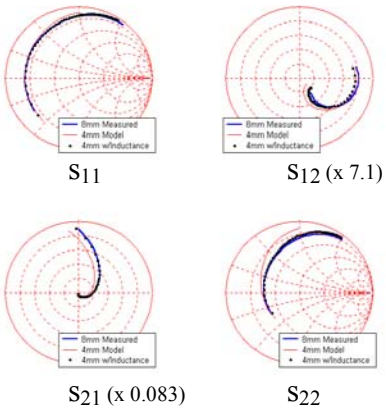


Figure 1. Measured maximum output power vs. device width for L4B MOSFETs at P_{in}=7dBm/mm, f=900MHz, Vg=1.2V, and Vd=3.5V. The measured output power deviates further away from the ideal linear relationship (dotted line) as W increases. At 64mm, while the ideal output would be around 8W, the measured output is only 3W.



(a) (b)

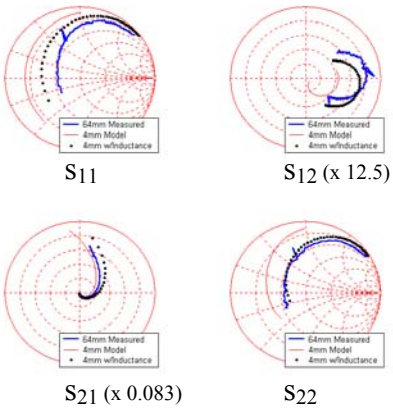
Figure 2. (a) SEM photo of a device with W=8mm. The bondwire geometry is used to extract the inductance values. (b) SEM photo of a W=36mm device. The 5-wire structure should give more mutual inductance.



S_{11} S_{12} (x 7.1)

S_{21} (x 0.083) S_{22}

Figure 3. Comparisons between the 4mm Root model, the Root model with inductances from Table 1, and measured data for W=8mm. The s-parameter simulations were performed at Vg=1.2V, Vd=3.5V, and f=0.5-4.5GHz. Note that the added inductance makes the 4mm model perform like a W=8mm device.



S_{11} S_{12} (x 12.5)

S_{21} (x 0.083) S_{22}

Figure 4. Comparisons between the 4 mm Root model, the Root model with extra inductance, and measured data for W=64mm under the same conditions as for Figure 3. The inductance causes the Root model to perform like a W=64 mm device.

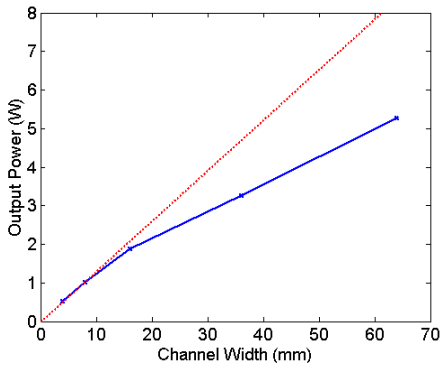


Figure 5. Simulation results showing maximum output power against device width. Load-pull simulations at 900 MHz were performed in ADS using the 4 mm Root model, biased at Vg=1.2V and Vd=3.5V, with the inductances from Table 1 to mimic the characteristics of the larger devices. The dotted line shows the ideal scaling (linear increase) of output power with W. The output power at W=64mm reaches only 5.2W, whereas a linear scaling should yield 8W.

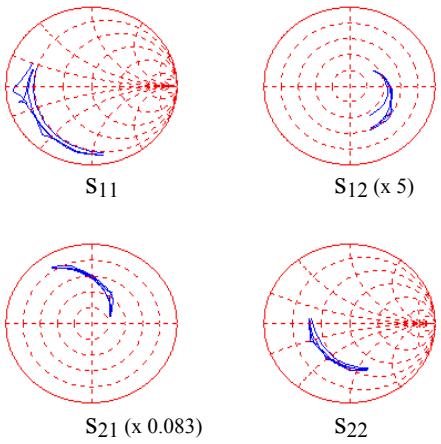


Figure 7. S-parameter simulation results (f=0.6-3.0 GHz, Vg=1.2V, Vd=3.5V) for systems with baluns. For device widths of 8mm, 16mm, 32mm, and 64mm, all the curves are nearly identical, demonstrating that the effects of mutual inductance is negated by the phase-inversion generated by the baluns.

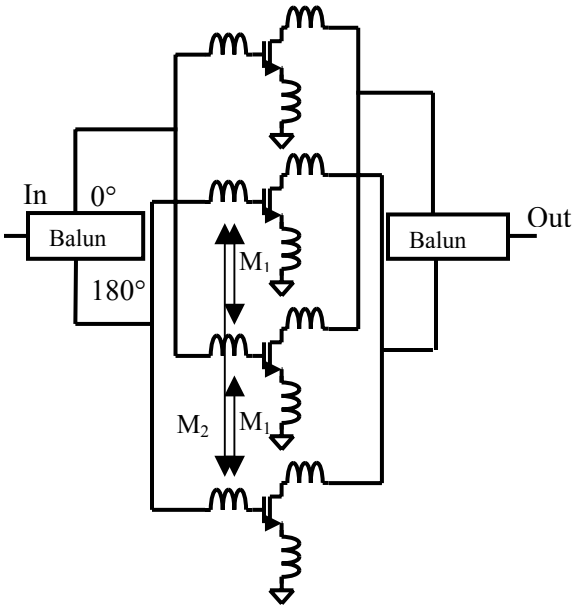


Figure 6. Power amplifier circuit diagram to counter the mutual inductance at the three terminals. Phase inversion is achieved in adjacent unit cells by using baluns. Phase inversion generates negative mutual inductance between adjacent unit cells ($M_1<0$), thus countering the source degeneration effect caused by positive mutual inductance observed in traditional power amplifier devices. Although $M_2>0$, since $|M_1|>|M_2|$ due to the larger distance for M_2, the net effect of all the mutual inductances should be negative. This canceling of mutual inductance should not only occur at the gate terminal as shown, but also at the drain and source terminals.

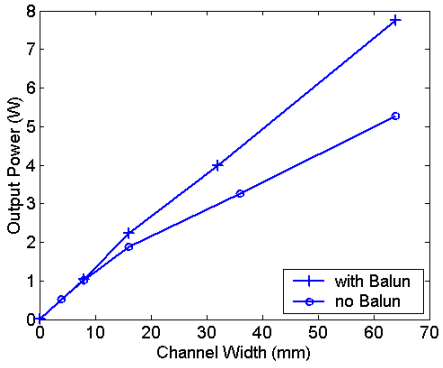


Figure 8. Maximum output power plot against device width (W), comparing the systems with and without baluns. The curve for the system without baluns is taken from Figure 5. By using baluns, the mutual inductance is canceled, and the maximum output power becomes roughly proportional to W. Comparison at W=64mm shows output powers of 5.2W without baluns, but 7.8W with baluns.