

CHARACTERIZATION, MODELING, AND DESIGN OF ESD PROTECTION CIRCUITS

By

STEPHEN G. BEEBE

March 1998

Technical Report No. xxxxxxxx

Prepared under
Semiconductor Research Corporation Contract 94-SJ-116
Semiconductor Research Corporation Contract 94-YC-704

Special support provided by
Advanced Micro Devices, Sunnyvale, California

© Copyright by Stephen G. Beebe 1998
All Rights Reserved

Abstract

For more than 20 years, susceptibility of integrated circuits to electrostatic discharge (ESD) has warranted the use of dedicated on-chip ESD protection circuits. Although the problem of ESD in integrated circuits (ICs) has received much attention industry-wide since the late 1970s, design of robust ESD circuits remains challenging because ESD failure mechanisms become more acute as critical circuit dimensions continue to shrink. In the past increased sensitivity of smaller devices, coupled with a lack of understanding of ESD phenomena and the consequent trial-and-error approach to ESD circuit design, resulted in design of ESD protection effectively starting from scratch in each new technology. Now, as life cycles of new technologies continue to decrease, better analysis capabilities and a systematic design approach are essential to accomplishing the increasingly difficult task of adequate ESD protection-circuit design.

This thesis reviews the problems of ESD in the IC industry and the standard models used to characterize ESD protection-circuit performance. Previous approaches to ESD circuit design are discussed, including design theory and specific design examples. Transmission-line pulsing (TLP), a relatively new ESD characterization and analysis test method, is presented. This test method offers many advantages over standard characterization techniques, including the ability to extract critical parameters of an ESD protection circuit and to determine the failure level of a circuit over a wide range of ESD stress durations. Dependencies of ESD circuit performance on critical process parameters of a CMOS technology are discussed. Two-dimensional numerical device simulation techniques are presented for modeling ESD in circuits, including electrothermal simulation and a curve-tracing algorithm, detailed in an appendix, used to guide simulations through complex current-voltage (I-V) curves. Results are given for TLP experiments run on parametric ESD structures created in a 0.5 μm CMOS technology, including MOSFET snapback I-V

characteristics and failure thresholds. Results of calibrated simulations are also presented and compared to experiments. Details of the simulation calibration procedure are provided.

A design methodology for multiple-fingered CMOS ESD protection transistors is presented. The methodology employs empirical modeling to predict the I-V characteristics and ESD withstand level of a circuit given the circuit's layout parameters. A critical correlation between transmission-line pulse withstand current and human-body model (HBM) withstand voltage is demonstrated. Quantitative prediction is achieved for HBM withstand voltages in a 0.35 μm -technology SRAM circuit. Optimization of protection-transistor layout area for a given ESD withstand level is illustrated. The thesis concludes with a discussion of future work and issues pertaining to the impact of ESD on future technologies.

Acknowledgments

This work could not have been accomplished without the assistance of many people. Primary thanks go to Professor Robert Dutton of Stanford University and to Ben Tseng of Advanced Micro Devices for their foresight in recognizing the opportunity to apply recently introduced simulation techniques to a reliability problem which becomes increasingly important to the integrated-circuit industry with every new technology. Forming an industrial partnership with AMD provided an excellent opportunity to conduct research on a leading-edge technology, and during my tenure there as a graduate student I received help from many people I am now happy to call my coworkers. Kurt Taylor took me under his management basically sight unseen, but his increasing interest in ESD generated many enlightening discussions and his effort in laying out test structures made the experimental work in this thesis possible. Kurt must also be credited for steering me towards the design-of-experiments modeling approach. Others deserving thanks include, but are not limited to, Dave Forsythe for discussions regarding simulator calibration, Pete Williams for helping take experimental data, Dave Greenlaw, Ken Hicks, D.H. Ju, Kelvin Lai, and Ian Morgan.

At Stanford, special gratitude goes to Zhiping Yu and Ronald Goossens, both of whom provided not only technical guidance but career advice and friendship. Ronald must also be credited (or blamed) for some of the most grueling runs since my college track days. I would like to thank the members of my reading and orals committees: Drs. Robert Dutton, Bruce Wooley, Kenneth Goodson, and William Dally. Fellow students who provided help include Aon Mujtaba for discussion of mobility modeling, Chiang-Sheng Yao for discussion of impact-ionization modeling, Richard Williams for discussion of any manner of device physics, and Zak Sahul for providing answers to many questions regarding the Unix operating system. Support was also provided by Chris Quinn and Todd Atkins of

EECF/EECNS and by Fely Barrera and Maria Perea. To the other members of the TCADre, I have not forgotten you and will often reminisce on those three character-building softball seasons which taught us that victory is sweeter when tasted less often.

Contents

Abstract	iii
Acknowledgments	v
List of Figures	xi
List of Tables	xvi
1 Introduction	1
1.1 ESD in the Integrated Circuit Industry	3
1.2 Characterizing ESD in Integrated Circuits	4
1.3 Protecting Integrated Circuits from ESD	6
1.4 Numerical Simulation	8
1.5 Design Methodology	11
1.6 Outline and Contributions.	12
2 ESD Circuit Characterization and Design Issues	15
2.1 Classical ESD Characterization Models and Industrial Testing	16
2.2 Transmission Line Pulsing	19
2.2.1 MOSFET Snapback I-V Curve	22
2.2.2 Failure Power vs. Time to Failure.	29
2.2.3 Leakage Current Evolution	33
2.2.4 Advanced TLP Setup	35
2.3 Overview of Protection Circuit Design	37
2.4 Dependence of Critical MOSFET I-V Parameters on Process and Layout	44
2.5 Design Methodology	49

3 Simulation: Methods and Applications	55
3.1 Lattice Temperature and Temperature-Dependent Models	57
3.1.1 Mobility and Impact Ionization Models	58
3.1.2 Analysis of Thermal Assumptions	61
3.2 Curve Tracing	64
3.3 Mixed Mode Simulation	67
3.4 Previous ESD Applications	70
3.5 Extraction of MOSFET I-V Parameters	74
3.6 Extraction of MOSFET P_f vs. t_f Curve	77
3.7 Simulation of Dielectric Failure and Latent ESD Damage	86
4 Simulation: Calibration and Results	95
4.1 Calibration Procedure	96
4.1.1 Structure Definition	96
4.1.2 Calibration of MOSFET Characteristics	99
4.1.3 Calibration of the Snapback I-V Curve	107
4.1.4 Calibration of Thermal Failure	116
4.2 MOSFET Snapback I-V Results	120
4.3 Device Failure Results	125
4.4 Design Example	134
5 Design and Optimization of ESD Protection Transistor Layout	139
5.1 Methodology	141
5.1.1 Characterization of Test Structures	141
5.1.2 Correlation of TLP to the Human Body Model	143
5.1.3 Development of Second-Order Linear Model	148
5.1.4 Identification of Critical Current Paths	152
5.2 Application	154
5.3 Analysis	156
5.3.1 Model Terms	156
5.3.2 SRAM Model Prediction	158
5.4 Optimization	160
5.5 Summary of Design Methodology	162

6 Conclusion	165
6.1 Contributions	166
6.1.1 Transmission Line Pulsing	166
6.1.2 Numerical Device Simulation.	167
6.1.3 Design Methodology	168
6.2 Future Work	168
6.2.1 Characterization.	168
6.2.2 Modeling	170
6.2.3 Design	171
A Tracer User's Manual	173
A.1 Command Line	174
A.2 Trace File	174
A.3 CONTROL Card	175
A.3.1 Description.	175
A.3.2 Syntax	175
A.3.3 Parameters	175
A.3.4 Examples.	176
A.4 FIXED Card.	177
A.4.1 Description.	177
A.4.2 Syntax	177
A.4.3 Parameters	177
A.4.4 Examples.	177
A.5 OPTION Card.	178
A.5.1 Description.	178
A.5.2 Syntax	178
A.5.3 Parameters	178
A.5.4 Examples.	181
A.6 SOLVE Card	182
A.6.1 Description.	182
A.6.2 Syntax	182

A.6.3	Parameters	182
A.6.4	Examples.	183
A.7	Input Deck Specifications.	185
A.7.1	Load and Solve Cards	185
A.7.2	Contact Card	185
A.7.3	Method Card	186
A.7.4	Options Card.	186
A.8	Data Format in Output Files	186
A.9	Examples	187
A.9.1	BV_{CEO}	187
A.9.2	GaAs MESFET	192
	Bibliography	199

List of Figures

- 1.1 ESD protection circuits in a CMOS technology 8
- 2.2 Circuit model for the HBM and MM and SPICE3-generated short-circuit
HBM output current waveform 17
- 2.3 SPICE-generated short-circuit MM output current waveforms. 18
- 2.4 Circuit model for the CDM 20
- 2.5 TLP schematic and equivalent circuit. 21
- 2.6 Qualitative I-V curve for an NMOS transistor subjected to a positive
ESD pulse 23
- 2.7 Depiction of second snapback in a qualitative transient I-V curve 26
- 2.8 A screen capture of a Tektronix TDS 684A digitizing oscilloscope for a
circuit response to TLP 27
- 2.9 Screen capture of breakdown and snapback 28
- 2.10 Screen capture of second breakdown 28
- 2.11 3D thermal box model. 29
- 2.12 A qualitative schematic of input power-to-failure vs. time-to-failure
predicted by an analytical thermal model. 32
- 2.13 Qualitative plot of device leakage evolution vs. stress-current level of
a TLP experiment 34
- 2.14 Advanced TLP schematic and equivalent circuit 36

2.15	ESD diode protection circuit in a CMOS technology and use of a series resistor in combination with diode protection	39
2.16	CMOS input and output protection	40
2.17	Gate-bouncing techniques.	42
2.18	Combination resistor/transistor ESD input protection circuit.	43
2.19	Layout of a multiple-finger NMOS transistor between input and V_{SS}	44
2.20	Circuit diagram of CMOS input protection using multifinger structures. . .	50
2.21	Qualitative TLP I-V curve for an NMOS multifinger structure subjected to a positive ESD pulse	52
3.22	Qualitative plot of impact-ionization rates for electrons and holes.	60
3.23	Schematic representation of various types of simulator bias specification.	64
3.24	Schematic of a general device with external load and voltage; adapting the load line	66
3.25	Projection and recalibration.	67
3.26	Mixed-mode circuit model for an NMOS transistor subjected to the human-body model	69
3.27	Mixed-mode circuit model for a multiple-finger ESD NMOS structure subjected to the human-body model	69
3.28	ESD protection circuit used for SPICE simulations by Chatterjee et al. [33]	71
3.29	I-V curves for curve-tracing (solid line) and TLP (points) simulations for a 20/0.5 μ m MOSFET	76
3.30	I-V curves of a single TLP simulation and of points resulting from a group of TLP simulations.	77
3.31	The dependence of the steady-state change in peak temperature, ΔT_{SS} , on b/c	80

3.32	Simulated $1/\Delta T$ vs. time and ΔT vs. time curves for various length/width ratios in a uniformly doped semiconductor region with a constant applied power	81
3.33	Power to failure, normalized by a , κ , and ΔT , is plotted vs. time to failure for the 2D and 3D implementations of the thermal box model	83
3.34	The maximum electric field in the gate oxide of an ESD-protection MOSFET subjected to a square pulse with a 3ns rise time is plotted vs. time	87
3.35	A qualitative plot of time-to-failure vs. stress voltage	89
3.36	Gate current vs. time for 50/0.75 μm MOSFETs with (a) 10K Ω gate resistor and (b) grounded gate.	91
3.37	A constant-temperature contour is plotted for every 200K increment in temperature for a simulation structure at the time of peak ESD stress	92
3.38	A contour within which the intrinsic carrier concentration, n_i , is greater than the background doping level is drawn for a simulation structure at the time of peak ESD stress	93
4.39	This example of a MEDICI-generated grid shows the concentration of grid points in the channel, LDD, and junction regions	98
4.40	Qualitative depiction of I-V curves used for MOSFET calibration.	100
4.41	I-V points from the transmission-line pulse sweep of a standard characterization structure	108
4.42	Device current per width vs. device voltage for a dc-sweep simulation of the standard structure.	111
4.43	Simulated I-V sweep for T=297K boundary conditions	114
4.44	Device voltage and current vs. time for a transient simulation of the 100/0.75 μm structure	118
4.45	Experimental and simulated snapback resistance, R_{sb} , vs. contact-to-gate spacing for a 50/0.75 μm MOSFET test structure	121
4.46	Experimental snapback resistance, R_{sb} , vs. inverse gate width.	122

4.47	Experimental and simulated snapback voltage, V_{sb} , vs. gate length for 20 μm -wide test structures	123
4.48	Simulated trigger voltage, V_{t1} , vs. gate resistance, R_{gate} , for the 50/0.75 μm -wide test structure	125
4.49	Power to failure, P_f , (a) and current to failure, I_f , (b) vs. device width for 0.75 μm test structures	126
4.50	Simulated and experimental power-to-failure, P_f , vs. contact-to-gate spacing for 50/0.75 μm test structures.	128
4.51	Experimental current-to-failure, I_f , vs. contact-to-gate spacing for 50/0.75 μm test structures	129
4.52	Power at second breakdown, P_{t2} , vs. time to breakdown, t_2 , for a 25/0.75 μm structure.	131
4.53	Experimental power-to-failure (a) and current-to-failure (b) vs. time-to-failure, t_f , for 50/0.75 μm test structures with varying CGS	133
5.54	Snapback I-V curve for a 50/0.6 μm NMOS transistor generated by TLP	141
5.55	Layout of a four-fingered ESD structure	143
5.56	Normalized (divided by width) withstand current vs. drain-side CGS	147
5.57	Normalized withstand current vs. number of 50/0.6 μm fingers	148
5.58	Example of a complete second-order linear equation modeling the response of a variable with three factors	149
5.59	Schematic of critical ESD protection circuits in a chip with split power supplies and separate clock supply	153
5.60	Catalyst model graph for Lot 1 V_{sb} , R_{sb} , and $I_{TLP,ws}$	157
5.61	Calculated minimum area of transistor source/drain diffusion needed for 5kV HBM protection	162
5.62	Block diagram of ESD circuit design methodology	163
A.63	The input file, bvceo.pis, for the BV_{CEO} example	188
A.64	The trace file, bvceo.tra, for the BV_{CEO} example	189

A.65	The output file, bvceo.out, for the BV_{CEO} example	190
A.66	Collector current vs. collector voltage for the BV_{CEO} example	191
A.67	The mesh generation and eliminate statements of the file mes.pis for the GaAs MESFET example	193
A.68	The second half of the file mes.pis for the GaAs MESFET example.	194
A.69	The input file, mesvg.5.pis, for the GaAs MESFET example	195
A.70	The trace file, mesvg.5.tra, for the GaAs MESFET example.	196
A.71	Drain current vs. drain voltage for the GaAs MESFET example.	196
A.72	The output file, mesvg.5.out, for the GaAs MESFET example.	197

List of Tables

2.1	Dependence of critical I-V parameters on process and layout	46
5.2	Experimental and modeled SRAM HBM withstand voltages	156