CHARACTERIZATION, MODELING, AND DESIGN OF ESD PROTECTION CIRCUITS

By

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Abstract

For more than 20 years, susceptibility of integrated circuits to electrostatic discharge (ESD) has warranted the use of dedicated on-chip ESD protection circuits. Although the problem of ESD in integrated circuits (ICs) has received much attention industry-wide since the late 1970s, design of robust ESD circuits remains challenging because ESD failure mechanisms become more acute as critical circuit dimensions continue to shrink. In the past increased sensitivity of smaller devices, coupled with a lack of understanding of ESD phenomena and the consequent trial-and-error approach to ESD circuit design, resulted in design of ESD protection effectively starting from scratch in each new technology. Now, as life cycles of new technologies continue to decrease, better analysis capabilities and a systematic design approach are essential to accomplishing the increasingly difficult task of adequate ESD protection-circuit design.

This thesis reviews the problems of ESD in the IC industry and the standard models used to characterize ESD protection-circuit performance. Previous approaches to ESD circuit design are discussed, including design theory and specific design examples. Transmission-line pulsing (TLP), a relatively new ESD characterization and analysis test method, is presented. This test method offers many advantages over standard characterization techniques, including the ability to extract critical parameters of an ESD protection circuit and to determine the failure level of a circuit over a wide range of ESD stress durations. Dependencies of ESD circuit performance on critical process parameters of a CMOS technology are discussed. Two-dimensional numerical device simulation techniques are presented for modeling ESD in circuits, including electrothermal simulation and a curve-tracing algorithm, detailed in an appendix, used to guide simulations through complex current-voltage (I-V) curves. Results are given for TLP experiments run on parametric ESD structures created in a 0.5μm CMOS technology, including MOSFET snapback I-V

characteristics and failure thresholds. Results of calibrated simulations are also presented and compared to experiments. Details of the simulation calibration procedure are provided.

A design methodology for multiple-fingered CMOS ESD protection transistors is presented. The methodology employs empirical modeling to predict the I-V characteristics and ESD withstand level of a circuit given the circuit's layout parameters. A critical correlation between transmission-line pulse withstand current and human-body model (HBM) withstand voltage is demonstrated. Quantitative prediction is achieved for HBM withstand voltages in a 0.35μm-technology SRAM circuit. Optimization of protection-transistor layout area for a given ESD withstand level is illustrated. The thesis concludes with a discussion of future work and issues pertaining to the impact of ESD on future technologies.

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