ESD Simulation to Find Correlation Between Junction Depths and Snapback Slope Using 0.35μm nMOSFETS

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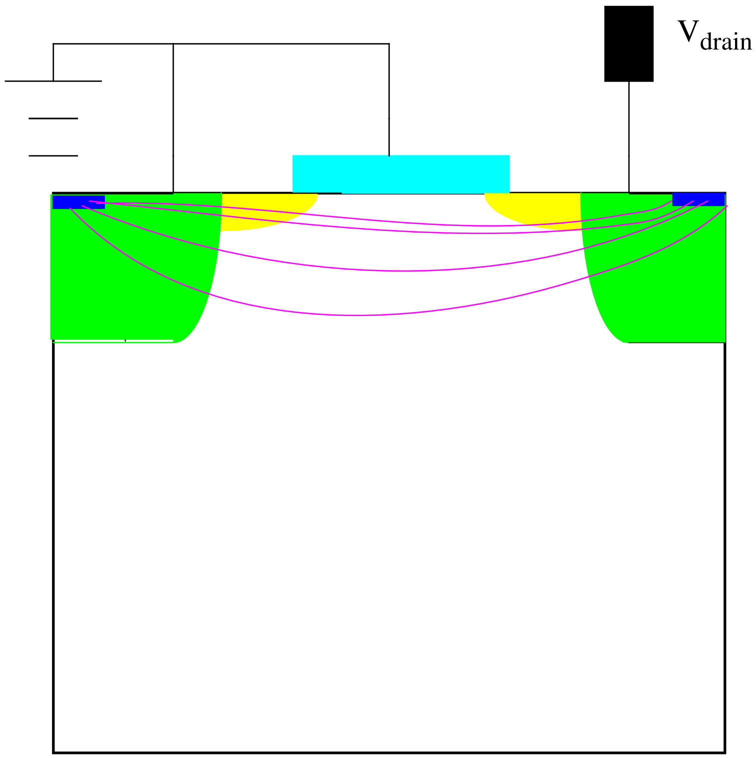
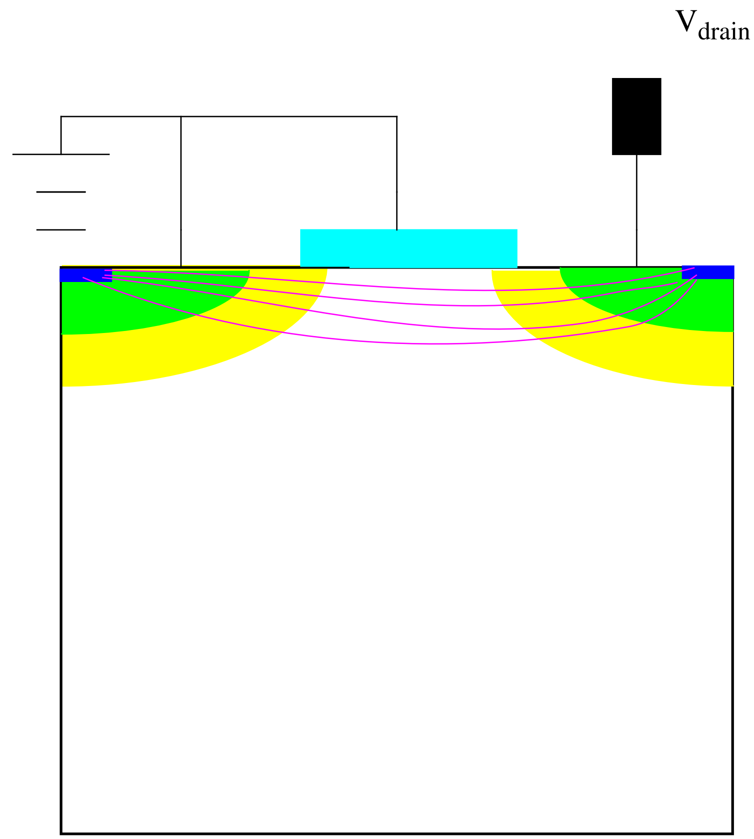
Future Work

- The results need to be verified with different grid densities.
- Test structures need to be fabricated to verify the simulation results.
- Transmission Line Pulsing (TLP) method should be used to measure the test structures.

Conclusion (cont.)



Current Flow Plot for LDD



Current Flow Plot for DDD

Conclusions

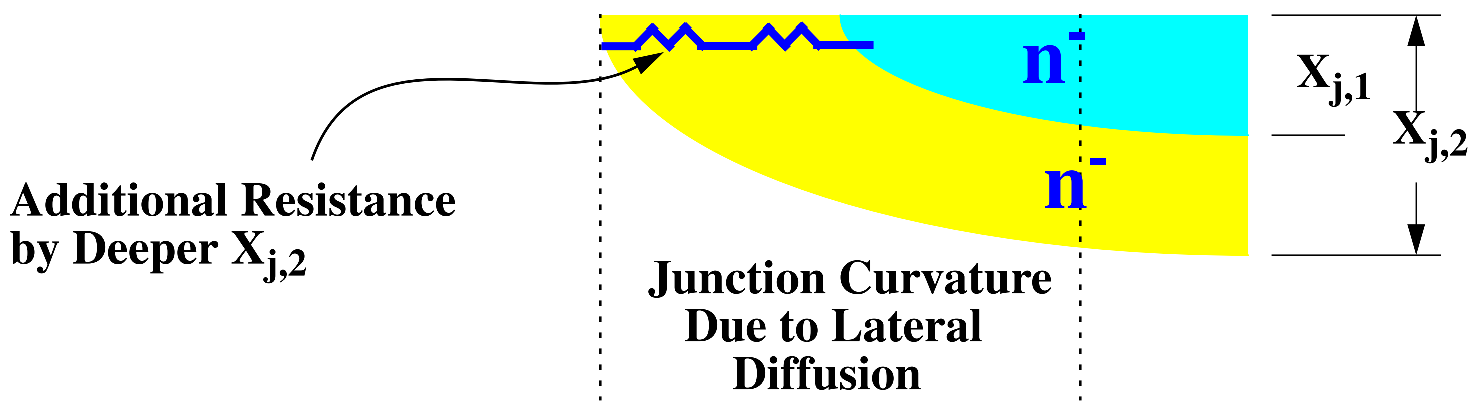
The following conclusions are reached:

- **The snapback slope ($1/R_{sb}$) does increase as the n^- junction depths increase.**
- **The snapback slope does not depend on the junction curvature of the n^+ region ($X_{j,D}$).**

During the snapback mode, the current flows from the bulk to the drain contact. As shown in the contour figures, the current must pass thru the n^- region to reach the contacts; therefore, the resistance of n^- region plays a role in determining the snap-back slope.

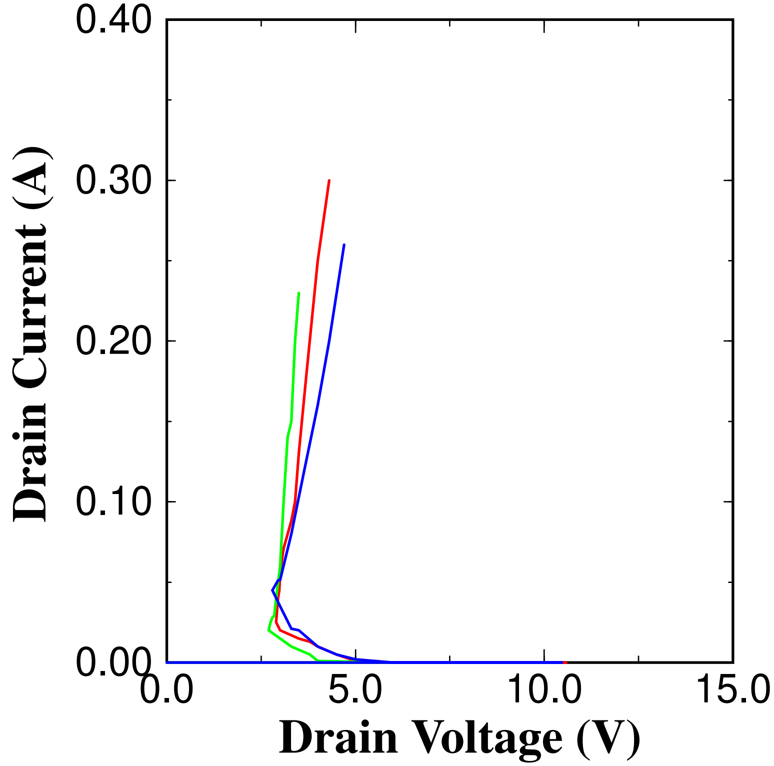
Discussion

Based on the simulation results, the snapback slope ($1/R_{sb}$) decreases with deeper n^- junction depths. In theory, $1/R_{sb}$ should increase because the source/drain diffusions resistance decreases with increasing junction depth; however, deeper junctions have larger junction curvatures, assuming the lateral diffusion constant is the same, so the larger junction curvature adds more lateral resistance. From simulation results, the effect of n^+ junction depths on the snapback slope is not observed.

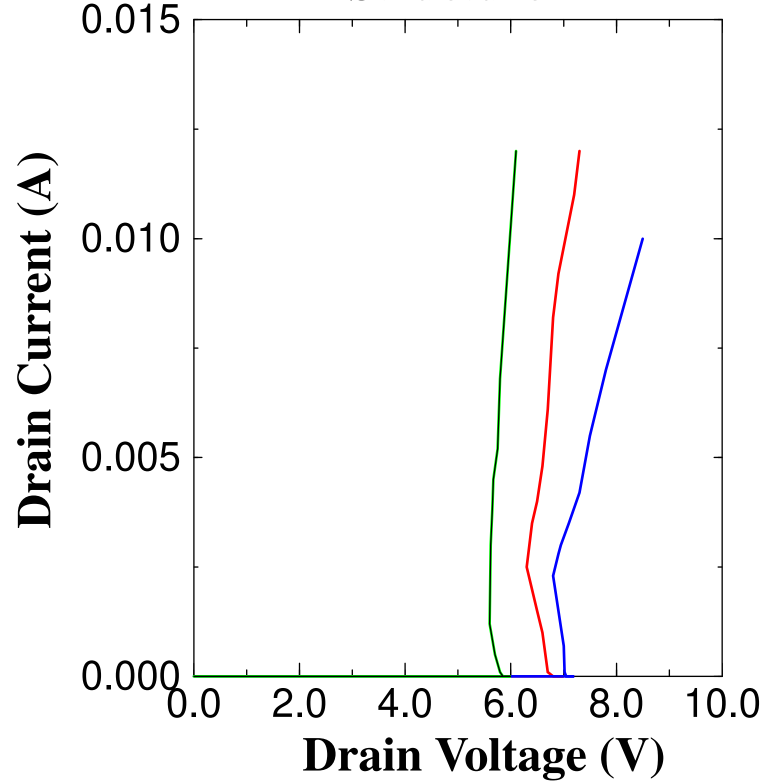


Simulation Results

Snapback Slope vs. $X_{j,L}$ and $X_{j,D}$ for the LDD Structure



Snapback Slope vs. $X_{j,L}$ for the DDD Structure



---- $X_{j,L}$: 0.08µm, $X_{j,D}$: 0.10µm ---- $X_{j,L}$: 0.11µm, $X_{j,D}$: 0.15µm
---- Xj,L: 0.14µm, Xj,D: 0.20µm

$X_{j,D}$: 0.06µm same for all cases
---- $X_{j,L}$: 0.11µm ----$X_{j,L}$: 0.14µm ---- $X_{j,L}$: 0.17µm

Simulation Procedure

For both DDD and LDD structures, the following simulation procedures were used:

- Three cases of junction depths for each structure were simulated:

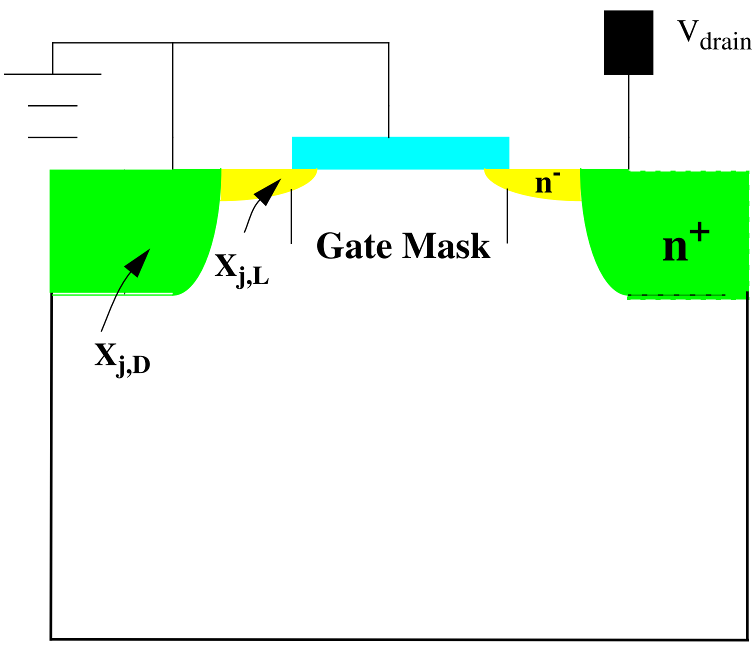
  1. $X_{j,D}$ (n^+ junction for the LDD structure) was varied from 0.10μm to 0.20μm in increments of 0.05μm; $X_{j,D}$ (for the DDD structure) was constant at 0.06μm.

  2. $X_{j,L}$ (n^- junction for the LDD structure) was varied from 0.08μm to 0.14μm in increments of 0.03μm; $X_{j,L}$ (n^- junction for the DDD structure) was varied from 0.11μm to 0.17μm in increments of 0.03μm.

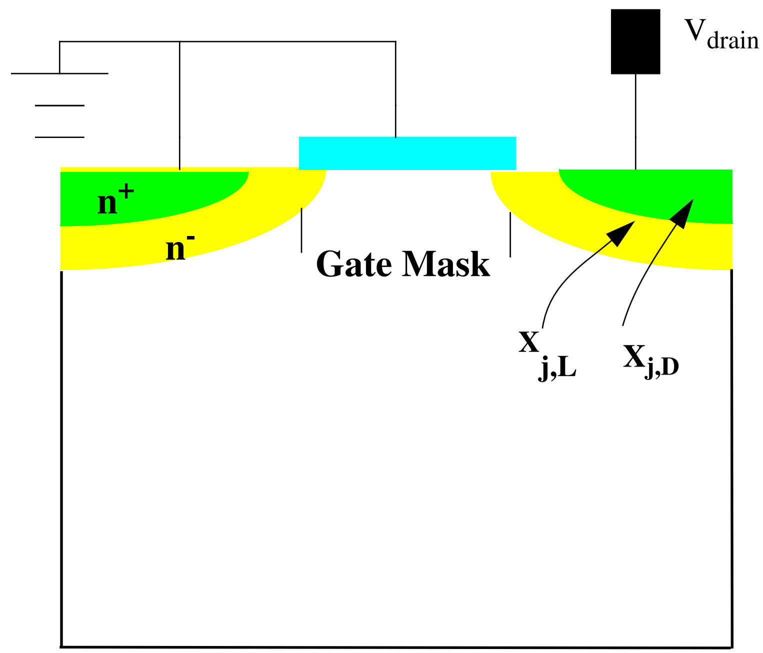
While varying the junction depth, the length of the gate mask changes to keep the effect channel length the same for all junction depths, so that the change of R_{sb} would be affected by X_j's only.

Simulation of the Snapback Slope ($1/R_{sb}$)

This study examines the relationship between the junction depths (X_j) and snapback slope. A LDD and a DDD (double-diffused-drain) structures shown below, were constructed from AMD's 0.35μm nMOS.



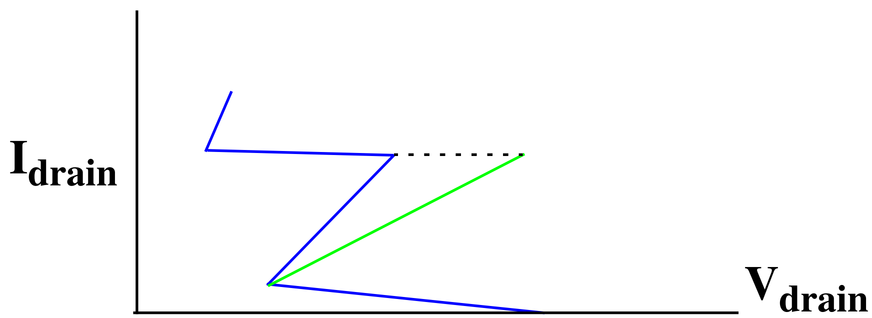
LDD Structure



DDD Structure

Modeling of Snapback Slope ($1/R_{sb}$)

In the snapback mode, the current rises along a line with slope $1/R_{sb}$, where R_{sb} is the snapback impedance. R_{sb} equals the source and drain diffusions and contact resistance. The device incurs no damage in the snapback mode unless the current level becomes high enough to trigger thermal runaway (also called second breakdown), a positive feedback process. The goal of ESD protection is to raise the ESD failure threshold. By increasing R_{sb}, the above objective can be achieved because larger R_{sb} delays the formations of hot spots. Usually, the magnitude of R_{sb} is increased by increasing the contact resistance.



Modeling of V_{sb} (cont.)[1]

Based on the model circuit,

$$V_{bs} = I_{sub} (R_{sub} + R_{ext}) - V_{SB}.$$

When Vbs > 0.6, the parasitic bipolar turns on. Once the parasitic bipolar is on, the nMOS goes into snapback region, and the snapback voltage (V_{sb}) is determined by the breakdown voltage (BV_{dss}) and effective current gain of the parasitic BJT (β_{eff}).

$$V_{sb} \sim BV_{dss} / (\beta_{eff})^{1/n}$$

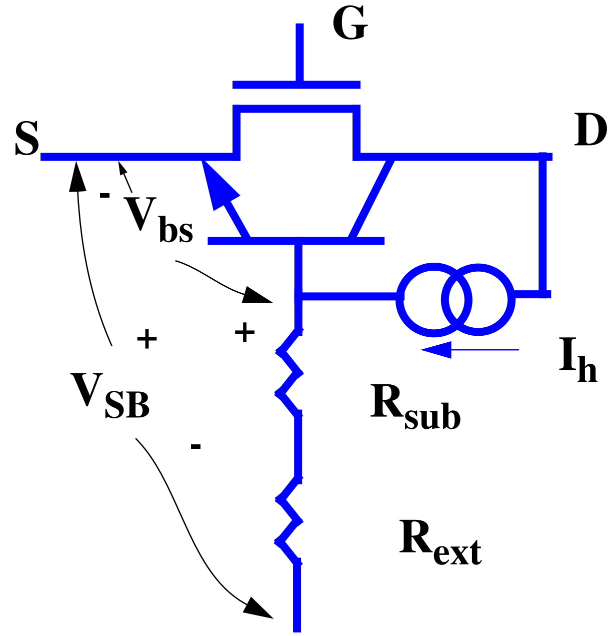
$$\sim BV_{dss} (L_{eff}/L_d)^{2/n} / 2^{1/n},$$

where L_{eff} (W_B of the parasitic BJT) is the effective channel length, L_d is the electron diffusion length in the p-type substrate, and n is an empirical constant.

1. K.L. Chen. "The Effects of Interconnect Process and Snapback Voltage on the ESD Failure Threshold of NMOS Transistors," ***IEEE Transactions on Electron Devices*****, VOL. 35, NO. 12, December 1988.**

Modeling of V_{sb}

The magnitude of the first breakdown voltage (V_{t1}) depends on the junction depth and junction curvature; the value of the snapback voltage (V_{sb}) depends on the parasitic bipolar as well as V_{t1}. The snapback voltage can be modeled as follows:



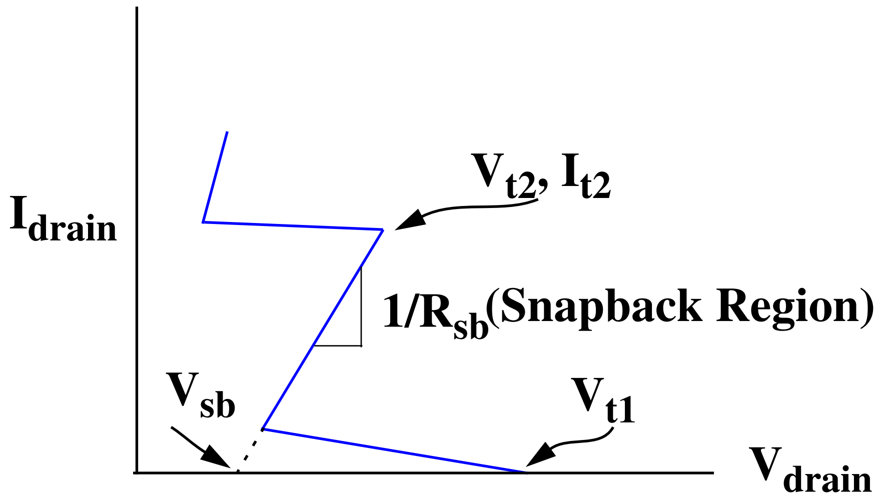
Design Constraints

For best ESD protection, there are limits on the values of the critical I-V parameters:

- **The V_{t1} should be designed to have the smallest breakdown voltage so that it will breakdown first to protect the internal circuitry from breaking down.**
- **The V_{sb} should be lower than the gate-oxide breakdown voltage as well as the avalanche breakdown voltage.**
- **The snapback slope ($1/R_{sb}$) should be small, preventing current crowding and increasing the ESD failure threshold.**
- **Extremely high current causes silicon to heat up above its melting point; ideally, I_{t2} should be chosen as high as possible, but it is limited by the thermal capacity of the device.**

Introduction to ESD Protection (cont.)

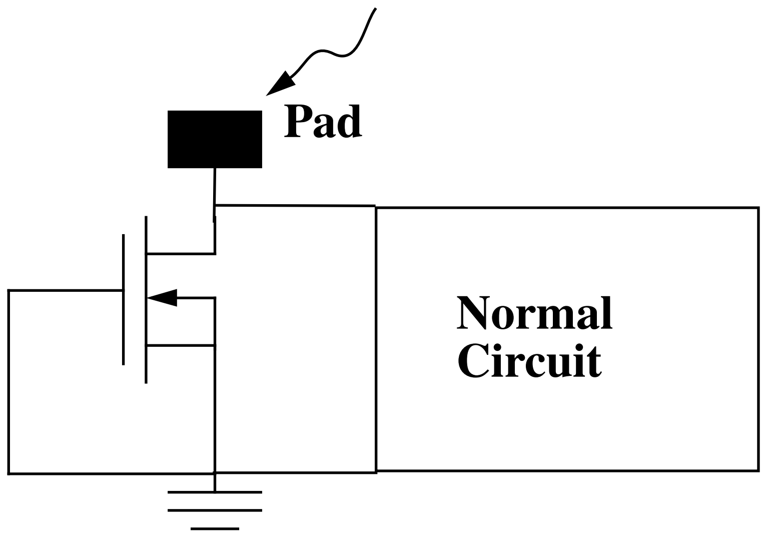
The I-V curve for the nMOS circuit above is shown below:



- **V_{t1} is defined as the trigger voltage, which is the voltage needed to trigger the device into snapback after the avalanche breakdown.**
- **V_{sb} is defined as the snapback voltage; it clamps the circuit voltage at V_{sb}.**
- **V_{t2} and I_{t2} are defined as the second breakdown voltage and current respectively; beyond V_{t2}, the device is damaged.**

Introduction to ESD Protection

The MOSFET configuration shown below is often used as a part of an ESD protection circuit. During normal operation, the protection circuit is off; however, during ESD stress, as a large discharge pulse is applied to the drain, the nMOS goes into avalanche breakdown followed by snapback, which is a parasitic bipolar action. Once in snapback mode, the nMOS can be used to clamp voltage and discharge current.



Research Motivation

As device dimensions shrink, designing ESD protection circuits becomes more challenging, especially in MOS technology. The protection circuits are more prone to damage due to higher current densities, which resulting from smaller device area. It is known that the magnitude of the snapback slope ($1/R_{sb}$) directly affects the ESD failure threshold. This study examines the dependence between the junction depths (X_j) and snapback slope ($1/R_{sb}$) based on AMD's 0.35μm nMOS.

Introduction

Electrostatic discharge (ESD) is one of the most important reliability problems in the integrated circuit industry. It is responsible for about one-third of field failures. The traditional design of ESD protection circuits by trial-and-error is not only time consuming, but also, it yields non-reusable circuits which can not be migrated to future technologies. A better design methodology is to employ numerical device simulation, which takes into consideration the underlying physics. Process and layout parameters of the device can be varied, with the results revealing important insights into the dependences of device characteristics with respect to the varied parameters. These dependences can also be used to predict the performance of similar circuits in future technologies, so previous design efforts are not wasted, but rather leveraged in creating new circuits.