nates the intrinsic device resistance, and hence determines the I-V slope. This verifies the use of techniques that increase the ballasting resistance of multi-finger ESD protection structures to provide more uniform turn-on.

We also note that at all Vg, the current level increases rapidly around the same Vd, corresponding to values of M that agree well with a second condition for current regeneration using positive feedback analysis [1]:

$$M-1 = 1/\beta \quad (4)$$

where β is current gain of the parasitic BJT.

Calibration and Results

Comparison of simulation results with measurements is shown in Figure 5. Tests were done on a 20u/0.35u NMOS device. There is good match for both the triggering voltage and current at Vg=0V. Also, at higher Vg, the transition in the avalanche region is good. The avalanche turn-on voltage for the different Vg's corresponds to M ~ 1.3. This is consistent with the use of β=3 in our BJT model (from (4)).

Noting that the measured turn-on voltage is around 6 volts, we use d2=6.7V. Next, we find that k2=1.8V^{-1} and Rsub=1k ohms gives acceptable fit in the snapback region for Vg=0V. Finally, noting that the output conductance starts increasing around Vd=4V, we use k1=0.07V^{-1}, d1=3.5V to achieve good fit in that region.

Conclusion

We have presented a more robust, computationally-stable formulation for the avalanche multiplicative M factor used in circuit modeling of MOS breakdown. This has useful applications for the design of ESD-protection circuits. Its continuity throughout all voltage range makes it friendlier to circuit simulators and improves convergence. The impact of each model parameter on the IV curve is described. The explanation for these effects are consistent with reported research. Finally, good agreement is obtained by calibrating to measurement results.

References

[1] F. Hsu, P. Ko, S. Tam, C. Hu, R. Miller, "An Analytical Breakdown Model for Short-Channel MOSFET's", *IEEE Trans. Elec. Dev.*, ED-29, p.1735-1740, 1982.

[2] A. Amerasekera, S. Ramaswamy, M. Chang, C. Duvvury, "Modeling MOS Snapback and Parasitic Bipolar Action for Circuit-Level ESD and High Current Simulations", *Proceedings of 34th Annual IEEE International Reliability Physics*, p.318-326, 1996.

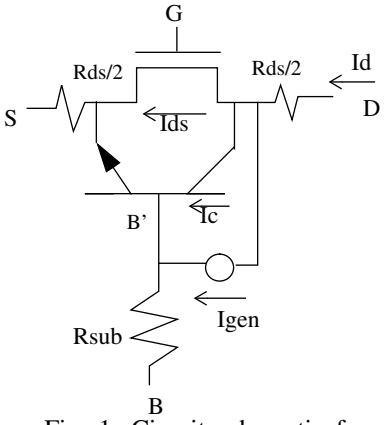

Fig. 1: Circuit schematic for simulating MOS breakdown.

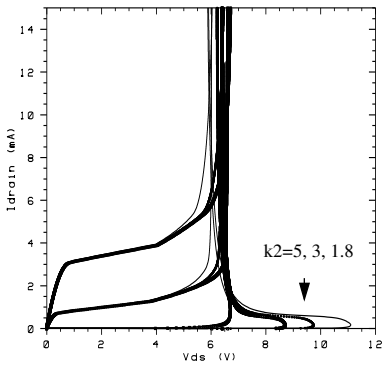

Fig. 2: Variation of snapback width with k2.

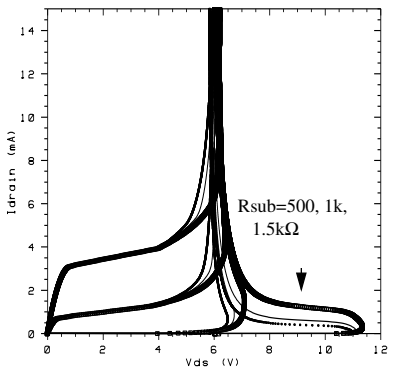

Fig. 3: Variation of snapback height with Rsub.

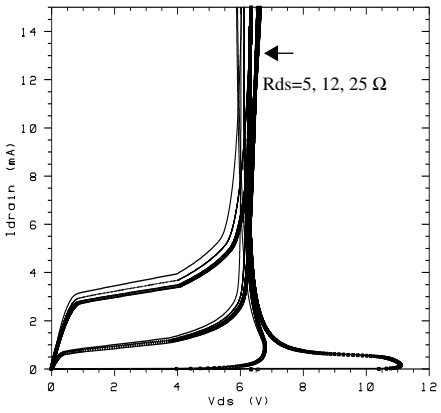

Fig. 4: Variation of snapback slope with Rds.

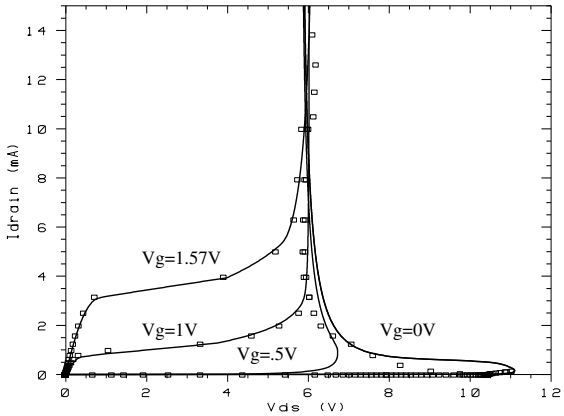

Fig. 5: Comparison of measurements (points) and simulation results (line).

A Computationally-Stable Quasi-Empirical Compact Model for the Simulation of MOS Breakdown in ESD-Protection Circuit Design

Shiang Liang Lim, Zhiping Yu, and Robert W. Dutton
Center for Integrated Systems, Stanford University, Stanford, CA 94305
Phone: (415) 725-3644, E-mail: sllim@gloworm.stanford.edu

Abstract -- This paper presents a simple-to-implement, semi-empirical model for circuit-level simulation of the MOS breakdown region, with application in ESD-protection circuit design. A formulation for the multiplicative factor M, used to model avalanche current generation, is shown that shows good convergence properties when used in circuit simulators. The effects of source/drain series resistance, substrate resistance and the M factor parameters are described. We describe how to calibrate the parameters for an NMOS device. Finally, we compare the simulated results with experimental data.

Introduction

Modeling of a transistor's I-V characteristic in the breakdown region is important for the design of electrostatic discharge (ESD) protection circuits. During an ESD stress, current and voltage levels far exceed the regions of normal transistor operation. The ability to model such high-current behavior in circuit simulators enhances fast and effective design of such protection circuits.

We can model the MOS breakdown region with a parasitic bipolar transistor in parallel with the MOS device, together with a current controlled current source that models the avalanche multiplicative effect [1]. Figure 1 shows a standard circuit used to model the breakdown. The avalanche-generated current is modeled as [1]:

$$Igen = (M-1)(Ids+Ic) \quad (1)$$

where Ids and Ic are the MOS surface drain current and parasitic bipolar (BJT) collector current respectively. The multiplication factor, M, is often written in the following form [2]:

$$M = 1/[1-k1.\exp(-k2/(Vd-Vdsat))] \quad (2)$$

where k1, k2 are fitting parameters related to the drain depletion width and impact ionization coefficients, and Vdsat is the MOS saturation voltage. However, this causes convergence problems when implemented directly in a circuit simulator such as SPICE. This is because there is a discontinuity in M when the denominator goes to zero. So as Vd increases, M goes to infinity. If the initial Ids and Ic are very small, as is the case when Vg is close to 0V, the parasitic bipolar will fail to turn on, because the iterations may "jump" across the discontinuity. This causes SPICE to either simulate the wrong behavior or fail to converge.

Alternative M Formulation

We can overcome the discontinuity in M by using a continuous function:

$$M = \exp(k1(Vd-Vdsat-d1)) + \exp(k2(Vd-Vdsat-d2)) \quad (3)$$

where k1, d1, k2, d2, are parameters to fit measurements. Two exponentials are used to approximate the M function from (2) in the region of interest, namely from M=1 to the point where snapback occurs. The result is a reasonably smooth I-V transition from the saturation region to the start of avalanche, and then snapback. This formulation shows better convergence properties than (2) because of its continuity, and produces the correct I-V behavior even at Vg=0V, without any modification to the SPICE code. This makes it simple to implement.

Analysis of Parameters

The k1 and k2 in (3) determine the rate of increase of M, while d1 and d2 are translation factors which determine when avalanche multiplication starts to take place. These four parameters can be used to fit measured data. Normally, d2 should be around the snapback voltage and k2 should be large to approximate the rapid increase in M near avalanche breakdown. The parameters k1 and d1 should be smaller, to model the initial gradual increase in conductance after the normal saturation region, but just before the very rapid increase in current.

From Figure 2, we observe that K2 affects the "width" of the snapback region for Vg=0V. We can explain this by first noting that since the total generated current is very small, we need a sufficiently high M to generate enough substrate current to forward-bias the parasitic BJT [1] (we assume that most of the avalanche-generated holes appear as substrate current before snapback occurs). Our simulations show that this occurs for Vb'~0.8V. Since M increases more slowly for a smaller k2, a higher Vd is needed to achieve the required M.

Figure 3 shows that more substrate resistance, Rsub, increases the "height" of snapback. The explanation is similar to above: to turn on the bipolar device at a lower Rsub, we need a higher trigger current. Hence, Rsub can be used as an additional parameter in modeling the snapback region.

Figure 4 shows the effect of the source/drain resistance, Rds, on the snapback slope. We note that a higher Rds gives a lower conductance. This is consistent with the view that at high current levels, the extrinsic resistance domi-