

# Accurate Doping Profile Determination Using TED/QM Models Extensible to Sub-Quarter Micron nMOSFETs

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## Abstract

Accurate doping profiles are needed to simulate device characteristics. We use capacitance-voltage curves to interrogate the doping profiles, threshold voltage, body effect, poly depletion and oxide thickness on a range of technology generations down to  $0.18\ \mu\text{m}$ . Proper modeling of both transient enhanced diffusion (TED) and quantum mechanical (QM) effects is essential to ensure the simulations match all aspects of the C-V data. The agreement confirms that the predicted doping profiles are accurate. Device simulations using these doping profiles give the correct threshold voltage, body effect and DIBL characteristics.

## Introduction

Doping profiles in small devices are difficult to measure directly using physical techniques. However, electrical measurements are very sensitive to slight changes in the doping profiles. We used capacitance-voltage curves measured on both large area ( $100 \times 100\ \mu\text{m}$ ) nMOSFETs and directly on serpentine, silicided nMOSFETs of varying gate lengths, to interrogate the doping profiles.

Figure 1 shows measured C-V data and default simulations for a  $0.35\ \mu\text{m}$  silicided nMOS device with a phosphorus LDD and a  $79\ \text{\AA}$  gate oxide. The measurement covers all aspects of C-V: inversion, accumulation, depletion as well as the flatband, threshold voltage and body effect. Also shown are default simulations where TED and QM effects are ignored. In the case of these default simulations, every portion of the curves is modeled incorrectly. Of particular importance to device simulation, the threshold voltage and body effect are not simulated accurately. Note that even if an effective oxide thickness is used, the fit is poor because the default doping profile is incorrect. In addition the predictions for drain induced barrier lowering (DIBL) using default simulations are usually estimated to be better than what is measured on actual devices.

Instead, a calibrated TED model is necessary to generate the correct channel and junction doping profiles. QM corrections are needed so the physical oxide thickness can be used in the simulations (rather than an effective oxide thickness) and to accurately model the C-V curves in accumulation and depletion regions. The modeling accuracy was established by using C-V curves at various substrate biases to probe the threshold voltage, body effect, poly depletion and oxide thickness on a range of technology generations down to  $0.18\ \mu\text{m}$ . In the remainder of this paper, we describe our calibration methodology in detail.

## DEFAULT SIMULATIONS

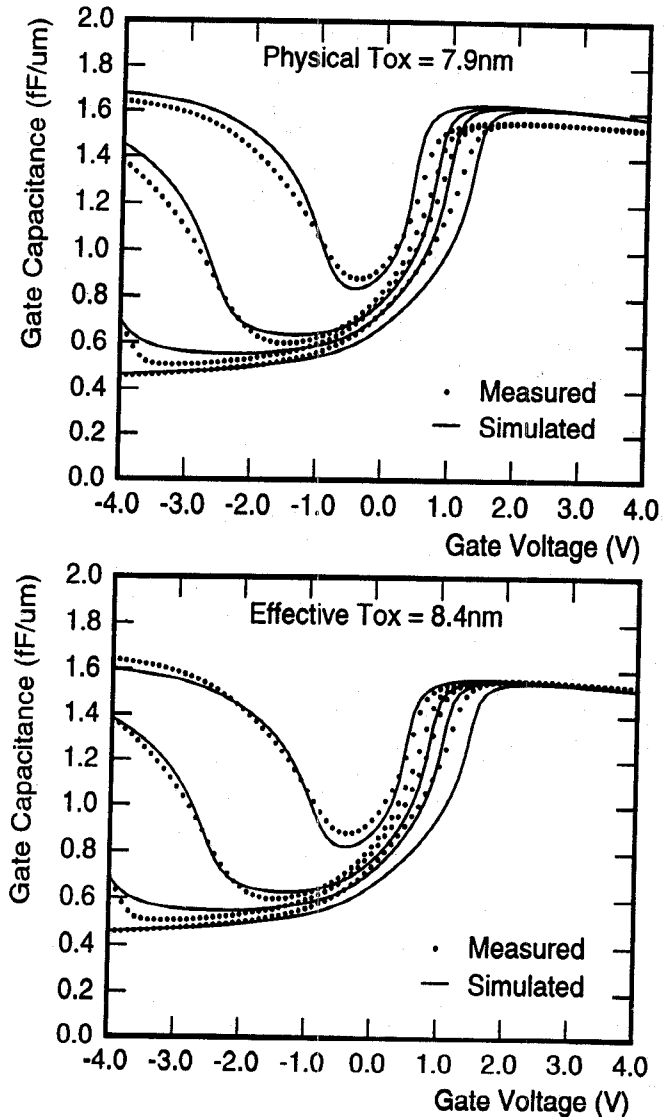


Figure 1: Measured and simulated gate capacitance ( $C_{gg}$ ) for  $0.35\ \mu\text{m}$  silicided, serpentine nMOS with substrate bias  $V_{bs}=0, -1.6, -3.2$  and  $-9.4$  volts. The simulations ignore TED and QM effects. (a) The simulations use the physical  $\text{tox} = 7.9\ \text{nm}$  (b) The simulations use an effective oxide ( $8.4\ \text{nm}$ ) chosen to fit the inversion capacitance. In either case the fit is very poor particularly with regards to threshold and body effect.

## Experiments and Simulations

### QM Corrections

The QM model is implemented in the 2-D device simulator PISCES and is based on van Dort's bandgap broadening approach [1] along with three major improvements: 1) the applicable range is extended to the accumulation region; 2) a fitting parameter  $\kappa$  is introduced and its value may be larger than 1 to account for the effect of quantized levels above the ground state and allow for calibration of the model to measurement data ( $\kappa = 1$  reduces to the original van Dort model.) 3) a newly developed relaxation scheme for AC analysis including QM effects is implemented allowing the calculation of the cross capacitances ( $C_{gb}$  and  $C_{gsd}$ ) [2]. The physical gate oxide thickness ( $t_{ox}$ ) is measured using ellipsometry and  $\kappa$  in the QM model is determined by fitting the accumulation capacitance for the large area nMOSFETs. The active poly doping,  $N_p$ , is then obtained from the inversion side of the curve. The comparison between simulated and measured  $C_{gg}$  vs.  $V_g$  is shown in Figure 2. It can be seen that  $\kappa = 1.75$  gives an excellent fit for  $t_{ox} = 31$  and  $79 \text{ \AA}$  with  $N_p = 3 \times 10^{19} \text{ cm}^{-3}$  in both cases. This value of  $\kappa$  provides excellent fits to oxides varying from 25 to  $80 \text{ \AA}$  for various processes. For pMOS devices, the heavier hole effective mass means that there is less splitting in the energy levels and a value of  $\kappa = 1.0$  provides good fits.

### TED Modeling

Transient enhanced diffusion occurs due to the damage created by the implants and significantly enhances the diffusivity of the dopants during RTA or furnace anneal cycles. The TED simulations are done with TMA's version of SUPREM-IV using a fully coupled model for dopant diffusion and a scaled "+1" model to account for point defects created by the implant damage. The TED model uses published point defect coefficients [3] and scaled +1 parameters and is calibrated to fit the final profile motion for a range of 1D profiles. The simplicity of this model limits it to predicting only the total amount of profile motion and not the details of the time dependent evolution of the profile. Figure 3 shows how this TED model fits published data [3]. Figure 4 shows the tuned fit to a SIMS profile in the S/D regions of a  $0.35 \mu\text{m}$  technology, including the LDD implant. In the 2D simulations, the surface dopant segregation is treated as a fitting parameter based on the reasoning that it is unlikely that the default equilibrium boundary condition is instantaneously enforced for TED time scales [4]. The TED model dramatically changes the default doping contours to that seen in Figure 5. TED pushes boron towards the surface because of point defect gradients, thus increasing the threshold voltage [5],[6]. TED also moves dopant deeper into the bulk, reducing the body effect. In addition, the enhanced diffusion of the channel dopant allows it to reach the heavily doped S/D regions by E-field aided diffusion where it is trapped in the highly doped n-type regions. Overall the effect of TED is to deplete boron from the channel laterally adjacent to the S/D junction, to pile-up boron under the center of the channel and to move dopant deeper into the bulk.

Channel implants were varied from  $5 \times 10^{12} \text{ cm}^{-2}$  to  $1.4 \times 10^{13} \text{ cm}^{-2}$ , ranging from very lightly doped near the surface to heavily doped near the surface. The doping profiles predicted from the TED model were input to the device simulator. The same physical oxide thickness and active polysilicon doping extracted from the inversion region with QM corrections of the large area MOS structures are used in all the 2D MOSFET simulations. To verify the accuracy of the doping profile, C-V simulations were conducted for  $V_{bs}$  from 0 to  $-9.4 \text{ V}$ . As shown in Figure 6(a), the agreement between the simulation and measurement for various substrate bias is quite reasonable, for a  $0.35 \mu\text{m}$  gate length device. The TED and QM models work well for the range of devices tested. In Figure 6(b), the measured and simulated cross capacitances are shown, indicating that the decomposition of  $C_{gg}$  into the gate-to-channel component  $C_{gb}$  and the source/drain overlap component  $C_{gsd}$  is modeled correctly.

We also show that the DIBL effect is modeled correctly for this  $0.35 \mu\text{m}$  technology, for a range of substrate biases, as shown in Figure 7.

Finally, Figure 8 shows that this calibration methodology is extensible across technology generations, where we show that simulations based on the TED/QM model are capable of fitting the measured C-V curves on a  $0.21 \mu\text{m}$  device with a  $2.9 \text{ nm}$  gate oxide. The inclusion of arsenic dose loss during TED from the medium doped tip extensions needs to be accurately modeled to achieve the fits shown.

In conclusion, we have shown that the combination of QM and TED models can accurately model the full 2D C-V curves for deep submicron device structures, providing accurate 2D doping profiles. Device simulations using these doping profiles can predict the threshold voltage, body effect and DIBL characteristics for different gate lengths in a range of technology generations.

**Acknowledgment:** The authors would like to thank their colleagues Min Cao, Carlos Diaz, Wayne Greene, Malahat Tavassoli and the staff at the HP-ULSI fabrication facility.

### References

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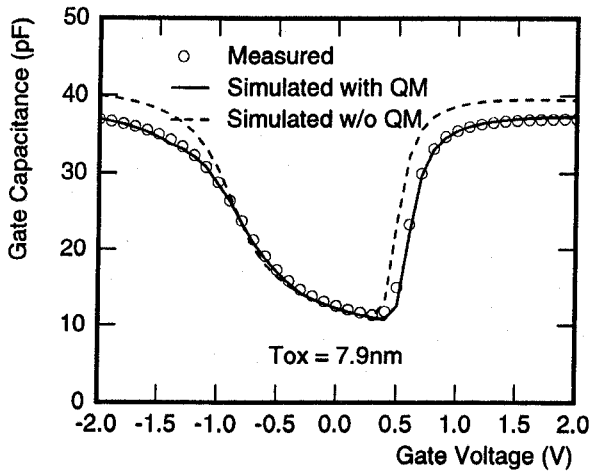
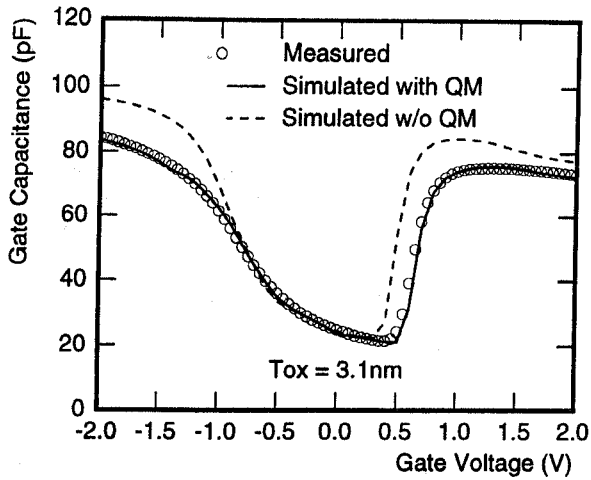


Figure 2: Measured and simulated gate capacitance ( $C_{gg}$ ) for large area ( $100 \times 100 \mu^2$ ) nMOS with gate oxides of 3.1 and 7.9 nm. The fit is excellent with the QM corrections but poor without.  $\kappa = 1.75$  is used for all the QM simulations.

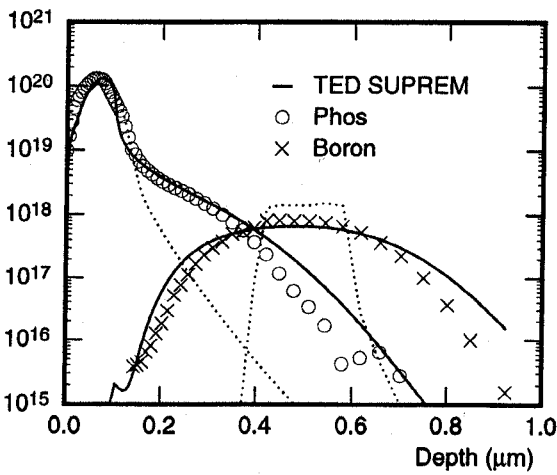


Figure 3: SIMS and calibrated SUPREM simulations for a 50keV,  $1 \times 10^{15} \text{ cm}^{-2}$  surface phosphorus implant and its effect on an epitaxial buried boron layer, after annealing for 2 hours at  $750^\circ\text{C}$ . TED effects cause a large, anomalous amount of profile motion (data taken from [3]).

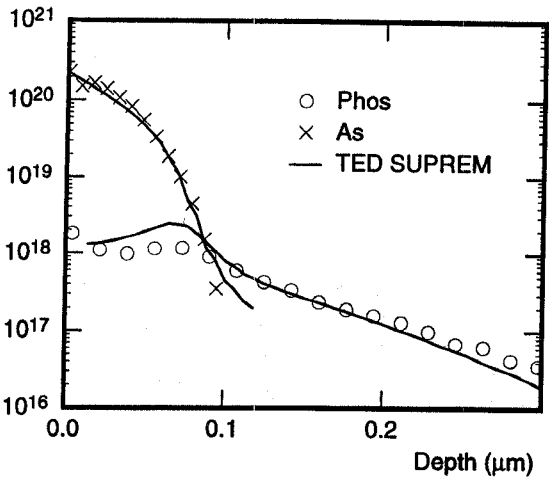


Figure 4: SIMS and calibrated TED SUPREM simulations for the source/drain/LDD region of the  $0.35 \mu\text{m}$  technology generation. The simulation is shifted to account for the consumption of silicon during the silicide growth.

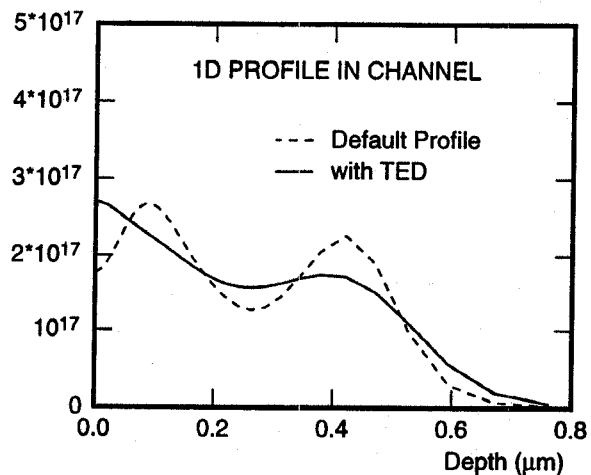
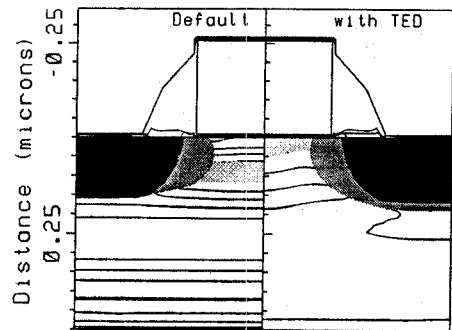


Figure 5: Simulated Boron Doping Profile for the  $0.35 \mu\text{m}$  device. (a) Boron contours with and w/o TED effects. The shaded region in the channel moves towards the surface under the influence of point defect gradients during TED. (b) Boron profile through the center of the channel, shown on a linear scale.

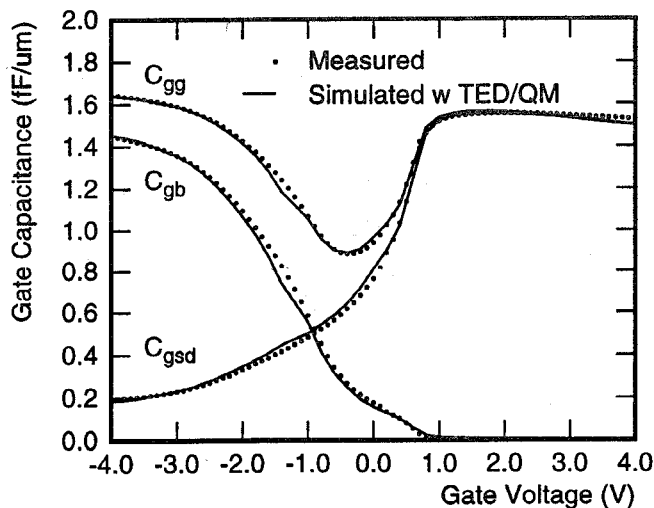
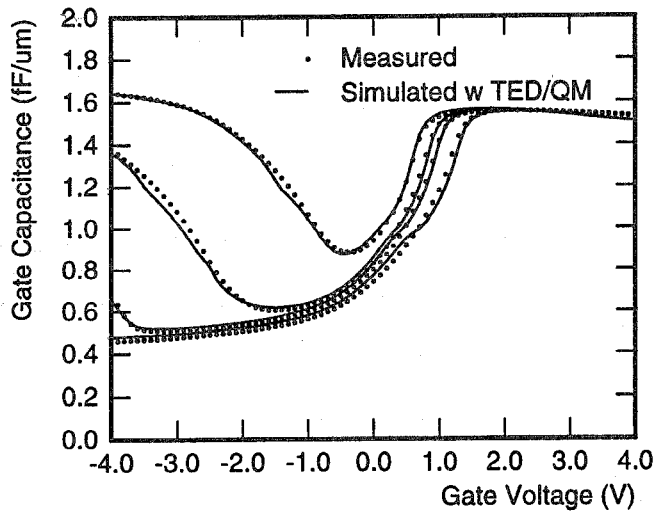


Figure 6: Measurement and TED/QM simulations for a  $0.35\mu\text{m}$  nMOS C-V curve (a)  $C_{gg}$  as a function of substrate bias  $V_{bs}=0, -1.6, -3.2$  and  $-9.4$  volts, to the same data shown in Fig. 1. (b) Decomposition of  $C_{gg}$  into  $C_{gb}$  and  $C_{gsd}$ . Each component of the gate capacitance is modeled correctly.

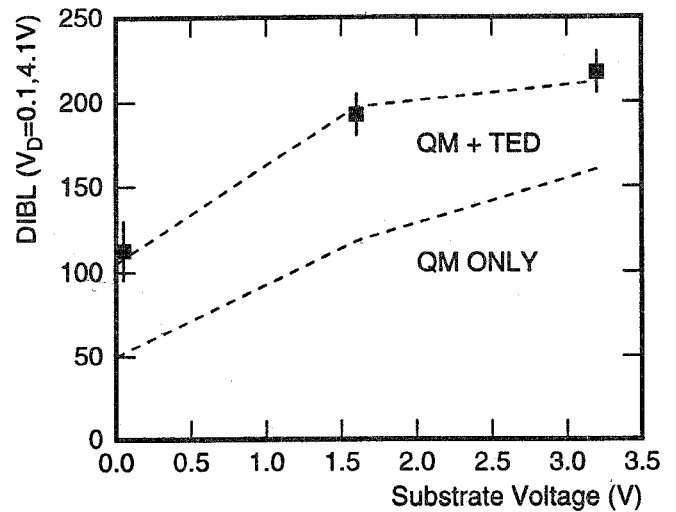


Figure 7: Measurements (solid symbols) and simulations (dashed lines) of Drain Induced Barrier Lowering (DIBL) for a  $0.35\mu\text{m}$  gate length device. The shift in the sub-threshold characteristic is measured when the drain voltage is changed from  $0.1\text{V}$  to  $4.1\text{V}$ , for a range of substrate voltages.

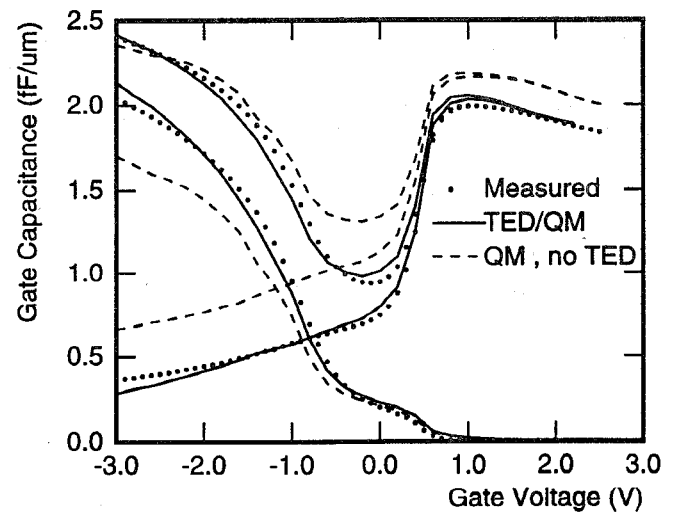


Figure 8: Extension of the calibration methodology to a  $0.21\mu\text{m}$  device with a  $2.9\text{nm}$  gate oxide. QM effects give the accumulation capacitance but without TED effects give a poor fit to the overlap and inversion regions. (dashed line). QM corrections, TED and dose loss during RTA provide an improved fit (solid line).