CHALLENGES IN PROCESS MODELING FOR MEMS

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The rapidly growing field of MEMS has created opportunities to merge new functional capabilities with integrated circuit (IC) electronics. MEMS fabrication uniquely requires accurate prediction of both geometry and materials dependencies that affect electrical, mechanical and other structurally constrained behavior.

I. INTRODUCTION

Computational prototyping of advanced VLSI technology has evolved rapidly, driven by aggressive targets for higher performance. This progress in TCAD for VLSI synergistically supports challenges that face the MEMS field. This paper presents results in support of process modeling for MEMS: geometric modeling, visualization, and physical models for deposition and etching.

II. GEOMETRIC MODELING

Figure 1 shows a 3D computational prototype of an RF switch fabricated with MEMS technology [1]. This model was created using a combination of 3D constructive computational geometry modeling [2] and surface extraction for both visualization and to generate a meshed surface representation. The level set algorithm allows a range of advanced physical models for deposition and etching to be incorporated into the simulations

The level set algorithms are implemented on an oct-tree grid as shown in Figure 2. The refinement (and de-refinement) features of tree-based gridding allows for local capture of process dependences, even down to atomic-scale features if needed [3]. Hence, numerical methods such as FEM and boundary movement algorithms can be formulated on the same static grid.

III. VISUALIZATION AND SUPPORTING ALGORITHMS

For FEM analysis, actual surface meshing of the final geometry is needed. The use of routines such as marching cubes for extraction of iso-surfaces provides a two-fold benefit: 1) it is useful as part of the visualization process and 2) it provides a means to capture and triangulate a mesh on the surfaces. Figure 3 shows both these capabilities in reference to modeling the RF switch.

IV. SIMULATION of DEPOSITION AND ETCHING

Modeling of IC technology has a long history in the area of VLSI bulk processing. For example, the SUPREM program provides capabilities to model 2D effects critical for device scaling. In the case of deposition and etching, especially for VLSI interconnect modeling, tools such as SPEEDIE [4] have demonstrated great potential in capturing the complexity of surface chemistry and associated effects from ion bombardment. For example, etching (chemical and sputtering) and deposition (inhibitor formation) occur simultaneously. Figure 4 shows a SPEEDIE simulation of etching silicon dioxide in high density plasma.

V. CONCLUSIONS

In summary, this paper shows recent progress in modeling complex MEMS devices from the perspective of structural definition (based on geometry modeling) and process simulation. The importance of feature-scale effects on MEMS behavior is also considered.

VI. ACKNOWLEDGEMENTS

The authors wish to thank DARPA for support under the Composite CAD Project (Contract # F30602-96-2-0308).

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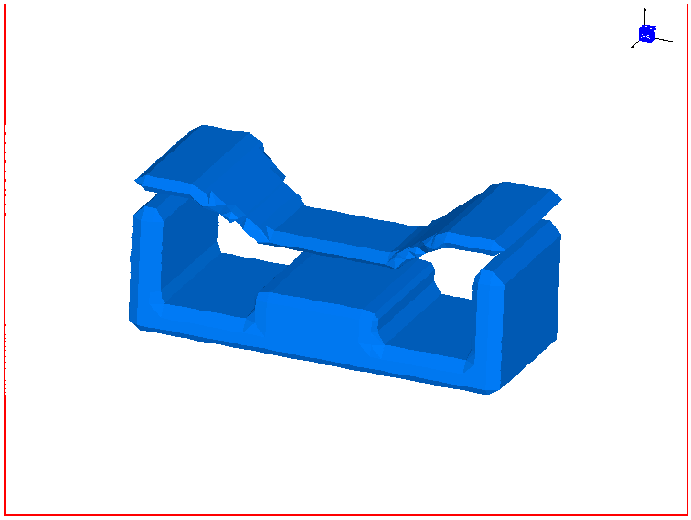

Figure 1: 3D computational prototype of an RF switch. An externally applied voltage deflects the top plate, as shown in the figure, and in turn modulates the capacitance across the air gap.

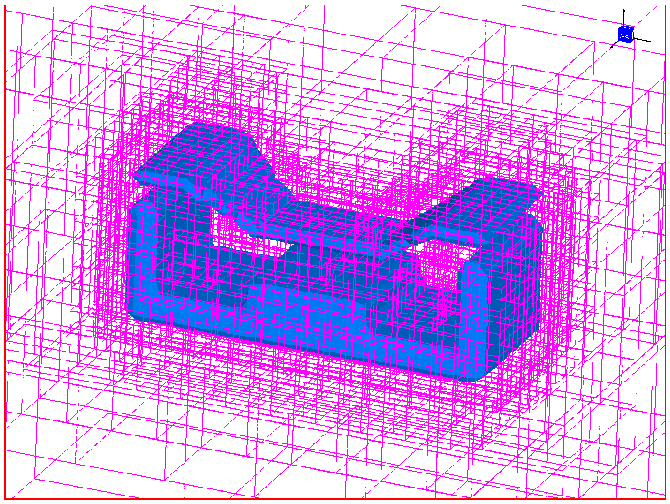

Figure 2: The oct-tree based level-set grid, from which the geometry in fig.1 is generated. The geometry is embedded in the grid. Each grid point holds a distance to the boundary of the geometry. Boundary movement can be performed on this grid using the level-set method.

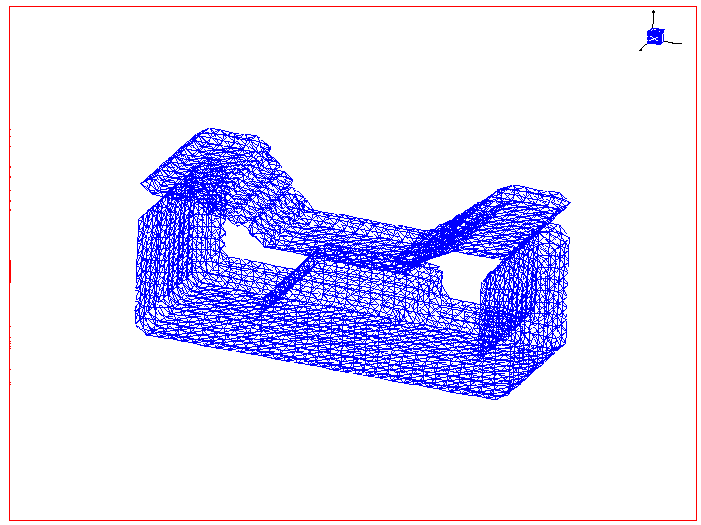

Figure 3: The triangular mesh generated from the level-set grid (fig. 2). The marching cube algorithm is used to extract the iso-distance surface. This mesh can be used for visualization and FEM simulation.

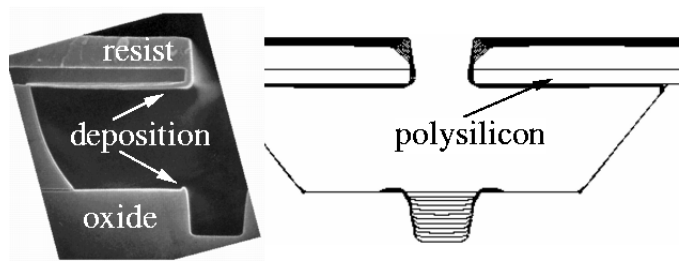

Figure 4: A SPEEDIE [4] simulation of etching silicon dioxide in high density plasma. Thin layers of inhibitor deposits on parts of the surface during etching. The physical model accounts for inter-structure radicals transport, ion sputtering, ion-assisted etching, and ion enhanced inhibitor deposition.