

## A Quasi-Mixed-Mode MOSFET Model for Simulation and Prediction of Substrate Resistance under ESD Stress and Layout Variations

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**Abstract** -- This paper presents a novel quasi-mixed-mode model for the computation of the varying substrate resistance during ESD stress. This model also predicts the change of substrate resistance with respect to layout variations. The model shows good agreement with experimental data, and has good convergence properties. This is the first time that a model has demonstrated accuracy in predicting the substrate resistance due to both ESD stress and layout changes.

### I. INTRODUCTION

Accurate modeling of substrate resistance is essential for the simulation and design of electrostatic discharge (ESD) protection circuits. The magnitude of substrate resistance reflects effects of layout changes (i.e. the geometries and substrate contact placement), and it also determines the turn-on of the parasitic bipolar transistor, which consists of the source, substrate, and drain ( $n^+ - p - n^+$  or  $p^+ - n - p^+$ ).

Experimental evidence suggests that the substrate resistance continues to change during ESD stress; hence, it has to be modeled as a dynamic device [1]. In the areas of compact modeling, previous works have modeled the substrate resistance as a current controlled voltage source,  $V_{sub} = R_{sub} \cdot I_{sub} - R_d \cdot (I_d - I_{ds})$ , where  $R_{sub}$  and  $R_d$  can be extracted from experimental data [2-3]. The compact model for simulating MOSFET breakdown, which includes the substrate current controlled voltage source, is shown in Figure 1. While such a current controlled model accurately captures the reduction of substrate resistance during ESD stress, it fails to predict the effects of layout variations because  $R_{sub}$  and  $R_d$  must be extracted again for each new layout [1]. Other authors have constructed substrate resistance networks to capture the effects of different geometries, but the reduction of substrate resistance during ESD stress is neglected [4-5].

After careful and extensive calibration, device simulators can simulate both the change of substrate resistance due to ESD stress and layout variations. However, the computation of impact ionization and the snapback portions of the ESD I-V curve often cause convergence problems. Moreover, these problems are compounded by the large size of ESD protection device; it becomes unstable and inefficient to use pure device simulator as an effective design tool [6].

Aiming to improve the existing substrate resistance model, this paper presents a novel quasi-mixed-mode approach that can accurately predict the substrate resistance using a device simulator, yet it is computationally stable and efficient. This report shall describe the quasi-mixed-mode model in the next section, and proceed to verify its results using both the full device simulation and experimental data in the following sections.

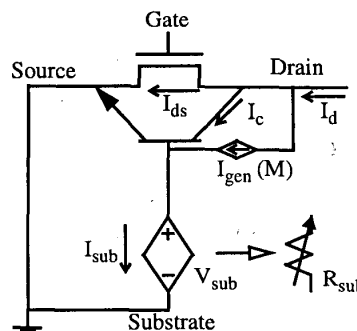


Figure 1. Compact model for simulating MOSFET breakdown uses substrate current controlled voltage source to represent changing  $R_{sub}$  during ESD stress.

### II. QUASI-MIXED-MODE APPROACH

The quasi-mixed-mode model is a marriage between device and circuit simulation. It differs from the traditional mixed-mode (device/circuit) simulation by not using a fully coupled matrix approach. Instead, the two simulators are not directly coupled; only the results of device simulation are fed into the circuit model, hence the adjective *quasi*.

The quasi-mixed-mode approach uses either the circuit or device simulator to model the lumped and distributed circuit elements accordingly. For a given technology, the process dependent parameters do not vary once extracted, so the physical effects can be modeled as lumped elements; hence, the impact ionization model (M) parameters are implemented directly in the compact model along with the parameters that govern normal MOSFET operation. On the other hand, the substrate resistance parameters tend to depend on layout; therefore, it is better suited to use distributed element modeling. The device simulator computes the substrate resistance based on layout. The compact model

takes the simulated substrate resistance, and simulates the resulting ESD I-V curve. In this manner, the quasi-mixed-mode model can be used as an effective tool in designing the optimal ESD devices without building and testing them on silicon.

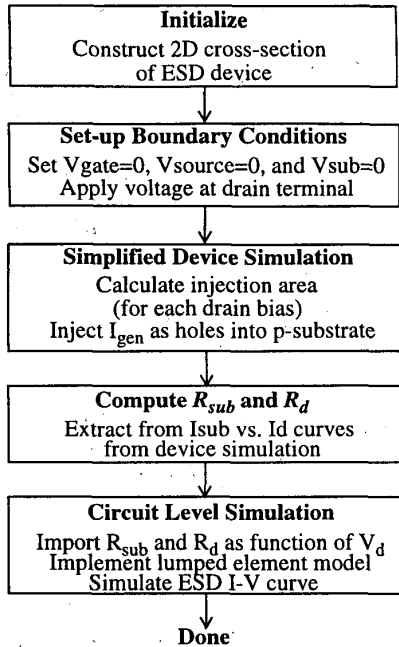


Figure 2. The flow diagram illustrates the system level set-up of the quasi-mixed-mode model.

The information flow of the quasi-mixed-mode model is described in Figure 2. To begin with, a 2D cross section of the ESD device is constructed using the device simulator. Then certain boundary conditions are imposed on the device that allow the holes to be injected into the silicon substrate. The placement of boundary conditions and the execution of device simulations are automated by using computer scripts. After running device simulations, a set of substrate current ( $I_{sub}$ ) vs. drain current curves ( $I_d$ ) under different drain bias are obtained. The values of substrate resistance parameters ( $R_{sub}$  and  $R_d$ ) can be extracted from these curves as a function of drain bias ( $V_d$ ), and imported into the compact model as  $V_{sub} = R_{sub}(V_d) \cdot I_{sub} - R_d(V_d) \cdot (I_d - I_{ds})$  for circuit level simulation. The compact model shown in Figure 1 is implemented inside the circuit simulator. The circuit parameters for normal MOSFET operation and impact ionization are already extracted from experimental data according to previously published research [2-4].

To avoid computational problems of traditional full ESD device simulation, the boundary conditions are set-up

to bypass the direct simulation of impact ionization. Thus the device simulation can be simplified to predict the substrate resistance with stability and speed.

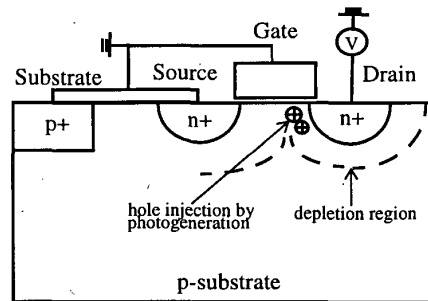


Figure 3. With the boundary conditions established, the full device simulation can be greatly simplified by using photogeneration function to replace hole generation by impact ionization. This corresponds to steps 2 and 3 of the flow diagram in Figure 2.

Figure 3 illustrates the placement of the boundary conditions on the ESD device. The gate, source, and substrate contacts are all tied to ground, and the drain terminal is biased to establish the corresponding electric field and depletion area. For each drain bias, a flux of holes are injected into the depletion region that has the highest electric field around the drain junction, much like the mechanism of hole generation by impact ionization. The hole injection is achieved using the photogeneration function. The entire process is equivalent to sweep the impact ionization current ( $I_{gen}$ ) under a constant drain voltage, then repeating it again under different drain bias. The  $I_{gen}$  is increased from zero until the turn-on of the parasitic BJT, and the device simulation is finished when the drain bias is increased to the avalanche breakdown voltage.

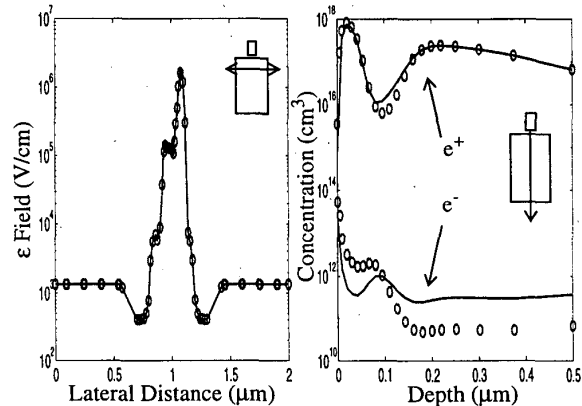


Figure 4. The electric field and electron/hole concentrations from the results of simplified device simulation (solid line) are compared to the results of the full device simulation (circled) at avalanche breakdown.

### III. VERIFICATION OF SIMPLIFIED DEVICE SIMULATION

The simplification of device simulation is a crucial step in the quasi-mixed-mode approach. Hence, it is important to verify that the hole injection by photogeneration can accurately approximate the hole generation by impact ionization. A  $0.25\mu\text{m}$  structure is constructed to compare the results of full device simulation against simplified device simulation. Since an electron/hole pair is generated due to impact ionization, the concentrations of holes and electrons before and after the turn-on of parasitic BJT are a good measure of the simplified method.

The avalanche breakdown and snapback voltages/currents ( $I_{\text{gen}}$ ) are obtained from the full device simulation, and the same drain voltages and  $I_{\text{gen}}$ s are applied to the simplified device simulation. The vertical electron/hole doping profiles and lateral electric field for the two simulations are plotted in Figures 4 and 5. The closely matched lateral electric fields indicate that the boundary conditions are placed correctly. The similar hole concentrations also demonstrate that the hole injection by photogeneration is an accurate approximation of hole generation by impact ionization. In addition, the sharp rise of electron concentrations after the snapback is also captured by the simplified device simulation.

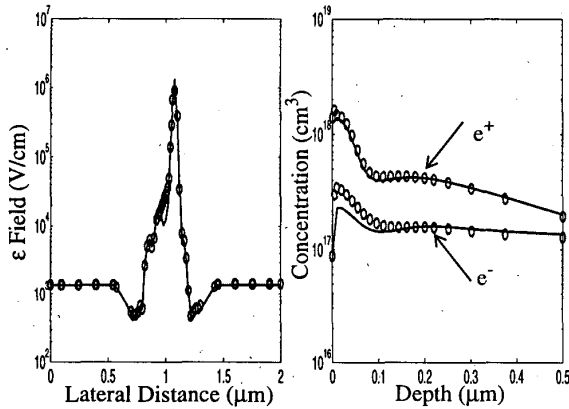


Figure 5. The electric field and electron/hole concentrations from the results of simplified device simulation (solid line) are compared to the results of the full device simulation (circled) at snapback.

### IV. APPLICATION OF QUASI-MIXED-MODE MODEL

After the verification of simplified device simulation, the quasi-mixed-mode model is applied to the modeling of on-chip ESD devices with layout variations. In this case, the ESD devices are AMD'S  $25\mu\text{m}/0.25\mu\text{m}$  and

$25\mu\text{m}/0.375\mu\text{m}$  NMOS devices with varying gate length and surface substrate contacts.

The device simulation is done using MEDICI, and the compact model is implemented in HSPICE. The automated script is written using PERL. Before applying the quasi-mixed-mode approach, the lumped elements (M and normal MOSFET parameters) are extracted from the experimental data of the  $0.25\mu\text{m}$  device, and implemented into the compact model [8]. Since the two devices are fabricated using the same process, the extracted compact parameters are also applicable for the  $0.375\mu\text{m}$  device.

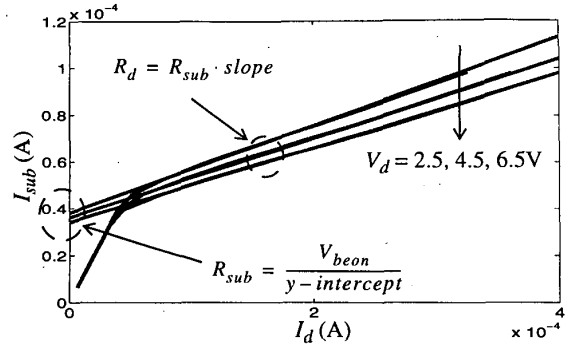


Figure 6. A set of  $I_{\text{sub}}$  vs.  $I_d$  curves are obtained under different drain biases. The  $R_{\text{sub}}$  and  $R_d$  values are extracted for each drain bias [2].

After setting-up the boundary conditions and performing the simplified device simulations, a family of  $I_{\text{sub}}$  vs.  $I_d$  curves at different drain bias is obtained as shown in Figure 6.

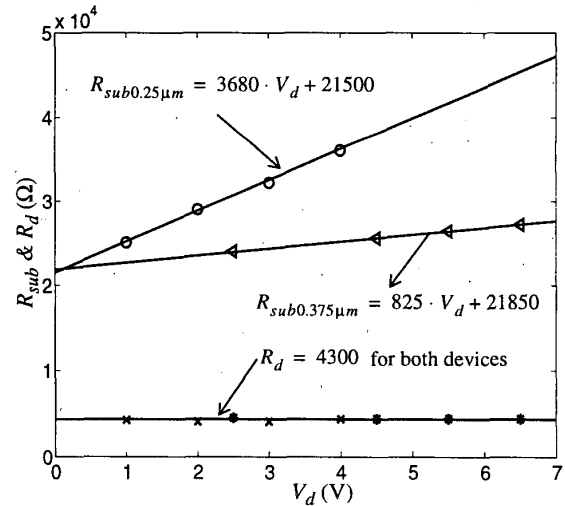


Figure 7. The dots are the extracted  $R_{\text{sub}}$  and  $R_d$  values from  $I_{\text{sub}}$  vs.  $I_d$  plots. The solid line is the linear approximation of the  $R_{\text{sub}}$  and  $R_d$  as a function of  $V_d$ .

The  $R_{sub}$  and  $R_d$  are extracted as a function of  $V_d$  for both devices as illustrated in Figure 7. In both cases, the  $R_{sub}$  parameter increases linearly with the drain bias, as approximated by the sloped line. The  $R_d$  parameter remains rather constant as approximated by the horizontal line. The  $R_{sub}$  of the 0.25 $\mu\text{m}$  device is larger than the 0.375 $\mu\text{m}$  device, and this difference is attributed to a bigger depletion area which is caused by a higher electric field inside the 0.25 $\mu\text{m}$  device. All of the above are evidenced in the larger  $R_{sub}$ - $V_d$  slope of the 0.25 $\mu\text{m}$  device. The similar y-intercepts of the two devices suggest that the two p-substrates are close in resistivity when the drain influence is small. The  $R_d$  values remained the same since the drain engineering is the same for both devices.

The equations that are listed in Figure 7 are implemented into the substrate current controlled voltage sources inside the compact models, which are then simulated with gate tied to ground. Comparison of the quasi-mixed-mode simulation results to experimental data are shown in Figure 8. Simulation results closely match the experimental data, indicating that the substrate resistance parameters are predicted correctly using the quasi-mixed-mode model.

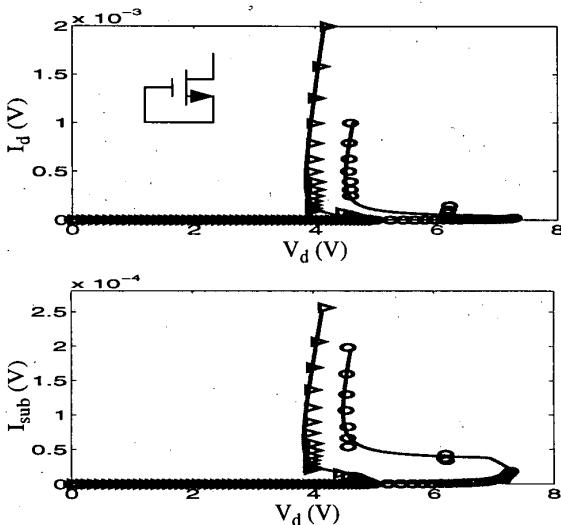


Figure 8. Comparison of quasi-mixed-mode simulation results (solid lines) to the experimental data (dotted lines), the measurements and simulations are both made with gate tied to the ground. The data with circles is taken from AMD's 25 $\mu\text{m}/0.25\mu\text{m}$  device, and the data with triangles is taken from AMD's 25 $\mu\text{m}/0.375\mu\text{m}$  device.

In this paper, all ESD simulations have been done with grounded gate; the compact model can easily simulate cases with gate bias above zero since all the compact parameters have been extracted. In addition, the compact parameters for the parasitic BJT can also be extracted from

the results of the simplified device simulations. The extraction procedures are detailed in previous researches [4,7].

By circumventing the simulation of impact ionization, the quasi-mixed-mode approach greatly improves the simulation speed as illustrated in Table 1. Moreover, the quasi-mixed-mode approach makes it easier to calibrate doping profiles.

Full Device Simulation MEDICI: 3052 nodes	37.26 min.
Quasi-Mixed-Mode Simulation MEDICI/HSPICE: 3052 nodes	16.5 min grid reduction: 5 min.
Circuit Level Simulation HSPICE: 1 ESD Device	3 sec.

Table 1. The quasi-mixed-mode simulation shows fifty percent speed improvement over full device simulation for the same number of nodes.

## V. CONCLUSION

The quasi-mixed-mode model has successfully predicted the changes of substrate resistance due to ESD stress and layout variations. Its robustness and efficiency makes it a effective tool for designing optimal ESD devices. It also can be easily expanded to compute substrate resistance for multi-finger devices and ESD I/O protection circuits. This is the first time that a technology oriented model has demonstrated accuracy in predicting the substrate resistance due to both ESD stress and layout changes.

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