2-3

Circuit Model for Power LDMOS including Quasi-Saturation

[a]Jaejune Jang, [b]Torkel Arnborg, [a]Zhiping Yu, and [a]Robert W. Dutton

[a]Center for Integrated Systems, Stanford University, CA 94304-4075, USA
[b]Ericsson Components AB, Kista S-164 81, Sweden

Abstract

This paper presents an analytical modeling of power LDMOS. The unique features of the LDMOS such as graded channel and quasi-saturation effect which results in a peculiar behavior on capacitance and non-linear LDD resistance are analyzed and modeled using an advanced device simulation.

1. Introduction

LDMOS (lateral double-diffused MOSFET) transistors are popular devices in such applications as motor control, switch-mode power supplies and telecommunication electronics. Optimal design of high-voltage integrated circuits requires physical LDMOS models implemented in a circuit simulator like SPICE. Several physically based models of LDMOST's have been developed[1]- [3], but a complete physical model is still lacking. This paper reports a detailed simulation study of the physical operation in terms of quasi-saturation behavior of a LDMOS device using PISCES. From the analysis, an analytical model is derived in conjuction with conventional SPICE MOSFET model.

2. Quasi-Saturation Effect of LDMOS and Its Modeling.

Consider LDMOS device as shown in Fig. 1. The device under study has the following characteristics. Under the gate oxide, a graded channel is formed by double diffusion technology. To sustain high voltage, lightly doped drift region between the active channel and the drain contact is necessary. For RF performance, source is tied to substrate.

A comparative study between MOSFET, MOSFET with a graded channel, and LDMOS device is done to analyze the effect of each region on device characteristic as shown in Fig. 2. Because of the existence of the drift region (LDD) the drain current tends to be saturated first not because of the pinch-off of the channel at the drain end, rather because of the velocity saturation in the LDD region for carriers from the channel. This so-called quasi-saturation phenomenon is unique for LDMOS (compared to other two types of MOS device) and gives rise to several interesting consequences. The major difference appears at high gate bias which affects drain current, and capacitance such as C_{DG} and C_{SG} as shown in Fig. 2. At high gate bias, drain current is dominated by current in drift region and at the onset of quasi-saturation as shown in Fig. 3, C_{DG} can be higher than total gate oxide capacitance due to change in surface potential in drift region goes negative

when there is a positive change in gate voltage [5]. The magnitude of peak of C_{DG} depends on the doping of LDD and V_{DS}. At quasi-saturation, the surface potential variation approaches zero which leads C_{SG} to approach the total gate oxide and C_{DG} to approach zero. Fig. 4 (at prequasi-saturation) and Fig. 5 (at quasi-saturation) show the distribution of lateral electric field and electron concentration along the channel and drift region for various drain bias. At prequasi-saturation, electric field peaks inside channel and at V_{DS} = 4.5V, drain current starts to saturate. However at quasi-saturation as in Fig 5, Electric field peaks inside drift region and the channel current is not saturated. By solving Poisson's equation along drift region using simulated electron concentration at quasi-saturation

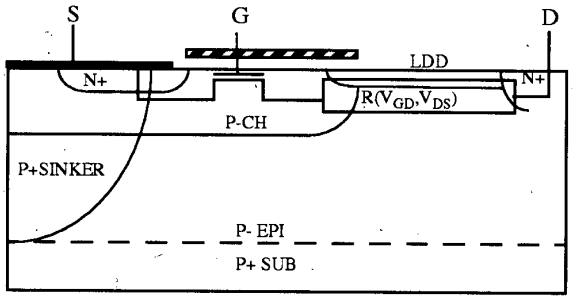


Fig 1. Unit-cell structure of the LDMOS transistor.

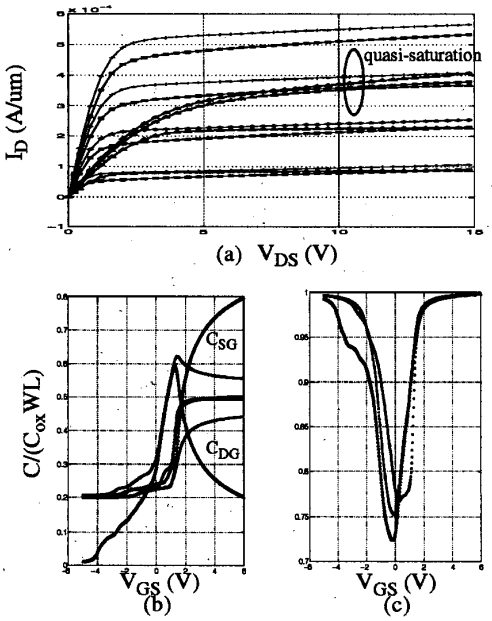


Fig 2. (a) I_D vs. V_{DS} when V_{GS} = 3V, 5V, 7V, and 9V, (b) C_{DG}, C_{SG} vs. V_{GS}, and (c) C_{GG} vs. V_{GS} curves for three different structures (LDMOS, MOS, MOS with graded channel).

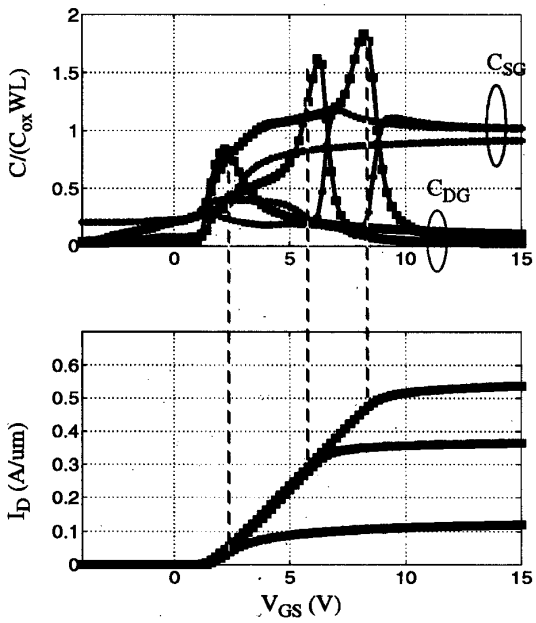


Fig 3. Normalized C_{DG}, C_{SG}, and the drain current versus V_{GS} for LDMOS device biased at V_{DS} = 1V, 8V, and 30V.

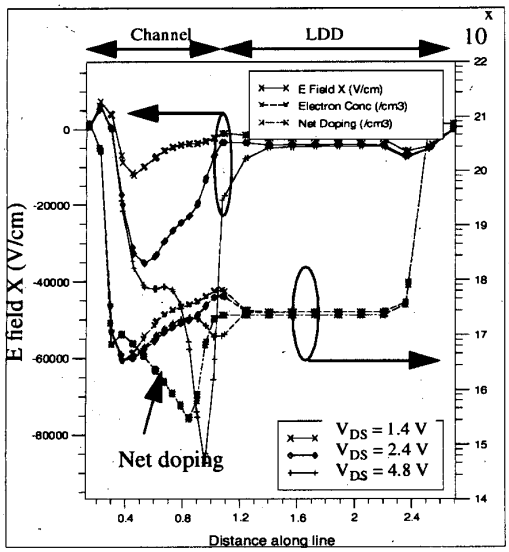


Fig 4. The distribution of lateral electric field, electron density, and net doping at V_{DS} = 1.2V, 2.4V, and 4.8V when V_{GS} = 3V.

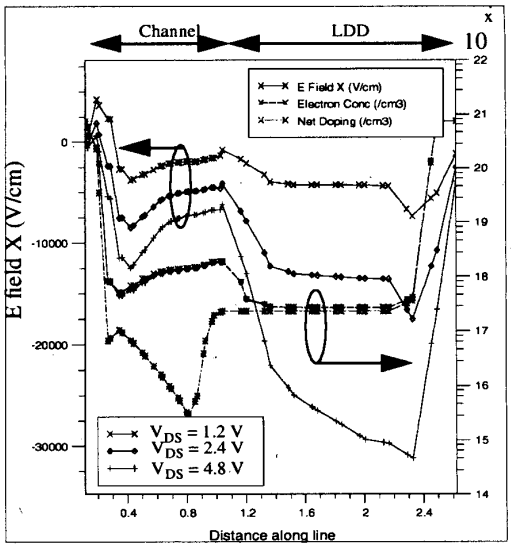


Fig 5. The distribution of lateral electric field, electron density, and net doping at V_{DS} = 1.2V, 2.4V, and 4.8V when V_{GS} = 9V.

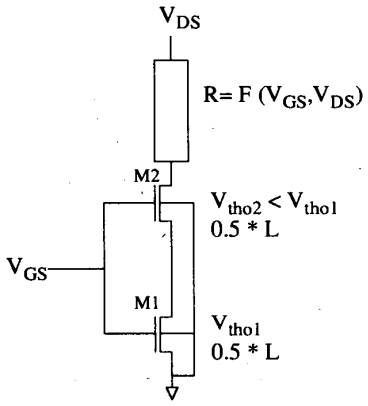
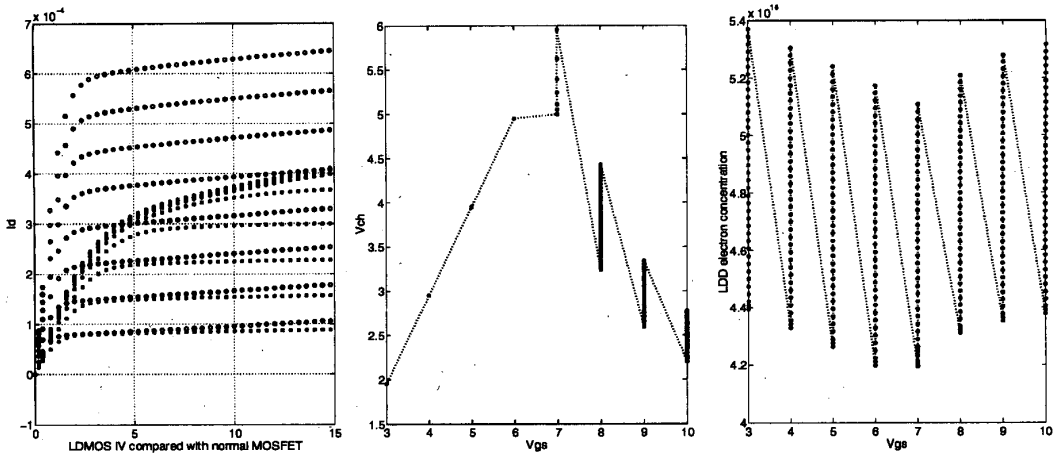


Fig 6. The large-signal equivalent circuit of the LDMOS device.

and by solving channel current equation, the non-linear resistive behavior of drift region is formulated. As shown in Fig 6, the channel region is modeled using multiple MOSFET devices with different channel doping to account for the effect of a graded channel and the drift region is modeled using non-linear resistor as a function of V_{GS} and V_{DS} to account for quasi-saturation behavior. The formulated non-linear resistive behavior is verified as shown in Fig 7. Fig 7(a) shows drain side channel voltage, V_{ch}, increases as V_{ds} increases and decreases as V_{gs} increases at quasi-saturation.



(a) (b) (c)

Fig 7. (a) V_{ds} vs. I_d between MOSFET and LDMOS. (b) Calculated V_{gs} vs. V_{ch} using LDMOS data as shown in (a). (c) Calculated V_{gs} vs. LDD electron concentration using LDMOS data as shown in (a). The calculation is valid at quasi-saturation ($V_{gs} > 6V$).

Fig 7(c) shows electrons in LDD increases as V_{gs} and V_{ds} increase. Above result agrees well with device simulation.

3. Acknowledgments

Support for this project came from Ericsson Components AB, Kista S-164 81, Sweden

References

[1] J. Victory, C. C. McAndrew, R. Thoma, K. Joardar, M. Kniffin, S. Merchant, and D. Moncoqut, "A Physically-Based Compact Model for LDMOS Transistors," SISPAD, pp. 270-274, 1998.

[2] Y.-S. Kim, J. G. Fossum, and R. K. Williams, "New Physical Insights and Models for High-Voltage LDMOST IC CAD," IEEE Trans. Electron Devices, vol.38, pp.1641-1649, July 1991.

[3] P. Perugupalli, M. Trivedi, K. Shenai, and S. K. Leong, "Modeling and Characterization of 80V LDMOSFET for RF Communications," Proc. IEEE BCTM, pp. 92-95, 1997

[4] C.-M. Liu, K.-H. Lou, and J. B. Kuo, "77K Versus 300 K Operation: The Quasi-Saturation Behavior of a DMOS Device and Its Fully Analytical Model," IEEE Trans., vol. 40, pp. 1636-1644, Sept. 1993.

[5] C.-M. Liu and J. Kuo, "Quasi-Saturation Capacitance Behavior of a DMOS Device," IEEE Trans., vol. 44, pp. 1117-1123, July 1997.