Impact of Substrate Resistance on Drain Current Noise in MOSFETs

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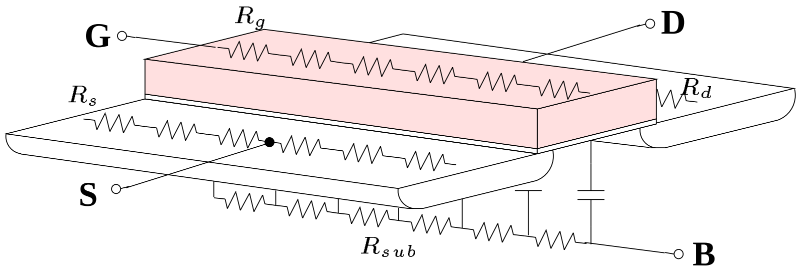
Outline

- Fundamentals
- Motivation
- Noise Model
- Simulation Results
- Discussion
- Conclusion

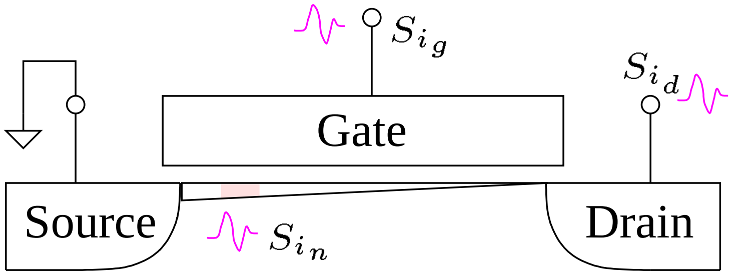
Fundamentals

(Noise in MOSFETs)

Parasitics



Intrinsic



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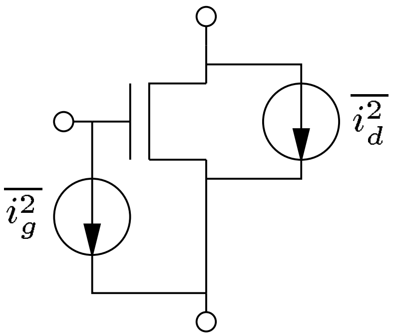
Fundamentals *(Continue)*

(van der Ziel's Long Channel Model)



$$\gamma = \frac{\overline{i_d^2}}{4\,k\,T\,\Delta f\,g_{d0}}$$

$$\delta = \frac{\overline{i_g^2}}{4\,k\,T\,\Delta f\,\Re[Y_{GS}]}$$

$$c = \frac{\overline{i_g i_d^*}}{\sqrt{\overline{i_g^2}\,\overline{i_d^2}}}$$

Classical Values

$\gamma = 1.0$ (Linear)
$= 2/3$ (Saturation)
$\delta = 4/3$ (Saturation)
$c = j0.395$ (Saturation)

Concerns

❖ Intrinsic noise exhibit larger γ and δ in short channel.

❖ Amount of increase is quantitatively still controversial.

❖ No physical explanation available yet.

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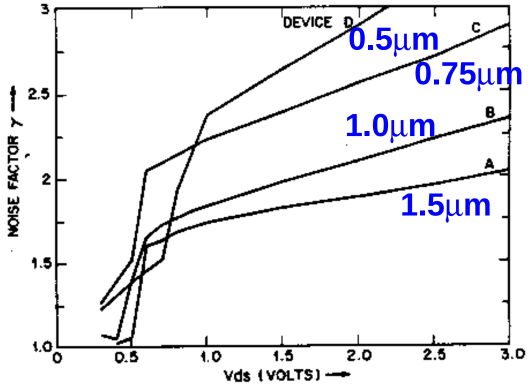
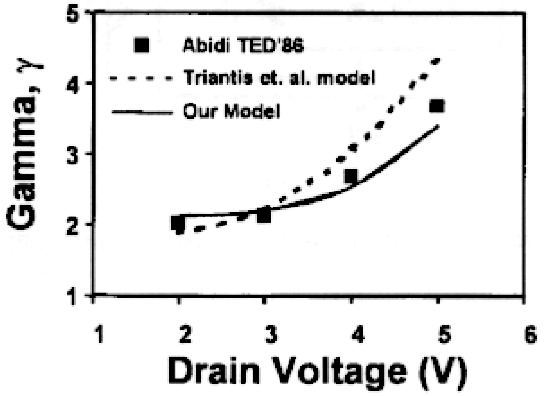
Motivation

(Excess Noise in Short Channel MOSFETs)

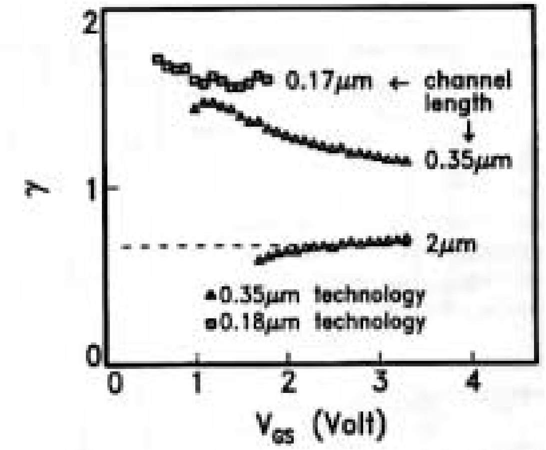
- ❖ Amount of γ increse largely varies, case by case.
- ❖ Very large γ : low f (<100MHz) and old technology.



R.P. Jindal (*IEEE T-ED*, 1986)



T. Manku(*IEEE JSSC*, 1999)



A.J. Scholten (*IEDM*, 1999)

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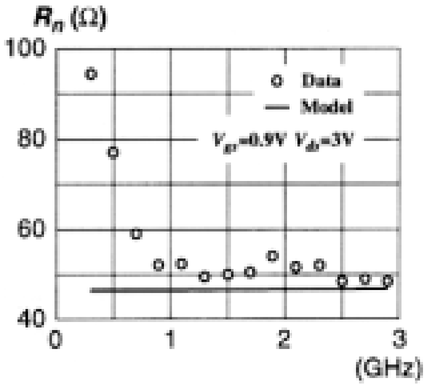
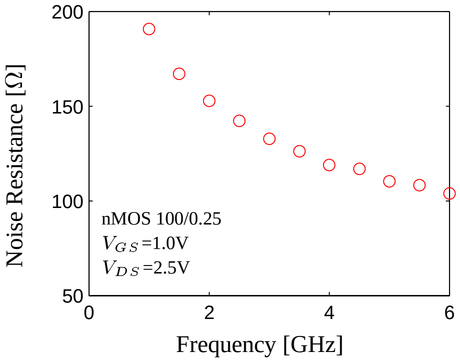
Motivation *(Continue)*

(Noise Spectrum)

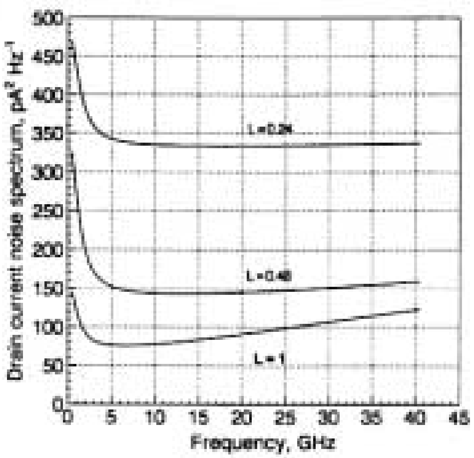
- ❖ Frequency dependence of R_n at a few GHz.
- ❖ A simulation study suggested a frequency dependence.



J. J. Ou (*Symp. VLSI Tech.*, 1999)



National CMOS8



S. Donati (*IEDM*, 1998)

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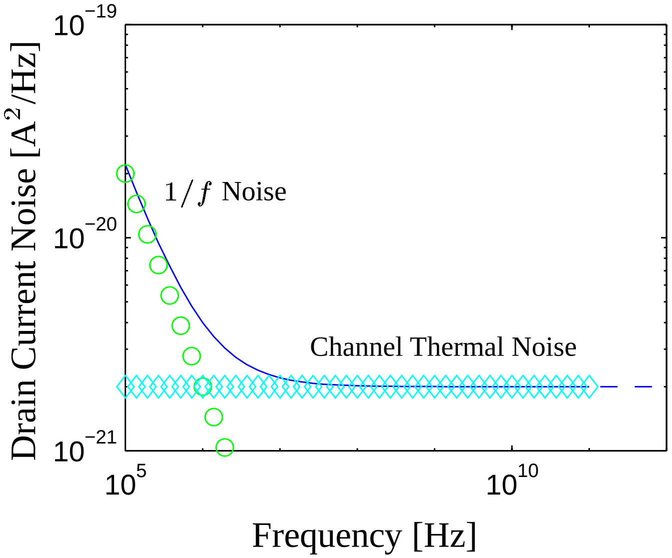
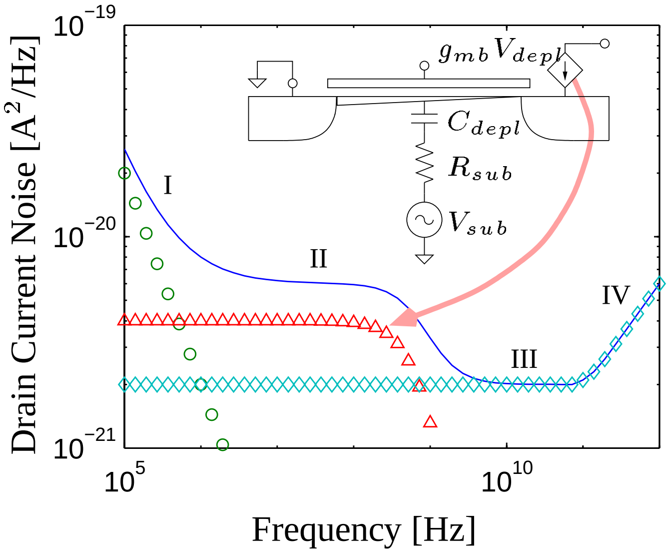
Motivation *(Continue)*

(Drain Current Noise Spectrum)

Commonly Assumed



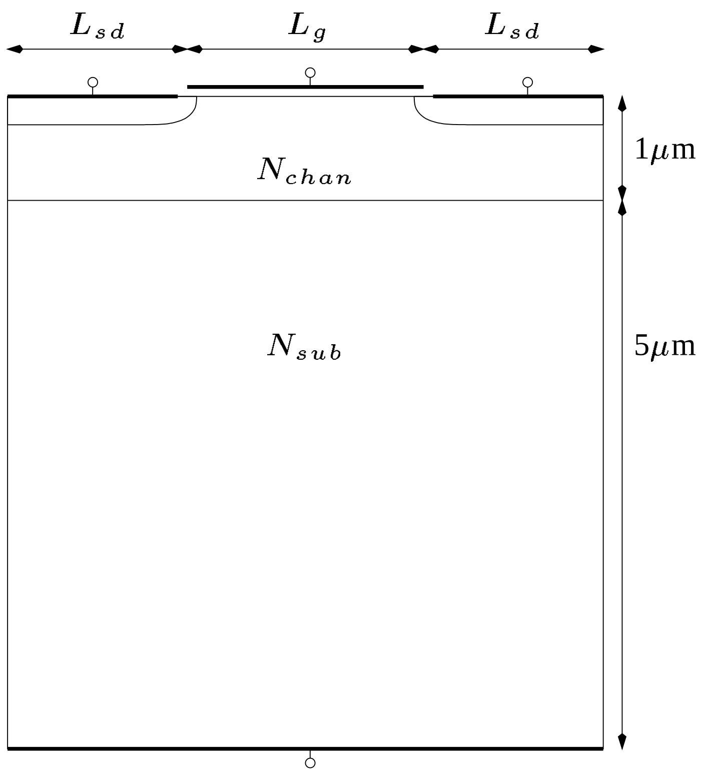
Proposed



$$S_{i_d,sub} = \frac{4kTR_{sub}g_{mb}^2}{1+(\omega R_{sub}C_{depl})^2}$$

Noise Simulation

(Structure)

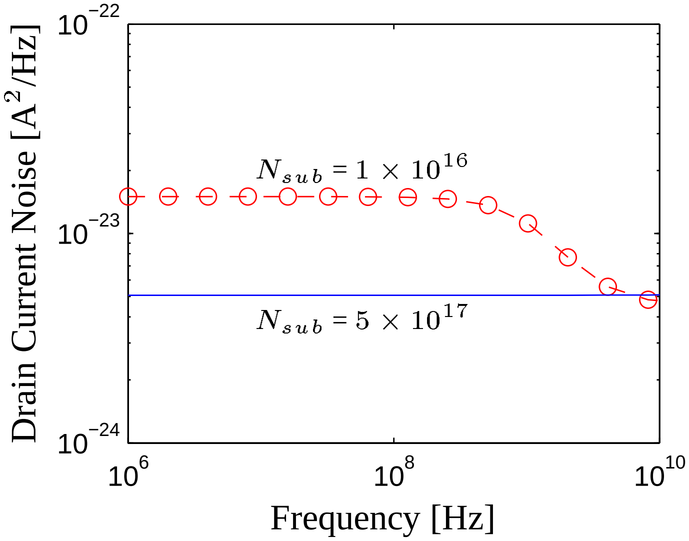


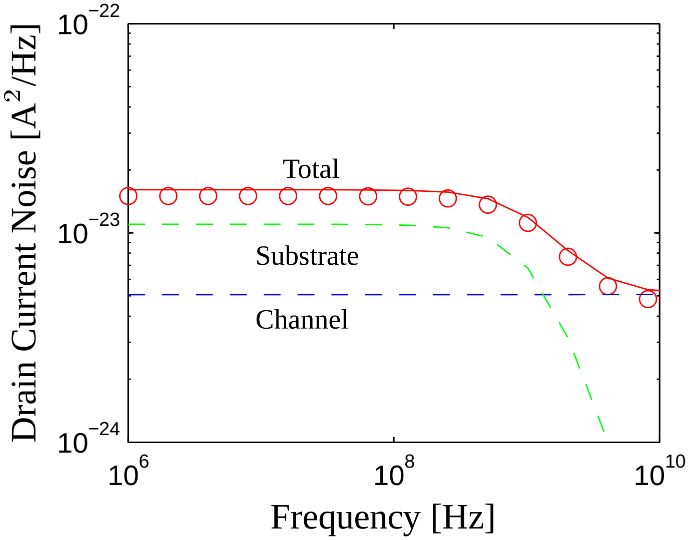
Simulation

- ❖ Lucent PADRE
- ❖ Full 2D noise simulation
- ❖ Drift-diffusion model
- ❖ Simplified structure
- ❖ Change Substrate Doping
  - ✧ $N_{sub} = N_{chan}$
  - ✧ $N_{sub} << N_{chan}$

Simulation Results *(Continue)*

(Impact on Spectrum)





- Drain current noise is increased by a substrate induced component at low frequencies.

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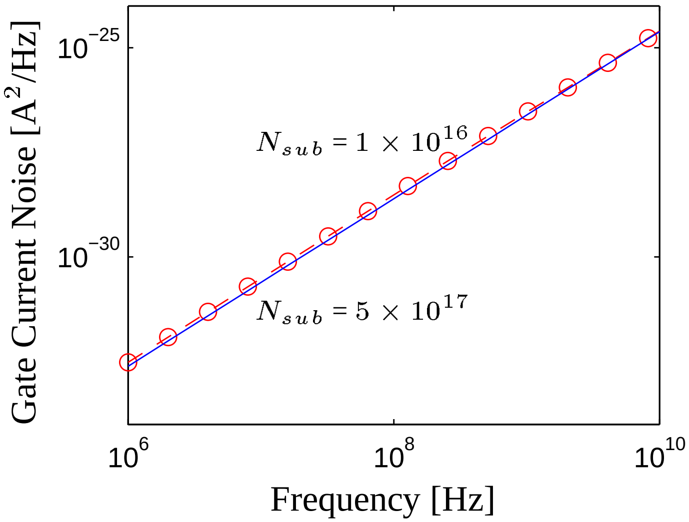
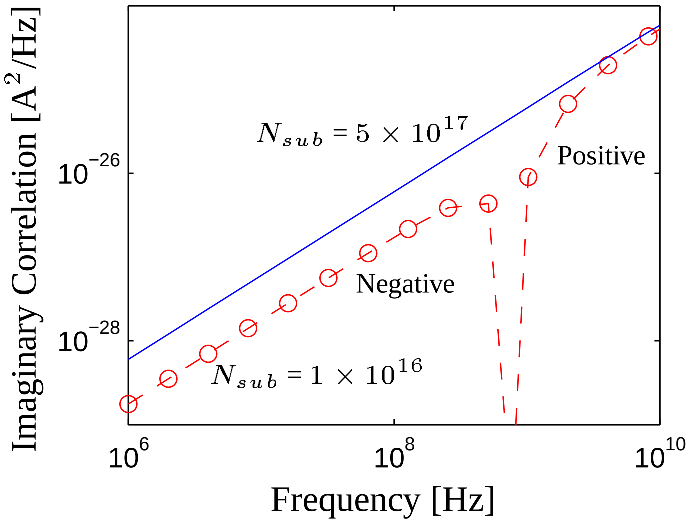
$$S_{i_d,sub} = \frac{4kTR_{sub}g_{mb}^2}{1+(\omega R_{sub}C_{depl})^2}$$

Simulation Results *(Continue)*

(Impact on Spectrum)

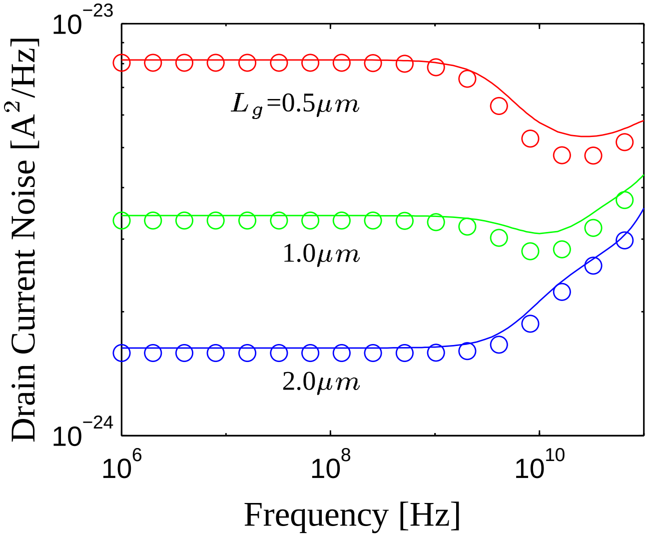


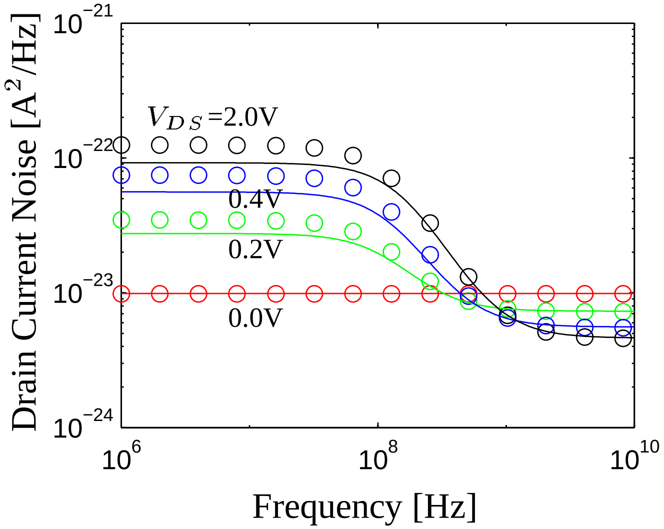


- ❖ Negligible increase of induced gate noise.
- ❖ Correlation between drain and gate noise is degraded.

Simulation Results *(Continue)*

(Length & Bias Dependence)





- ❖ Shorter device shows more impact.
- ❖ Higher drain bias leads to larger contribution.

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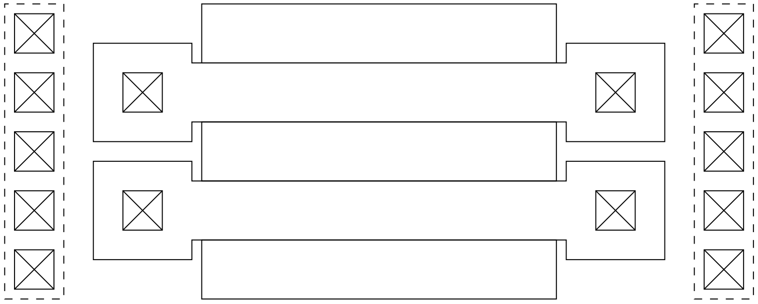
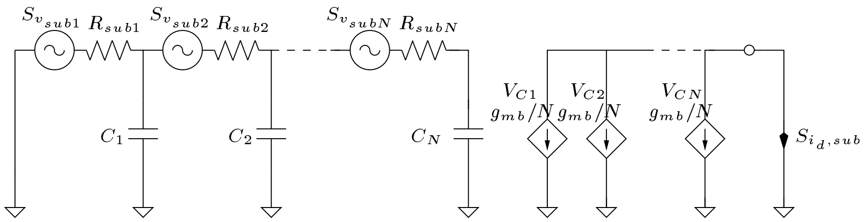
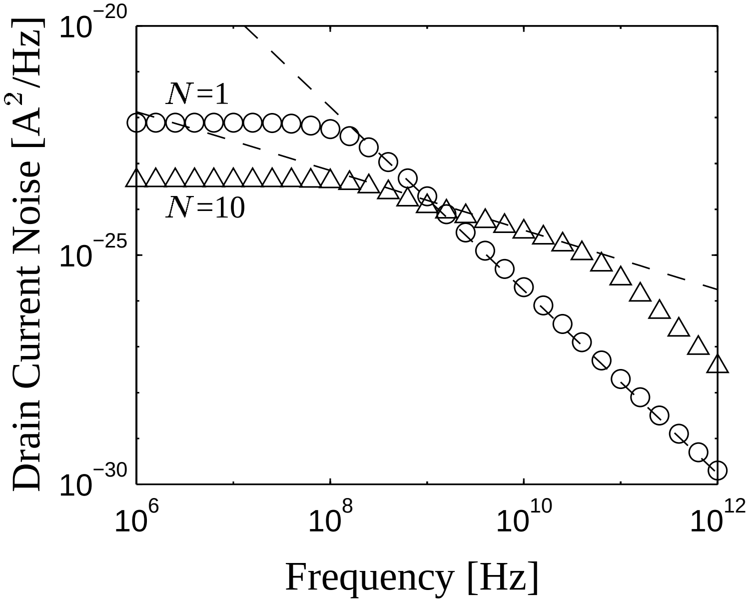
Simulation Results *(Continue)*

(3D Distributed Effect)







- Multiple components with different poles, due to distributed *RC.*
- Typical slope is below -5dB/dec.

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Discussion

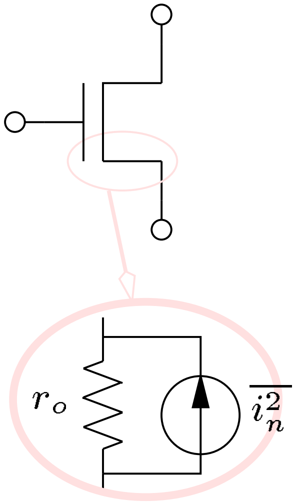
(Impact of Substrate Component)

- Match the description of excess noise.
- Uncorrelated with induced gate noise.
- May exaggerate γ at low f.
- Subject to layout and well profile.

Discussion *(Continue)*

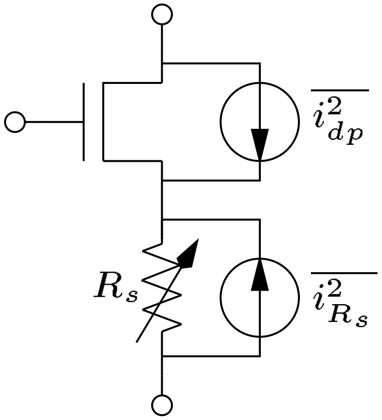
(Channel Noise Modeling Approach)

Physical Simulation



- High ac resistance r_o near source junction causes excess noise.

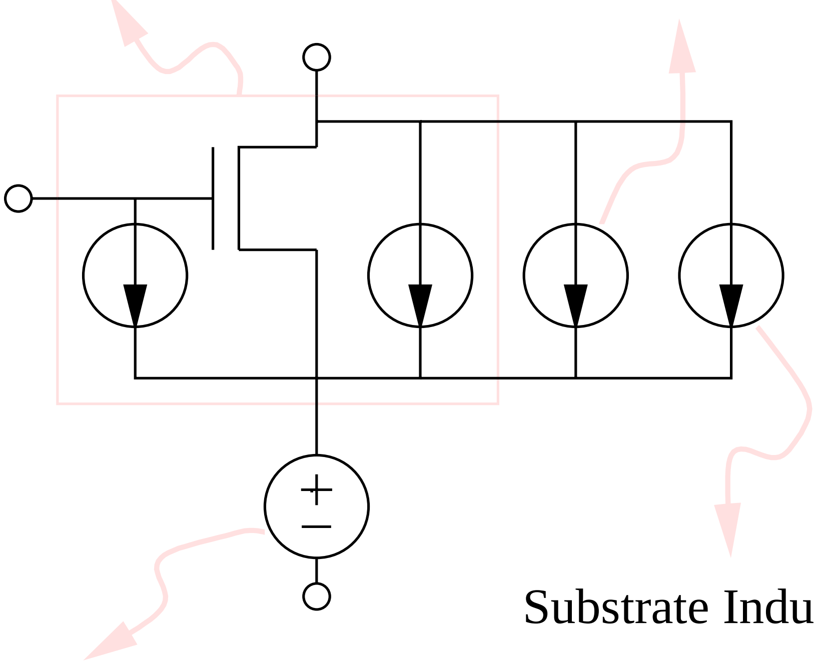
BSIM4 Implementation



- Capture excess noise by adjusting source side extra resistance R_s.

Discussion *(Continue)*

(Physical Noise Sources in MOSFETs)



Classical van der Ziel Model

$1/f$ Noise

Substrate Induced Noise

Excess Noise (BSIM4)

Conclusions

- Substrate induced noise has length and bias dependences.
- It may result in a frequency dependence in drain noise spectrum. -> exaggerate γ at low f.
- Prediction is a challenging issue due to 3D effects.
- Deep well doping profile can suppress this component.

Acknowledgment

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  - Dr. Mark R. Pinto, Dr. Conor Rafferty, and Dr. Muhamad A. Alam
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  - Dr. Keith R. Green and Dr. William Liu