RF LDMOS Characterization and Its Compact Modeling

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Abstract *-- This paper presents characterization of power LDMOS using device simulation and analytical modeling. Features of the LDMOS such as graded channel and quasi-saturation effect which result in a peculiar behavior on capacitance and non-linear LDD resistance are analyzed and modeled using device simulation. A compact model for LDMOS is implemented in HSPICE based on additional lumped elements, combined with the BSIM3 MOSFET model.*

I. INTRODUCTION

Broad deployment of wireless communications has created a demand for cost effective, linear, high-gain RF power transistors for application in base station power amplifiers. Peak power requirements from such amplifiers can be as high as 120 Watts in single carrier applications, operating from a 24-28 Volt power supply. Silicon technology has evolved to meet these needs, especially the development of sub-micron LDMOS. Optimal design of RF power amplifiers requires physical LDMOS models implemented in a circuit simulator. Several LDMOS models have been developed [1]-[3], but a complete physical model is still lacking such as a non-linear r_d in the small signal model. This paper reports a detailed simulation study of the operation that includes quasi-saturation behavior of a LDMOS device. From the characterization and analysis, an analytical model is derived in conjuction with conventional SPICE MOSFET model.

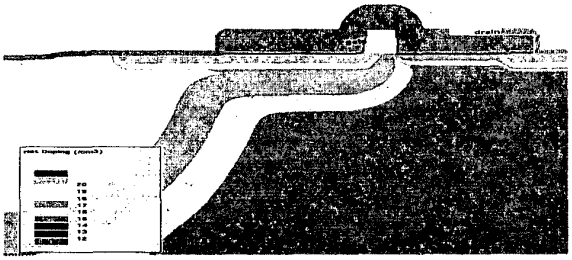

Fig. 1. Cross section of the LDMOS from process simulation.

II. MODELING OF LDMOS USING DEVICE SIMULATION

A device structure for simulation (shown in Fig.1) was created using process simulation that includes the actual process details used for fabrication. The device simulation was then used to reproduce the measurement DC characteristics.

Minor changes in the doping profiles within reasonable variation in fabrication process such as lateral diffusivity for p^+ graded channel and drift region were necessary to obtain good agreement between the measured and simulated value of V_{th} (4.3V). Modeling of the intrinsic device focuses on selecting an appropriate combination of physical models that represent the physics in the device. The mobility formulation and parameter choices are the single most important model that affect accuracy. The Lombardi model is selected because it provides excellent modeling of the inversion layer in MOSFET's [12]. First, the transverse mobility parameters mainly related to surface scattering are calibrated at low drain bias throughout the gate bias range as shown in Fig. 2 (a). Second, longitudal mobility parameters mainly related to velocity saturation are calibrated at high drain bias as shown in Fig. 2 (b). Fig. 2 (c) shows comparison between measurements and device simulation for I_{ds} vs. V_{ds}. The deviation at high gate bias and negative resistance originates from self heating. A thermal model is currently under development to include these effects [4].

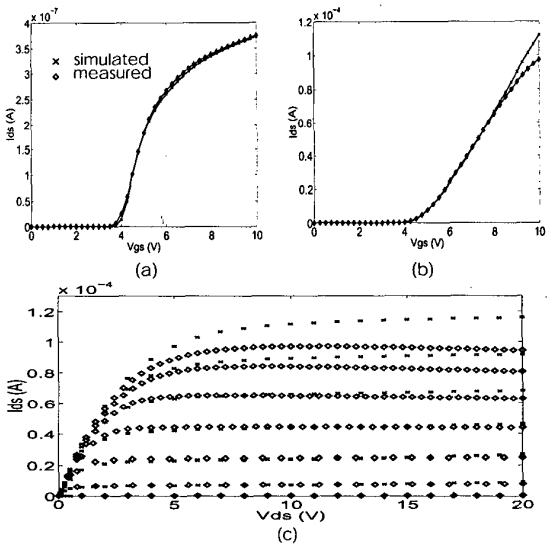

Fig. 2. Comparison between measurements and device simulation. (a) I_{DS} vs. V_{GS} at V_{DS} = 0.01V. (b) I_{DS} vs. V_{GS} at V_{DS} = 10.0V. (c) I_{DS} vs. V_{DS} for V_{GS} = 4-10V.

III. MODELING OF QUASI-SATURATION IN LDMOS

High voltage LDMOS transistors exhibit a limitation in the current level that can be attained. This is manifested in the high output conductance and the insensitivity to the increase in the gate voltage at high current levels as shown in Fig. 3. It has been shown that this effect results from carrier velocity saturation induced by the high electric field, as well

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as low impurity concentration in the drift layer [5].

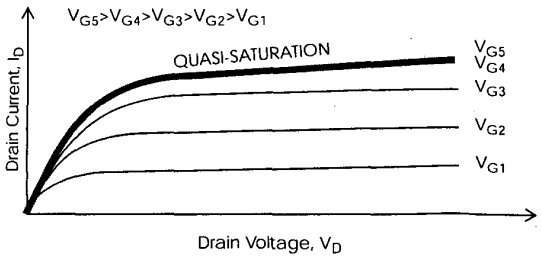

Fig. 3. Quasi-saturation of LDMOS device.

To understand the underlying physics in detail, device simulation is performed using the LDMOS structure. Fig. 4 (at pre quasi-saturation) and Fig. 5 (at quasi-saturation) show the distribution of lateral electric field along the channel and in the drift region for several drain bias values. At pre quasi-saturation (V_{GS}=3V), the electric field peaks inside the channel region and at V_{DS} = 4.8V, drain current starts to saturate. However at quasi-saturation (V_{GS}=9V) as shown in Fig 5, the electric field peaks inside drift region and the channel current is not saturated. Also drain side channel voltage, Ψch, (V_{DS}=4.8V) decreases from 3.8V to 1.2V when V_{GS} increases from 3V to 9V. The Ψch drop when V_{GS} increases explains capacitance peaking of C_{dg} greater than total gate capacitance [6,7].

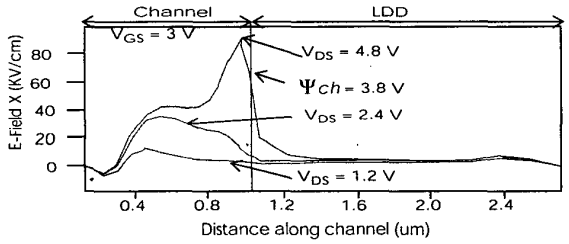

Fig. 4. E-field along channel and LDD at pre quasi-saturation.

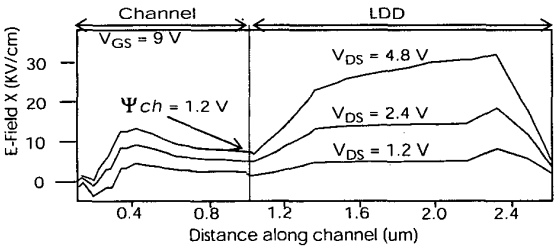

Fig. 5. E-field along channel and LDD at quasi-saturation.

By solving Poisson's equation along the drift region, using the simulated electron concentration values at quasi-saturation, including the channel current equation, the non-linear resistive behavior of drift region is formulated as below. The drain side channel voltage is expressed as a function of V_{GS} and V_{DS} as follows [7]:

$$\Psi ch = V_{GS} - V_{TS} + \frac{1}{BC} - \sqrt{\left(V_{GS} - V_{TS} + \frac{1}{BC}\right)^2 - \frac{2(V_{DS}+A)}{BC}} \quad (1)$$

where,

$$A = \frac{q}{2\varepsilon}N_D[L_d^2 - L_j^2] + q\frac{k}{3\varepsilon}L_j^3 + q\frac{k}{2\varepsilon}L_j^2 L_d + \frac{q}{\varepsilon}N_D L_j(L_d + L_j)$$

$$B = \frac{q}{2\varepsilon}(L_d^2 - L_j^2) + \frac{q}{\varepsilon}L_j(L_d + L_j),\ C = \frac{\mu C_{ox}}{q l v_s l_s}$$

N_D denotes doping concentration in the LDD region, and k, L_j, L_d, l, and l_s are geometry parameters of the channel and the LDD regions, respectively . Fig. 6 shows the behavior in the quasi-saturation region using the equation (1). When the gate bias increases, the drain side channel voltage decreases for the same drain bias, which means that current is limited by velocity saturation in drift region.

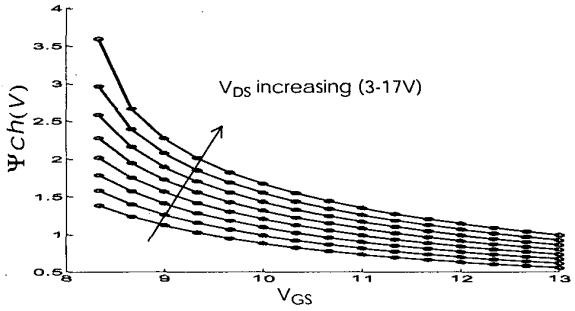

Fig. 6. Drain side Channel voltage vs. V_{GS} for V_{DS} (3-17V, step = 2V) using analytical equation given in (1).

IV. LARGE-SIGNAL MODEL

From a comparative study between LDMOS and MOSFET [7], the channel region is modeled using two MOSFET devices with different channel doping to account for the effect of a graded channel and the drift region is modeled using a non-linear resistor as a function of V_{GS} and V_{DS} to account for the quasi-saturation behavior as shown in Fig. 7.

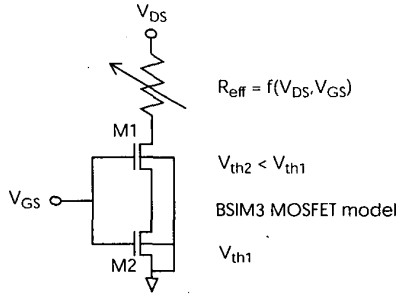

Fig. 7. Large-signal equivalent circuit of the LDMOS.

Using equation (1) and device simulation, an effective resistive value is extracted as shown in Fig. 8. For increasing gate bias the non-linear behavior of the LDD region increases. At

low gate bias, the LDD region shows a small bias dependence but the resistance increases with V_{DS}, due to reduction of the effective conduction area owing to depletion between the bulk and LDD region.

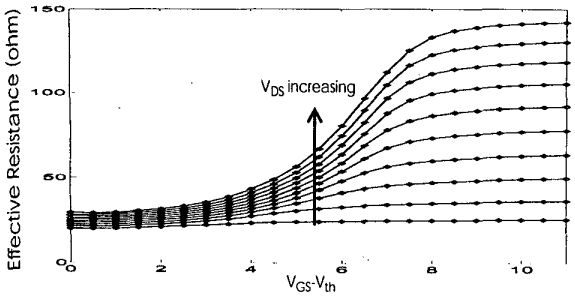

Fig. 8. Effective resistance vs. V_{GS}-V_{th} of LDD for V_{DS} (2-20V, step =2).

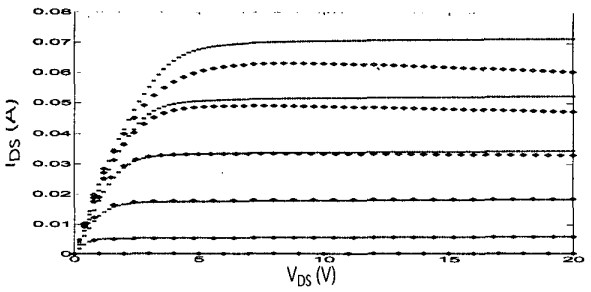

Fig. 9. Comparison between measured and SPICE simulated I_{DS} vs. V_{DS} for V_{GS} = 4 - 9V (o: measured, -: simulated).

To model this DC characteristics in SPICE, low gate and low drain bias region is first calibrated using measurements since in those regions the non-linear behavior of the LDD region is negligible. After calibration, the non-linear resistor is implemented using a voltage controlled resistor in SPICE. Fig. 9 shows a comparison between measurements and SPICE BSIM3 simulation. Again, at high gate bias, measurements are influenced by self-heating effects.

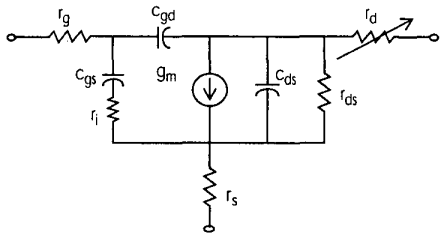

Fig. 10. Silicon LDMOS small-signal equivalent model.

V. SMALL-SIGNAL MODEL

Fig. 10 shows the schematic of the equivalent model used to characterize the small-signal behavior of the LDMOS. Unlike the MOSFET equivalent model [8-11], r_d is not a constant for the LDMOS as evidenced by Fig. 8. Therefore r_d was taken from device simulation as described in the previous section. Owing to capacitive coupling between gate and channel at high frequency, part of the channel conductance is present as a resistance (r_i) in series with the gate input capacitance. The parasitic resistor model parameters (r_g, r_d and r_s) were extracted through the use of a set of S-parameters of a device biased at V_{GS}=V_{DS}=0V [8]. This bias condition causes the contribution of the voltage dependent current generator (g_m) used in the model to become zero and maximizes the drain-source capacitance (c_{ds}) and the output resistance (r_{ds}). Channel resistance (r_i) is also ignored due to the absence of channel charge. A schematic of the zero bias equivalent circuit [8] is shown in Fig. 11. The Fig. 12 shows the values of r_g, r_s, and r_d extracted by this technique.

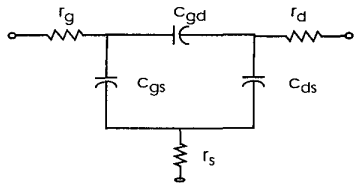

Fig. 11. Zero bias small-signal equivalent circuit.

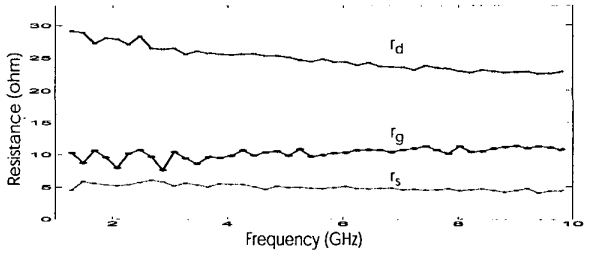

Fig. 12. Extracted r_g, r_s, and r_d vs. frequency at V_{DS}=V_{GS}=0.

With knowledge of the parasitic resistance parameters (r_g, r_d, and r_s), the intrinsic model can be determined. The intrinsic model z-parameters of the intrinsic model shown in Fig. 10 are:

$$Z'11 = Z11 - (rg + rs)$$
$$Z'12 = Z12 - rs$$
$$Z'21 = Z21 - rs$$
$$Z'22 = Z22 - (rd(V_G, V_D) + rs)$$

where Z is the z-parameter network of the device under bias conditions and Z' is the z-parameter network describing the intrinsic model. Here r_d is expressed as a function of both V_G and V_D as described in Fig. 8.

From the above Z' network, y-parameters (Y') can be generated by a simple conversion. The intrinsic y'-parameter network can be expressed as a function of the following small-signal model parameters [9]:

$$Y'11 = \frac{r_i Cgs^2 \omega^2}{D} + j\omega\left(\frac{Cgs}{D} + Cgd\right) \quad (2)$$

$$Y'12 = -j\omega Cgd \quad (3)$$

$$Y'21 = \frac{g_m e^{-j\omega\tau}}{1 + jwr_i Cgs} - j\omega Cgd \quad (4)$$

$$Y'22 = \frac{1}{rds} + j\omega(Cds + Cgd) \qquad (5)$$

where

$$D = 1 + \omega^2 Cgs^2 r_i^2 \qquad (6)$$

Separating (2) through (6) into their real and imaginary parts, the elements of the small-signal equivalent circuit can be determined analytically as follows [11]:

$$Cgd = \frac{-Im(Y'12)}{\omega}$$

$$Cgs = \frac{Im(Y'11) - \omega Cgd}{\omega}\left(1 + \frac{(Re(Y'11))^2}{(Im(Y'11) - \omega Cgd)^2}\right)$$

$$r_i = \frac{Re(Y'11)}{(Im(Y'11) - \omega Cgd)^2 + (Re(Y'11))^2}$$

$$\tau = \frac{1}{\omega} arc\sin\left(\frac{-\omega Cgd - Im(Y'21) - \omega Cgs r_i Re(Y'21)}{g_m}\right)$$

$$Cds = \frac{Im(Y'22) - \omega Cgd}{\omega}$$

$$rds = \frac{1}{Re(Y'22)}$$

$$g_m = \sqrt{((Re(Y'21))^2 + (Im(Y'21) + \omega Cgd)^2)(1 + \omega^2 Cgs^2 r_i^2)}$$

As shown in Fig. 13, extracted capacitances are constant valued throughout a broad range of frequency (1-10 GHz). Using the analytical approach, the S-parameter comparison between measurements and simulations are shown in Fig. 14. Good agreement with measurements throughout the whole operating range is achieved.

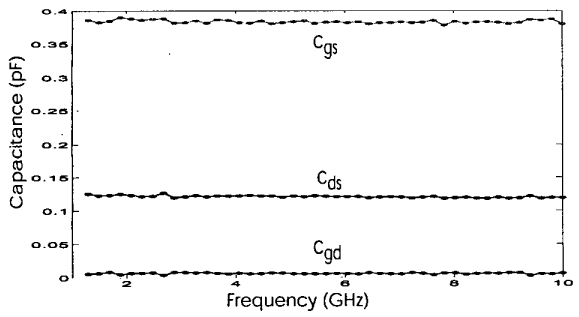

Fig. 13. Extracted c_{ds},c_{gs}, and c_{gd} at V_{DS}=20V and V_{GS}=9V.

VI. CONCLUSION

Extensive characterization work is done using device simulation to model LDMOS including quasi-saturation behavior. A method for obtaining a compact model for large-signal and the broad-band small-signal operation of LDMOS was presented and compared with measurements. This technique accurately extracts large and small signal parameters.

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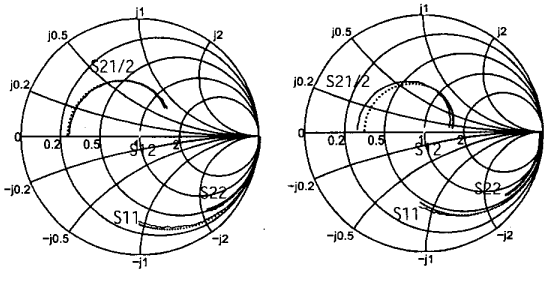

Fig. 14. (a) Measured and modeled S-parameters using extracted model parameters at V_{DS}=20 and V_{GS}=5, (b) at V_{DS}=30V and V_{GS}=9V (solid line:measured, dot:simulated).

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