Device Simulation for RF Applications

Robert W. Dutton, Boris Troyanovsky†, Zhiping Yu, Torkel Arnborg‡,
Francis Rotella, Gordon Ma*, and Junko Sato-Iwanaga§

Center for Integrated Systems, Stanford University, Stanford, CA 94305, USA
†HP EEsof Division, Hewlett-Packard Co., Santa Rosa, CA 95403, USA
‡Microelectronics Research Center, Ericsson Components AB, Kista, Sweden
*Networking & Computing Systems Group, Motorola, Tempe, AZ, USA
§Electronics Research Lab., Matsushita Electronics Corporation, Osaka, Japan

Introduction

The rapid growth of wireless systems at radio frequencies (RF) is driving the need for improved analog circuit and device analysis at gigaHertz frequencies. This includes: low noise front ends, linear amplifiers, mixers, and power amplifiers. Moreover, the parasitic effects of capacitance and inductance, both on- and off-chip, require careful extraction and characterization in support of predictive modeling. While time-domain techniques work well for digital systems, often the spectral and dynamic range requirements for communications systems necessitate accurate analysis of harmonic content with frequency differences of a thousandfold or more. This paper demonstrates the applicability and unique strengths of device-level harmonic balance (HB) in the simulation and physical modeling of RF circuits.

The HB method is briefly reviewed along with recent algorithmic innovations that improve both efficiency and range of applications -- for example, in support of high-Q circuit design. Next several applications of device-level HB will be used to illustrate how the technique supports RF design across a range of device technologies: bipolar, MOS, and compound materials (GaAs, etc). Included in this discussion are both the direct assessment of circuit level performance factors such as harmonic (HD) and intermodulation distortion (IM) as well as the underlying physical causes. Namely, the device level HB capabilities provide unique insight into the technology and device geometry factors that directly affect the performance. Finally, many of the calibration and parasitic extraction issues involved in RF modeling will be discussed. A novel parasitic extraction technique will be demonstrated that uses constructive solid geometry as a means to support package modeling.

Numerical Approach Using Harmonic Balance

Device-level harmonic balance (HB) extends the well-known circuit analysis technique to the nodal (i.e. grid) scale inside the device. The normal set of semiconductor variables (ψ, n and p) are expanded in a quasi-Fourier series at each node and iteratively solved for, along with the circuit boundary conditions, to obtain a steady state solution. Hence, the total number of unknowns is $N(2H+1)$, where N is the number of nodes multiplied by three (three variables per node) plus the number of device terminals and H is the number of harmonics not including the DC component. Those nodes (or grid) typically represent the device in 1D or 2D. When solved, the system of equations results in a Jacobian matrix of size $(2H+1)N \times (2H+1)N$ -- indeed a potentially huge numerical problem (typical N in 2D is more than 3000, and H can easily exceed 100). The efficient numerical solution of device-level HB equations has involved extensive research and prototyping over the past few years (1), (2), (3), (4). A few highlights of recent progress are now presented.

Given the frequencies of the (possibly multi-tone) input signal, the harmonics are chosen by a so-called diamond truncation scheme of order P. A system of $(2H+1)N$ nonlinear equations in as many unknowns is obtained by applying a finite difference scheme over the spatial dimensions, and by taking $2H+2$ samples along the time axis. The Newton-Raphson method is then used to solve the resulting system of nonlinear algebraic equations. At each iteration, because of the large size of the matrix, the linear system is solved iteratively using GMRES (Generalized Minimum RESidual), a method in the category of Krylov subspace solution techniques. There are two key steps in applying GMRES: computing matrix-vector products involving the HB Jacobian, and applying backsolves involving a preconditioning matrix. The matrix-vector products can be carried out efficiently using the FFT operator. A relatively efficient preconditioner can be constructed by noting that in the low-distortion regime, the HB Jacobian assumes the form of $H+1$ decoupled AC matrices. The large size of device simulation problems, however, precludes the storage of all these matrices in the multi-tone case. To save memory and computational effort, we observe that large portions of the harmonic balance Jacobian vary slowly with frequency, and only the portion of the matrix corresponding to external circuitry varies rapidly (e.g, the resonant filter of Figure 4). We further note that typical two-tone simulations result in

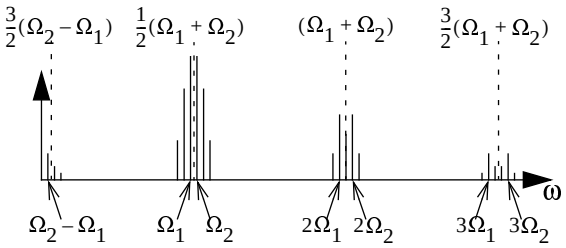
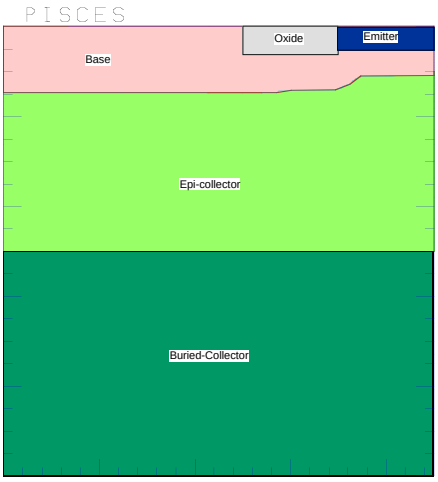


Figure 1. Tightly spaced frequency bands in a two-tone stimulus simulation.

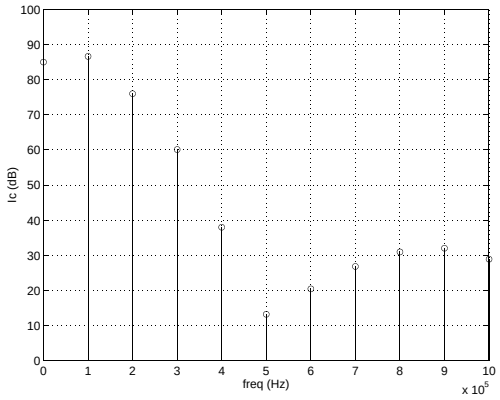
closely spaced "sections" (or bands) of frequencies (Figure 1). Large memory savings may be achieved by partitioning the preconditioning matrix into a large slowly-varying portion that is stored only at the band-center frequencies, and a small rapidly-varying portion that is stored at all H+1 HB frequencies. Block-LU algorithms are then applied to efficiently factor the resulting system. Details are given elsewhere, along with other algorithms used to more efficiently store the sampling data (6).

Applications of Device Level HB Analysis

The HB approach allows one to analyze the behavior of RF circuits based directly on the nonlinear device effects -- compact models are not used or required. Moreover, the major strength of the harmonic balance approach is its ability to resolve closely spaced harmonics, especially those resulting from IM distortion. Figure 2 shows the cross-section of a bipolar transistor and Figure 3 illustrates the output spectrum of collector current for the device, embedded in a high-Q tuning circuit shown in Figure 4. The exponential nonlinearity of the device, combined with the 50 mV input drive conditions, result in a rather severe broadening of the spectrum.



ıe cross-section of the BJT device used in high-Q circuit



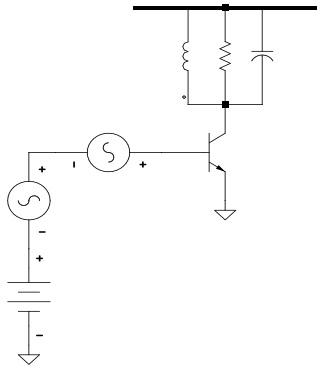


Figure 4. Circuit diagram of a single transistor mixer with high-Q output filter.

There are a number of alternative device and circuit architectures now being considered for RF power amplifiers that are targeted to overcoming the limitations indicated in the above example. The use of MOS devices and especially laterally-diffused (LDMOS) versions have become of growing interest due to their increasing frequency performance and the flexibility of digital/analog system integration that can be achieved using MOS technology (5).

Figure 5 shows the cross-section of such an LDMOS device along with typical parasitic components that surround it due to the packaging. There are four unique features associated with this structure to improve the RF and power performance of the device: (1) a laterally diffused, graded channel that enhances the RF performance (through a drift region) and prevents the punch-through, which in turn increases the device transconductance; (2) a p^+ sinker, not shown in the figure but represented by a side contact to the device in the simulation, that connects the source and substrate together to eliminate extra bonding wires; (3) the n-LDD region which decreases the electric field on the drain end of the channel and optimizes the output resistance and improves BV_{dss} and C_{dg}; (4) a metal gate field plate, represented by C_{gs}(I) in the figure, reduces the

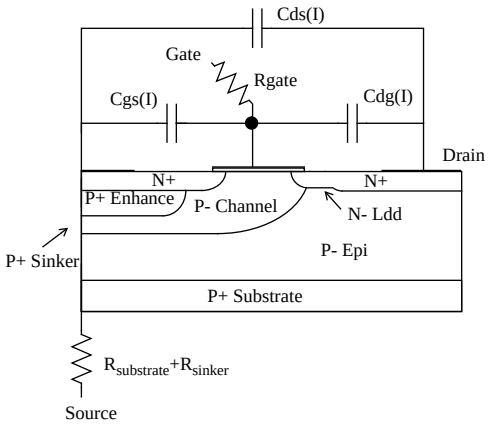


Figure 5. Cross-section of an LDMOS device surrounded by the equivalent circuit for parasitics.

electric fields at the edge of the g ate, thereby increasing the breakdown voltage and also reducing C_{dg}. In addition to the intrinsic structure of the device, the proper modeling and calibration of parasitics including g ate/source resistances and interconnect capacitance are critical to the simulation of RF performance.

Figure 6 shows the comparison between simulated and measured power gain and po wer added ef ficiency of the de vice. The agreement is quite reasonable, especially given the sensitivity of the results to the parasitic components in the model. Figure 7 sho ws detailed plots of ef ficiency v ersus output power for a set of statistical variations of key parameters. The strongest effect comes from the g ate resistance, which drives the efficiency inversely with increased values of R_g. C_{gs} has the ne xt strongest impact and L $_s$ has the smallest impact. These results provide the de vice and process engineers with necessary information for improving the overall device design by reducing the parasitics.

GaAs MESFET structures with recessed gate have a long and successful history as RF po wer devices. The combination of epitaxial doping and recess g ate structures have been highly optimized to give e xcellent power added ef ficiency, e ven at

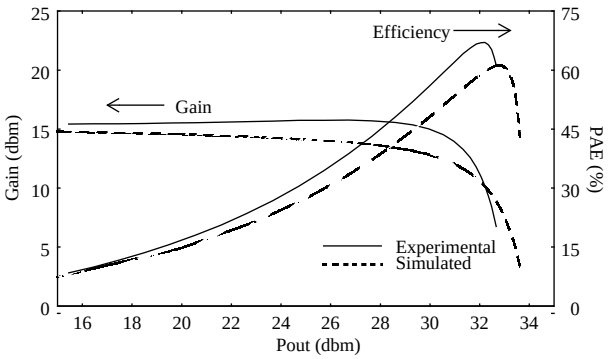
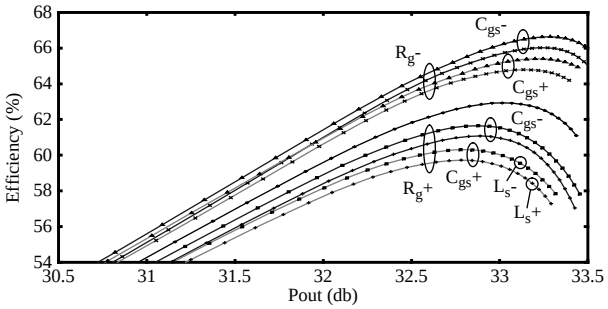
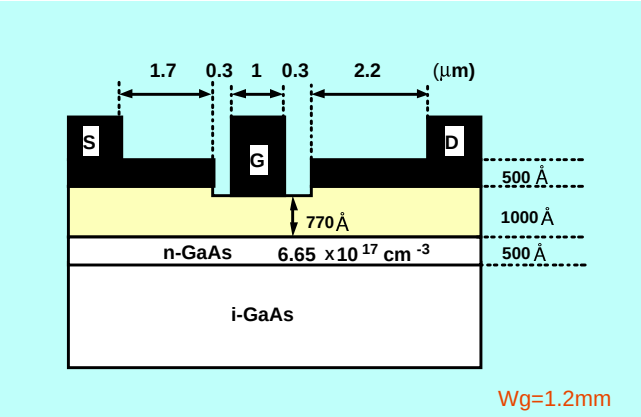


Figure 6. Comparison of simulated and measured power gain and added efficiency.





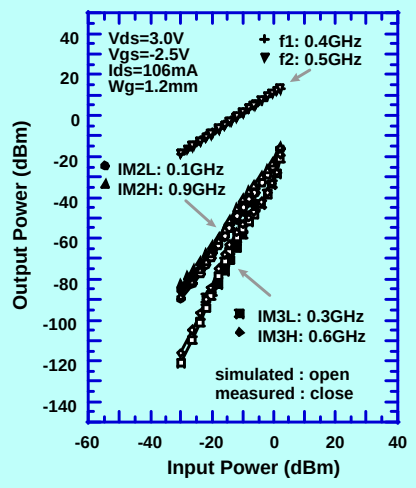


Figure 9. Comparison between simulated and measured intermodulation distortion level.

very high input signal/po wer le vels. One such structure is shown in Figure 8 where critical layer thicknesses and spacings are indicated. Figure 9 shows both simulated and experimental IM (InterModulation) distortion characteristics. The choice of frequencies reflects primarily limitations in the measurement equipment. The results sho w e xcellent agreement for second- and third-order distortion with dynamic range

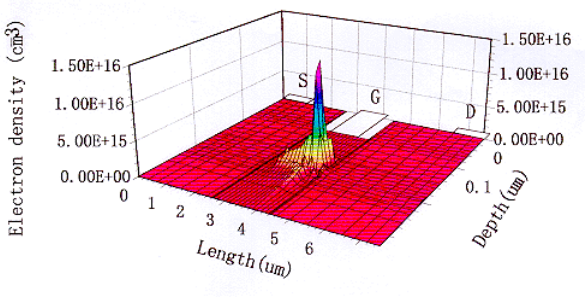


Figure 10. Bird's eye plot of distortion in electron concentrations.

greater than 65 dBm which is of critical importance for the particular cellular phone application. A unique strength of the HB approach is illustrated in Figure 10 which shows a bird's eye plot of where in the MESFET the total harmonic distortion occurs. A sharp spike in electron density occurs at the gate edge at a depth from the surface where the channel doping has been epitaxially deposited. Based on this detailed information, it is possible to consider local alteration of dopant distributions near this region to smooth out the nonlinearity and hence directly impact the distortion characteristics.

Parasitic and Packaging Effects on RF Behavior

Packaging issues are of major importance in achieving accurate RF models and parasitics (capacitance and inductance) critically affect the termination of circuits. Figure 11 and Figure 12 show both the overall complexity of the packaging for a 6W RF bipolar device package and a solid geometry representation that is being used in conjunction with FASTHENRY to extract parasitic inductance. In this way, geometry factors arising from the bonding and overall packaging processes can be included in the model rather than to simply use the empirical process of circuit de-embedding based on measurements

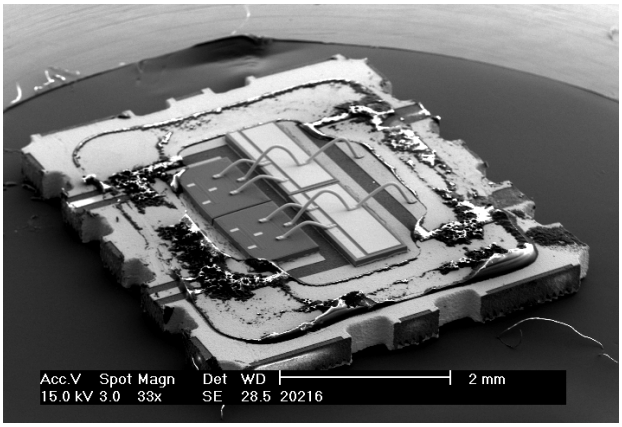


Figure 11. Photo micrograph for the RF package of a BJT power device from Ericsson.

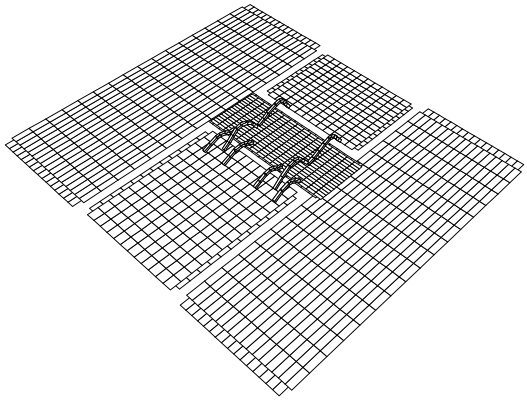


Figure 12. Solid geometry model for package shown in Figure 11 and used for parasitic inductance extraction.

Conclusions and Acknowledgment

This paper has highlighted recent contributions in the analysis of RF performance of several IC technologies based on device level harmonic balance (HB) analysis. The technique is shown to be powerful and new physical insight is possible based on the results.

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