Non-uniform Conduction Induced Reverse Channel Length Dependence of ESD Reliability for Silicided NMOS Transistors

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Abstract

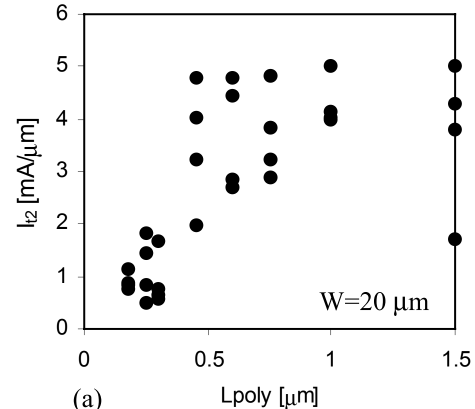
Contrary to general understanding, ESD performance of NMOS devices can degrade for shorter channel length transistors in advanced silicided CMOS technologies. In this work, using test structures in a 0.13 μm CMOS process, detailed characterization has been carried out for the first time to comprehend and model the physical mechanism causing this degradation. It is shown that the reverse channel length dependence of ESD performance is mainly due to severe non-uniformity in lateral bipolar conduction, which reduces the effective device width. Furthermore, it is demonstrated that substrate bias can be effective in alleviating this reverse channel length effect.

I. Introduction

In advanced CMOS technologies, the gate-grounded NMOS transistor is widely used as a protection device due to its effectiveness during ESD events. Based on the traditional parasitic lateral bipolar transistor triggering model under ESD conditions [1-2], it is generally believed that shorter channel length (L_{poly}) devices with higher current gain (β) will show better ESD performance since the power dissipation of such devices is smaller for a given ESD stress.

However, recent experimental observations indicate that it is not always the case; the dependence of ESD performance on the channel length can become reversed. In this regard, K. Bock et al. [3] qualitatively proposed that the trade-off between power dissipation and melt volume of the entire parasitic bipolar transistor determines the ESD performance, and not just the parasitic bipolar triggering model.

However, along with the reverse channel length dependence of ESD performance, new experimental results presented here also show a strong non-uniformity in the lateral n-p-n bipolar current conduction, which was not observed in the previous study [3]. This additional experimental observation has given new insight into phenomenon. Therefore, in order to gain a better understanding of the physical mechanism responsible for this unusual ESD behavior involved in the advanced silicided technologies, a detailed characterization study has been carried out using test structures implemented using a 0.13 μm CMOS process.



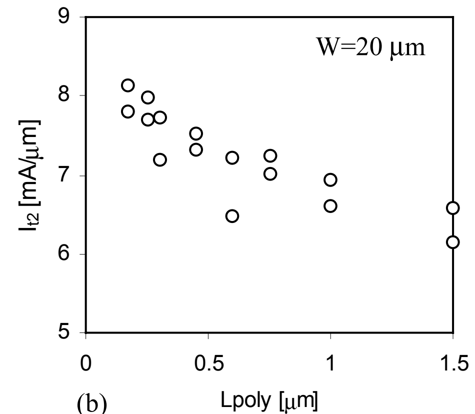


Figure 1: Dependence of the second breakdown triggering current (I_{t2}) on the channel length for (a) the silicided and (b) non-silicided 1.5V NMOS devices. The data show two different trends depending on silicided process.

II. ESD Performance

As a monitor of ESD hardness, transmission line pulsing (TLP) tests have been performed for various test structures with silcided ($CoSi_2$) and non-silicided diffusions. Fig. 1(a) shows the second breakdown triggering current (I_{t2}) with L_{poly} for the silicided devices; strong degradation of I_{t2} can be observed for L_{poly} < 1μm. This is contradictory to the expectation from the parasitic bipolar transistor triggering model [1-2]. However, as shown in Fig. 1(b), the same measurements for the non-silicided devices show that I_{t2} values indeed increase with decrease in L_{poly}. This implies

that the channel length dependence of I_{t2} is not always consistent for different technologies; moreover, the application of silicide diffusion strongly influences the ESD behavior of advanced NMOS transistors. The data in Fig. 1(b) also demonstrates that the model proposed in [3] to account for the short channel length effect is not appropriate.

The I_{t2} dependence on the effective channel length can also be observed through the data of I_{t2} versus drive current (I_{drive}) in Fig. 2, since the I_{drive} is inversely proportional to the effective channel length. In addition, as shown in Fig. 3, despite the decrease in I_{t2} with smaller L_{poly}, the bipolar current gain (β) of the silicided devices increases (in the same manner as non-silicided devices) with decrease in L_{poly} as expected, since the ratio of triggering voltage (V_{t1}) to holding voltage (V_h) (i.e. V_{t1}/V_h) is proportional to β through the relation given by

$$(1+\beta)^{\frac{1}{n}} = \frac{BV_{CBO}}{BV_{CEO}} \approx \frac{V_{t1}}{V_h} \qquad (1)$$

where n is a constant [4].

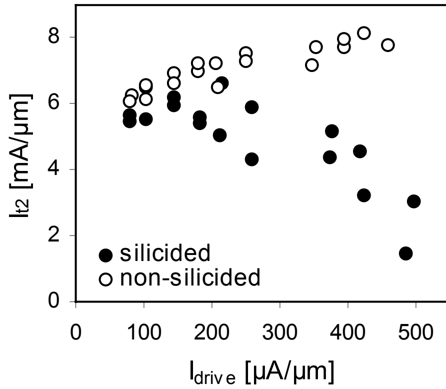


Figure 2: I_{t2} versus the drive current (I_{drive}) for the 1.5V NMOS transistors where W= 20 μm. The reverse channel length dependence of I_{t2} on the effective channel length for the silcided devices is clearly shown.

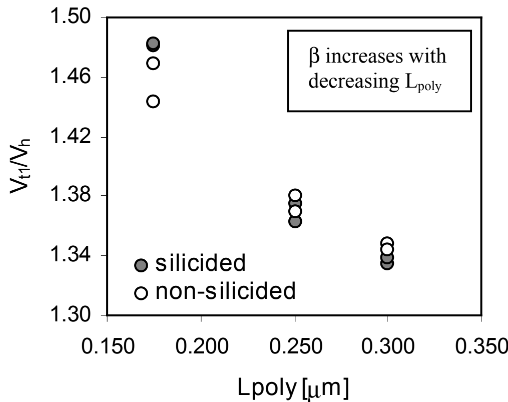


Figure 3: The V_{t1}/V_h with L_{poly} for the 1.5V NMOS devices. It shows that the bipolar current gain (β) of both silicided and non-silicided devices increases with decrease in L_{poly}.

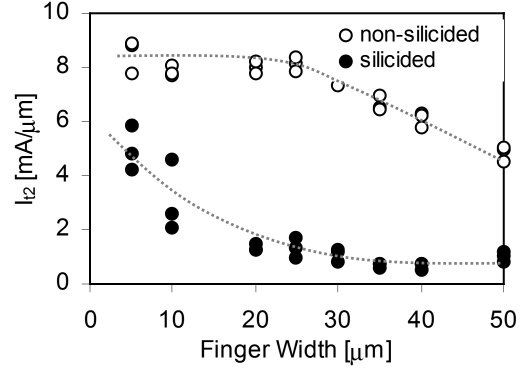


Figure 4: Finger width dependence of I_{t2} for the 1.5V silicided and non-silicided devices where L_{poly}=0.175 μm.

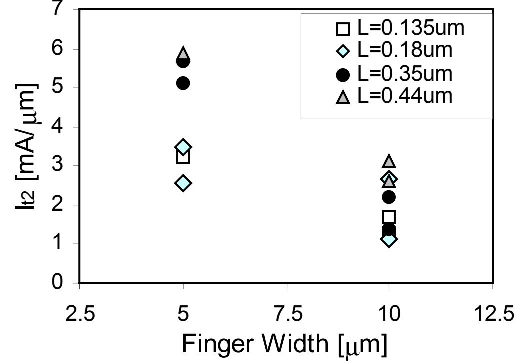


Figure 5: I_{t2} with finger width for the silicided 1.5V devices with different channel lengths. For the smaller channel length devices, uniform conduction is not reached even at W=5 μm.

III. Analysis and Discussion

In order to identify the root cause of the reverse channel length dependence, the I_{t2} has been characterized for devices with various finger widths (W) as shown in Fig. 4. Without silicided diffusions, the test devices show uniform ESD current distribution (constant I_{t2}) up to a finger width of about 25 μm. On the other hand, the silicided devices show a strong non-uniformity in the ESD current [5], which implies that the ESD behavior is strongly influenced by 3-D current conduction phenomenon. Although this behavior was not reported in earlier work [3], the non-uniform bipolar conduction effect has been predominantly observed for the advanced silicided devices studied here. Therefore, it is important to investigate whether this non-uniform current conduction has any possible impact on I_{t2} degradation with decreasing L_{poly}.

It can be observed from Figs. 1 and 4 that for the silicided devices, I_{t2} of the device with narrow fingers (W=5 μm and L_{poly}=0.175 μm) is nearly the same (~ 5 mA/μm) as that of the devices with wider fingers (W=20 μm) and L_{poly} > 1 μm. This also suggests that the I_{t2} degradation with L_{poly} can be shown to be different according to the reference finger width. However, it is not clear as to how the extent of the non-uniformity depends on the channel length L_{poly}.

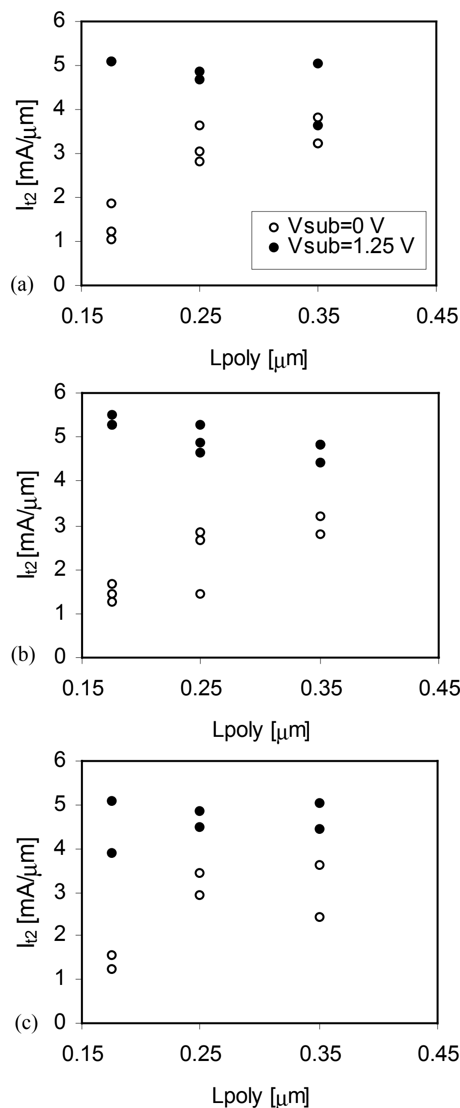


Figure 6: I_{t2} with L_{poly} for the silicided 1.2V devices (W=20 µm) with process splits. (a) baseline (b) *As* supplement S/D implant and (c) *P* supplement S/D implant.

In order to investigate the dependency of the strength of this non-uniform bipolar conduction effect on L_{poly}, I_{t2} was tested for devices with varying W and L_{poly}. As shown in Fig. 5, the non-uniform conduction seems to be stronger as L_{poly} shrinks since the shorter channel length devices show low I_{t2} (~ 3mA/µm), even at W=5 µm. Furthermore, it is known that the substrate bias improves I_{t2} by enlarging the turned-on finger width under ESD conditions [5]. The impact of substrate bias on the reverse channel length effect was also explored. Applying an external substrate bias, the I_{t2} dependence on L_{poly} for the 1.2V devices with various process splits is shown in Fig. 6. As can be seen, with substrate bias, the I_{t2} degradation with L_{poly} disappears independent of the process splits considered.

The above result also suggests that the dominant cause of the reverse channel length effect is non-uniformity in ESD current distribution, which is more prominent in the devices with silicided processes. In addition, we have also carried out a detailed investigation into thermal effects that might be involved in this reverse channel length phenomenon.

Electro-thermal transient simulations shown in Figs. 7 and 8 indicate that the temperature distribution at thermal failure changes significantly with L_{poly}. As the L_{poly} becomes short, the temperature distribution seems to be more localized, in consistence with [3]. Furthermore, for a given power dissipation, the maximum temperature increases with decreases in L_{poly} (see Fig. 9) since the power density in the shorter device becomes higher. However, as shown in Fig. 10 the measured failure power for the non-silicided devices still increases, despite the decrease in L_{poly} or the power dissipating volume, which is in contrast with observations from Figs. 8 and 9.

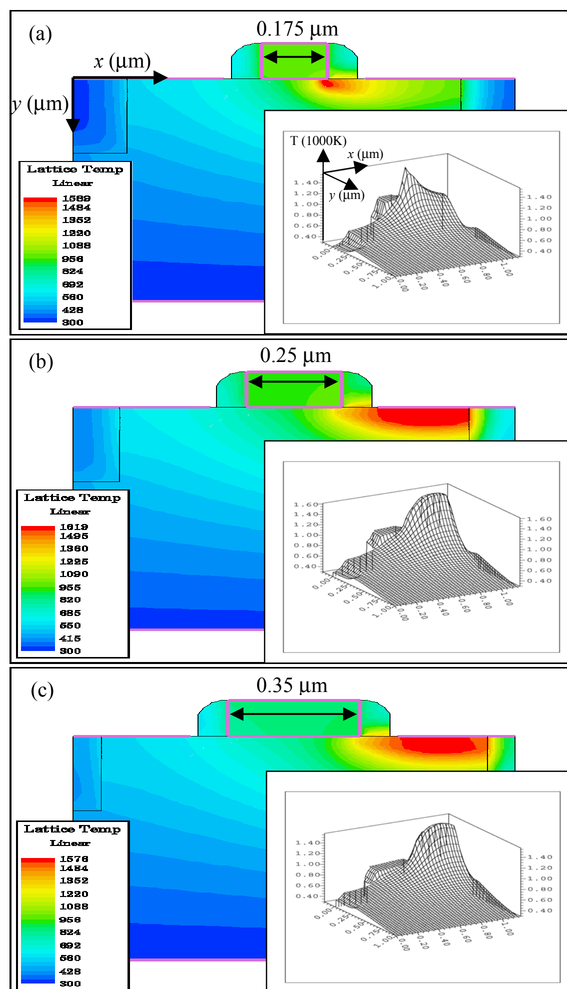


Figure 7: The temperature contours and 3-D distribution (insets) just before thermal failure for the devices with (a) L_{poly} = 0.175 µm, (b) L_{poly} = 0. 25 µm, and (c) L_{poly} =0.35 µm

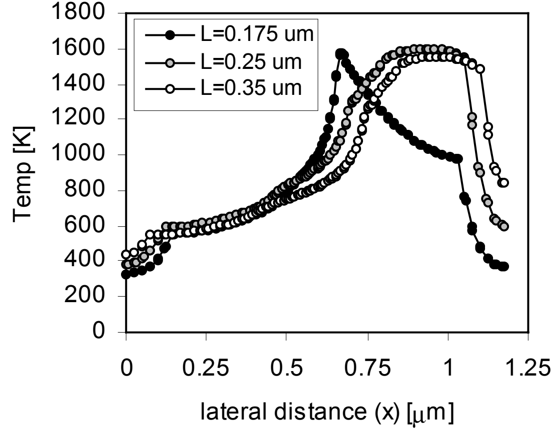


Figure 8: The temperature distribution along the channel (*x*-direction) for devices with different channel lengths just before thermal failure (at *y*=0.05 μm in Fig. 7).

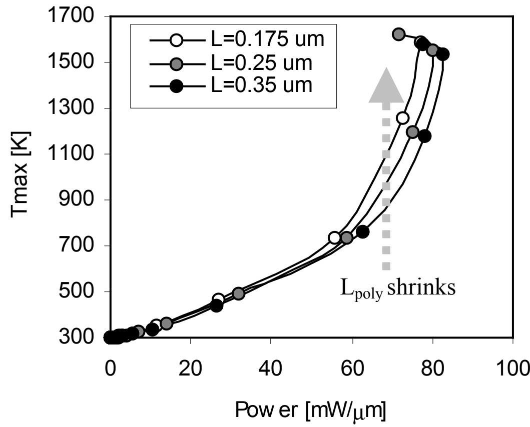


Figure 9: The maximum temperature (T_{max}) with the power dissipation for the devices with different gate lengths (L_{poly}).

In fact, Fig. 10 implies that the thermal effects resulting from the decreased L_{poly} are negligible for the non-silicided devices, in contrast to the silicided devices where the $CoSi_2$ layer is known to be more vulnerable to thermal damage under high current stress [6]. However, the trends in failure power shown for the two technologies in Fig. 10 cannot be explained at the same time if thermal effects with L_{poly} reduction is the main cause of the reverse channel length effect. To further justify the role of the non-uniformity mechanism in the reverse channel length effect, consider a first-order model of the rectangular box heat source with dimensions *a*, *b*, and *c* (*a*> *b*> *c*) at the second breakdown, the failure power (P_f), before the drain-substrate junction reaches thermal equilibrium, is given by [7]:

$$P_f = \frac{4\pi ka\,\Delta T}{\log(t/t_b) + 2 - c/b} \qquad (2)$$

where ΔT is the temperature rise above room temperature (300K), *k* is the thermal conductivity, and t_b is the thermal diffusion time. Using Eq.(2) and the measured P_f data for silicided devices, the W_{eff} (a in Eq. (2)) along with L_{poly} for various conditions were calculated as shown in Fig. 11. It can be observed that the effective finger width decreases with decreasing L_{poly}. These results confirm that the reduction in effective finger width is the primary cause of reverse channel length dependence of ESD performance in silicided devices.

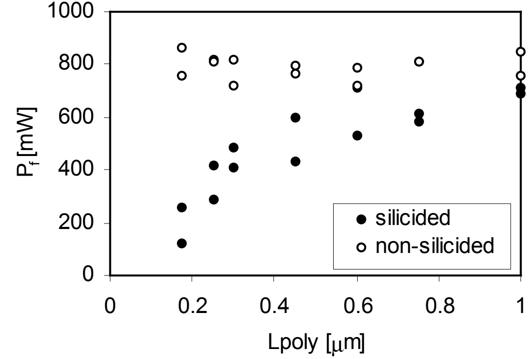


Figure10: The failure power with L_{poly} for 1.5V devices.

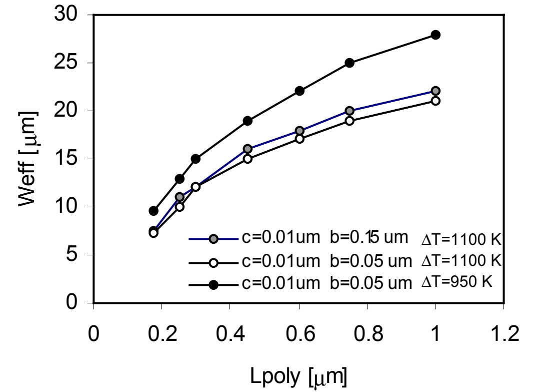


Figure 11: The predicted effective finger width (W_{eff}) with L_{poly} at second breakdown for the silicided 1.5V devices based on Eq.(2), depending on different conditions. The W_{eff} increases with decrease in ΔT for a given L_{poly}.

IV. Conclusions

Both device simulations and experimental data show that for deep submicron devices reverse channel length degradation of I_{t2} is due to a reduced effective device width due to non-uniform bipolar conduction during ESD. With substrate bias the reverse channel effect can be overcome, thus allowing the protection design with minimum L_{poly}, which is critical for input gate oxide and internal core circuit reliability.

Acknowledgements

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