A Bias Dependent Source/Drain Resistance Model in LDD MOSFET Devices for Distortion Analysis

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Abstract

In order to describe nonlinear distortion behavior precisely, an equivalent resistance model for n^- source/drain regions of LDD MOSFET featuring gate bias and drain bias dependence is implemented. Separating LDD device into an intrinsic MOSFET and two buried channel (BC) MOSFETs, a resistance model has been developed in a physically consistent manner. The proposed resistance model was confirmed using 2D device simulation results and its viability for distortion analysis has been investigated.

I. Introduction

Increasing demands on high linearity in MOS analog circuits have put an emphasis on the accurate physical behavior modeling in MOSFET devices. To achieve high linearity in MOS circuits, distortion behavior of MOSFETs has to be precisely described. As MOSFET devices have been scaled down, lightly doped drain (LDD) structures are commonly used to alleviate hot carrier effects by introducing n^- regions between the channel and the n^+ source/drain, which reduce maximum channel electric field and suppress the drain induced barrier lowering (DIBL) due to the voltage drop across LDD region. In LDD MOSFETs, the gate bias controls the surface carrier density in the n^- region under gate overlap, and in the rest of the n^-region through fringing fields. In addition, bulk carrier density is modulated by the depletion layer in the n^- region, which is determined by the n^- doping concentration and bias. Therefore the n^- source/drain resistances are nonlinearly dependent on the gate bias and the drain bias [1], [2], which lower the effective gate bias and drain bias as well. In general, these parasitic source/drain resistances are modeled as a gate bias dependent resistance, or described using a drain voltage reduction parameter in the saturation region [3]. However, this resistance is governed by gate bias and drain bias simultaneously, so the accurate characterization of its bias dependent behavior is required for predicting nonlinear behavior of MOSFET devices. Using an equivalent circuit analogy, a single LDD MOSFET device can be represented as a series combination of an enhancement mode MOSFET with no parasitic resistances and two equivalent BC MOSFETs as shown in Fig.1. In this paper, we include a fringing capacitance [4], and surface and bulk charge transport in BC MOSFET modeling [5]. Using the proposed physics-based equivalent source/drain resistance model, distortion behavior of sub-micron MOSFETs can be described more accurately.

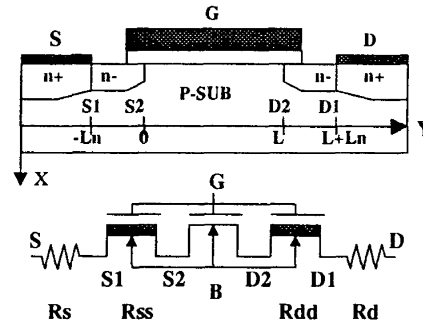

Fig.1. The cross section view of an LDD MOSFET and its equivalent circuit representation for a resistance modeling.

II. Approach

A. Equivalent Source/Drain Resistances

The structure of an LDD MOSFET and its equivalent circuits are shown in Fig.1, where R_s and R_d are the parasitic source/drain resistances including n^+ diffusion, contact, and wiring series resistances, which are considered to be constant. The equivalent resistances for n^- source/drain region, R_{ss}/R_{dd}, are derived as follows. Considering the drain n^- region as a buried channel MOSFET, and then its drain current can be written as

$$I_{ds} = W(\mu_{\text{eff}} Q_{sc}(y) + \mu_b Q_b(y)) \frac{d\Psi(y)}{dy} \tag{1}$$

where W is the electrical channel width, $\Psi(y)$ is the potential in the channel, μ_{eff} is the effective channel mobility, and μ_b is the doping dependent bulk mobility. The surface charge density Q_{sc} and the bulk charge density Q_b can be expressed as [6]

$$Q_{sc}(y) = \overline{C}(V_{gd2} - V_{FBn} - \alpha\Psi(y)) \tag{2}$$
$$Q_b(y) = qN_d(X_j - X_d(y)) \tag{3}$$

where N_d is average doping concentration in the n^- region and V_{FBn} is the flat band voltage of n^- region. X_j, $X_d(y)$ and V_{gd2} is the junction depth of the n^- region, the depletion layer width in the n^- region, and the effective gate bias between G and D_2, respectively. In the drain n^- region, surface can be accumulated or depleted depending on the polarity of $V_{gd2} - V_{FBn} - \Psi(y)$, and Eq.(2) holds approximately even in depletion condition [6]. But for better accuracy, an adjusting parameter α is introduced. $\overline{C}$ is the effective capacitance per unit area

including overlap capacitance and fringing capacitance in n^- structure and is given by [4]

$$\overline{C} \approx \frac{1}{L_n}[\frac{\epsilon_{ox}\epsilon_o l_{ov}}{t_{ox}} + \frac{2\epsilon_{ox}\epsilon_o}{\pi}\ln(1 + \frac{X_p}{t_{ox}})] \quad (4)$$

where l_{ov} is the gate overlap length, X_p is poly gate thickness, and L_n is the lateral length of the n^- region. Assuming X_d is position independent, integration of (1) across two ends of the n^- region yields the drain current as [5]

$$I_{ds} = \frac{W}{L_n}[qN_d\mu_b(X_j - X_d)V_{ID} + \mu_{\text{eff}}\overline{C}(V_{gd2} - V_{FBn} - \frac{1}{2}\alpha V_{ID})V_{ID}] \quad (5)$$

where V_{ID} denotes the voltage drop across the n^- drain region between D_1 and D_2. The depletion layer in n^- region expands with increasing V_{ds}, and this expansion rate is more enhanced for $V_{ds} > V_{dsat}$. Hence the bulk charge density reduces rapidly when V_{ds} exceeds V_{dsat}. Assuming the n^- region is fully depleted for $V_{ds} > V_{dsat}$ and the decrease in bulk charge density is negligible for $V_{ds} < V_{dsat}$, this kind of behavior can be modeled using a geometrical factor G_{eo} as

$$G_{eo} = \frac{G_o}{\exp(\delta(V_{ds} - V_{dsx})^{\beta})} \quad (6)$$

where δ and β are model fitting parameters to adjust the transition from $G_{eo} = G_o$ to $G_{eo} = 0$, G_o is a geometrical factor with no bias which is determined by n^- doping density and geometry. The characteristics of the geometrical factor (6) is shown in Fig.2. The V_{dsx} is the effective drain voltage given by [7]

$$V_{dsx} = \frac{V_{ds}}{[1 + (V_{ds}/V_{dsat})^{2m}]^{1/2m}} \quad (7)$$

where m is an empirical fitting parameter that can take integer values only, which controls the smoothness in the transition from linear region to saturation region, and V_{dsat} is the saturation voltage in the channel region which is derived by [8]. V_{dsx} becomes V_{ds} for $V_{ds} < V_{dsat}$, and V_{dsx} clamps V_{ds} to V_{dsat} for $V_{ds} \geq V_{dsat}$. Using (6), the bulk charge density term of (5) can be rewritten as $qN_dX_jG_{eo}$. From the equivalent circuits in Fig.1, $V_{gd2} = V_{gs} - V_{ds} + I_{ds}(R_{dd} + R_d)$ is obtained. Substituting this relation and $V_{ID} = I_{ds}R_{dd}$ into (5), we can have the quadratic equation for R_{dd} [5].

$$a_1 R_{dd}^2 + a_2 R_{dd} + a_3 = 0 \quad (8)$$

where

$$a_1 = (1 - \frac{1}{2}\alpha)W\mu_{\text{eff}}\overline{C}I_{ds} \quad (9)$$

$$a_2 = W[\mu_b qN_dX_jG_{eo} + \mu_{\text{eff}}\overline{C}\cdot(V_{gs} - V_{ds} - V_{FBn} + R_dI_{ds})] \quad (10)$$

$$a_3 = -L_n \quad (11)$$

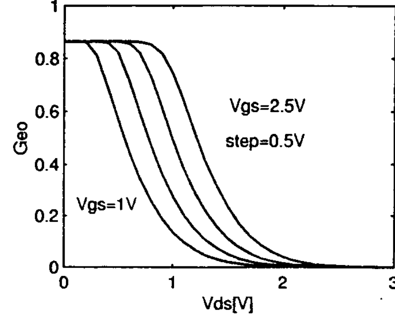

Fig.2. Characteristics of the geometrical factor (6) versus drain bias; $G_o = 0.864$, $\delta = 2.65$, and $\beta = 1.41$.

In (8), R_{dd} can be approximated as $-a_3/a_2$ if ${a_2}^2 \gg 4a_1a_2$ [2], [5]. However this approximation can be only valid for low V_{ds} region. So in order to get a continuous value of R_{dd} for all V_{ds}, Eq.(8) has to be solved. However, I_{ds} can not be determined without known R_{dd} so that the numerical iteration is required to get an accurate solution. To avoid time consuming iterations, I_{ds} can be approximated as the intrinsic drain current I_{dso}. This results in the overestimation in R_{dd} especially for high V_{ds}, but gives continuous R_{dd} values for all V_{ds}. The aspect of continuity is very important for distortion analysis, and the error in distortion analysis due to the approximated drain current will not be significant because of the fact that the extrinsic transconductance and output conductance depend weakly on R_{dd} for high V_{ds}. Using the same argument, R_{ss} can be computed. Since the geometrical factor for source n^- region can be considered to be independent of drain bias, it becomes a constant value G_o. For the source n^- region, ${a_{22}}^2 \gg 4a_1a_2$ holds for all regions of operating, and this results in $R_{ss} = -a_3/a_{22}$ where

$$a_{22} = W[\mu_b qN_dX_jG_o + \mu_{\text{eff}}\overline{C}\cdot(V_{gs} - V_{FBn} - R_sI_{ds})] \quad (12)$$

B. Intrinsic MOSFET Drain Current

Using bulk charge model, electron charge density of inversion layer can be written as

$$Q_n(y) = C_{ox}[V_{gs} - V_{th} - \Psi(y) - \gamma(\sqrt{\Psi(y) + 2\phi_F} - \sqrt{2\phi_F})] \quad (13)$$

where V_{th} is threshold voltage, $\gamma = (2\epsilon_{si}\epsilon_o N_{sub})^{1/2}/C_{ox}$, and $\phi_F = kT/q \cdot ln(N_{sub}/n_i)$. Drift velocity v_d in the inversion layer is given by

$$v_d(y) = \frac{\mu_{\text{eff}}E_y(y)}{1 + E_y(y)/E_{sat}} \quad (14)$$

where $E_y(y)$ is the longitudinal electric field, and E_{sat} is the critical electric field at which the carriers are velocity saturated. Using (13), (14) and $I_{dso} = WQ_n(y)v_d(y)$,

$E_y(y)$ can be written as

$$E_y(y) = \frac{I_{dso}}{W\mu_{\text{eff}}Q_n(y) - I_{dso}/E_{sat}} \quad (15)$$

By substituting $E_y(y)$ with $d\Psi(y)/dy$, and integrating (15) from $y = 0$ with $\Psi(y) = 0$ to $y = L$ with $\Psi(y) = V_{ds}$, intrinsic drain current is obtained as [9]

$$I_{dso} = \frac{1}{L + V_{ds}/E_{sat}} \cdot WC_{ox}\mu_{\text{eff}}F(V_{gs}, V_{ds}) \quad (16)$$

where

$$F(V_{gs}, V_{ds}) = (V_{gs} - V_{th} + \gamma\sqrt{2\phi_F})V_{ds} - \frac{1}{2}V_{ds}^2 - \frac{2}{3}\gamma[(V_{ds} + 2\phi_F)^{3/2} - (2\phi_F)^{3/2}] \quad (17)$$

In order to make a smooth transition for V_{ds} between linear region and saturation region, V_{ds} can be replaced with the effective drain voltage V_{dsx} (7), and this ensures the intrinsic drain current to be continuous for all regions of operation. Physical phenomenon such as DIBL, and channel length modulation in short channel devices can be included in the intrinsic drain current using conventional means in [10]. Substituting the intrinsic drain current (16) into (8), equivalent resistances, R_{dd} and R_{ss} can be obtained.

III. Results and Discussion

To verify the proposed equivalent resistance model, 2D device simulation was performed for a $0.5\mu m$ LDD MOSFET. The channel potential gradient $d\Psi(y)/dy$ is assumed the same as the quasi fermi potential gradient $d\phi_{\text{fm}}(y)/dy$, and R_{ss}/R_{dd} were extracted, dividing the quasi fermi potential difference across the n^- region $\Delta\phi_{\text{fm}}$ by the drain current I_{ds}. In addition, $\phi_{\text{fm}}(y)$ was read at Si/SiO_2 interface, and the potential variation along x direction was ignored. The modeled and simulated results are shown in Fig.3. For R_{dd}, modeled resistance shows better agreement with the simulation results as the gate voltage increases, but for low V_{gs} the modeled values show less accurate results. This discrepancy can be explained by the fact that the approximated surface charge model (2) was used for depletion condition. Under depletion conditions, the surface charge is proportional to the square-root of the channel potential, so that (2) is only available for weak depletion, even though the adjusting parameter α was used. On the other hand, irrespective of neglecting drain bias dependency of G_{eo}, R_{ss} model shows good agreement with the simulated results since the only accumulation layer can be formed in source n^- region. Including modeled R_{ss}/R_{dd}, the extrinsic transconductance can be approximated as

$$g_m \approx \frac{g_{mo}}{1 + g_{do}(R_{ST} + R_{DT}) + g_{mo}R_{ST}} \quad (18)$$

where $g_{mo} = dI_{dso}/dV_{gs}$, $g_{do} = dI_{dso}/dV_{ds}$, $R_{ST} = R_s + R_{ss}$, and $R_{DT} = R_d + R_{dd}$. In deriving g_m, we assumed that the variation of R_{ST} and R_{DT} are negligible in the very small change of bias. From (18), as long as $g_{mo} \gg g_{do}$, R_{DT} contribution becomes less significant. This condition holds for low V_{gs} and high V_{ds}, so that the proposed resistance model will not give a significant deviation in the extrinsic transconductance. The drain current can be reconstructed by summing the incremental current, up to the given bias.

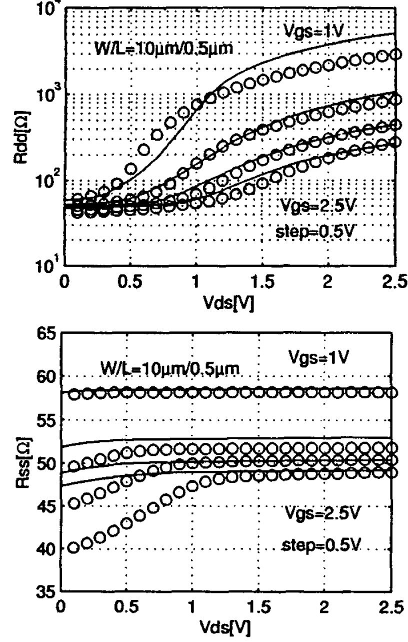

Fig.3. Modeled (line) and simulated (circle) R_{dd}/R_{ss}; $N_d = 1\times10^{18}cm^{-3}$, $X_j = 0.1\mu m$, $L_n = 0.125\mu m$, and $l_{ov} = 0.025\mu m$.

The modeled drain current and conductance results are compared with the measured data as shown in Fig.4, and the model reproduces very accurately the measured values. To confirm the model accuracy, harmonic distortion current amplitudes are also computed. This harmonic distortion behavior can be described by applying a sinusoidal signal to the gate terminal or the drain terminal, and then measuring the frequency spectrum of the drain current. Since the drain current depends nonlinearly on the gate bias and drain bias, the output drain current must have higher order harmonic components. For the frequency range where quasi static assumption holds, harmonic distortion components are mainly determined by the higher order derivatives of drain current with respect to the gate and drain bias. The gate induced harmonic distortion and drain induced harmonic distortion which are deduced from the proposed model are compared with the extracted values as shown in Fig.5. The proposed model shows good agreement with the extracted drain induced harmonic distortion and gate induced harmonic distortion as well.

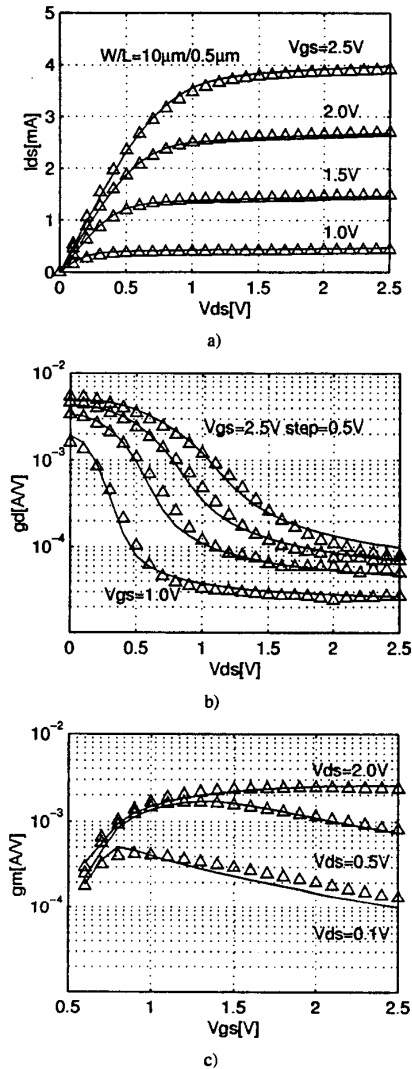

Fig.4. Calculated (line) and measured (triangle) current voltage characteristics for a $0.5\mu m$ LDD MOSFET; a) drain current, b) output conductance, c) transconductance

IV. Conclusion

A bias dependent source/drain equivalent resistance model for n^- region has been developed. Utilizing the charge transports in the n^- region and the intrinsic drain current, we expressed the source/drain resistance as a function of the gate and the drain voltage as well. Including the developed resistance model, I-V characteristics of LDD MOSFET device is well reproduced, and also the model can be applicable to the nonlinear distortion analysis.

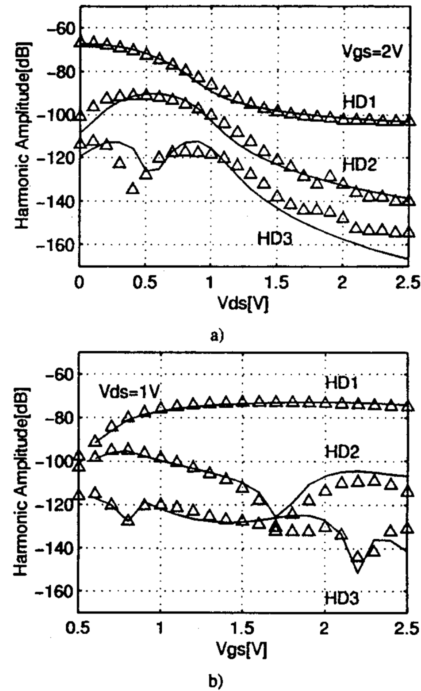

Fig.5. Calculated (line) and extracted (triangle) harmonic current amplitudes (the first order(HD1), the second order(HD2), and the third order(HD3)) for a $0.5\mu m$ LDD MOSFET;
a) drain induced harmonic distortion ($0.1\sin(2\pi ft)V$ applied),
b) gate induced harmonic distortion ($0.1\sin(2\pi ft)V$ applied)

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