Min/max On-Chip Inductance Models and Delay Metrics

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Abstract

This paper proposes an analytical inductance extraction model for characterizing min/max values of typical on-chip global interconnect structures, and a corresponding delay metric that can be used to provide RLC delay prediction from physical geometries. The model extraction and analysis is efficient enough to be used within optimization and physical design exploration loops. The analytical min/max inductance approximations also provide insight into the effects caused by inductances.

Keywords

Inductance, rlc tree, delay, on-chip interconnect modeling, physical design.

1. Introduction

As integrated circuit and system technologies continue to evolve, the delays associated with global interconnects have an increasingly dominant impact on the overall performance. With higher clocking frequencies and longer global interconnects to span the larger chip dimensions[1][4], interconnects are sometimes designed and optimized such that inductance effects become evident[2]. The inclusion of inductance in the timing analyses, however, can be a substantial problem for the overall design flows and methodologies. This difficulty is mainly because of the complexity associated with modeling inductance on an IC, which unlike capacitance that is solved via pattern matching, requires characterization via a field solver such as Fasthenry[3]. While significant progress has been made in speeding up field solvers such as Fasthenry, these solutions are impractical for use in an optimization loop or as part of a routing metric for early phase design planning. Since the global interconnects can have a dominant impact on the overall performance, it is imperative that metrics and models are available to assess the global RLC interconnect paths as early in the design flow as the architecture exploration process.

During the early phases of design, there is generally not even enough physical information to build a precise inductance model. Exact locations of the ground returns and densities and lengths of neighboring wires may not be available when assessment of the global interconnects is required. For this reason we would like to have a simple inductance extraction model, which when provided with the physical information that is available, could predict the minimum and maximum inductance that might result once the physical design is completed. Along with this min/max model we would like to have a delay metric that could be used to guide the optimization of the routing, insertion of repeaters, or changes in the overall floorplay.

In this paper, we propose an analytical inductance extraction model for characterizing min/max values of typical on-chip global interconnect structures. We further describe a delay metric that can be used in cooperation with these models to provide RLC delay prediction from physical geometries with efficiency that is sufficient for inclusion within optimization and physical design exploration loops.

†This work was performed when Yi-Chang Lu was at Monterey Design Systems

DAC 2001, June 18-22, 2001, Las Vegas, Nevada, USA.

2. Background and motivation

The most accurate way of analyzing inductive effects in complex structures is the *partial inductance* method[5]. To begin, the complex wiring structures are broken into simple segments. Since inductance is defined only for closed loops, partial inductances can be visualized as the inductance of a conductor segment as it forms a loop with infinity. That is, the return current path for the inductance is assumed to close at infinity, as shown in Fi g.1

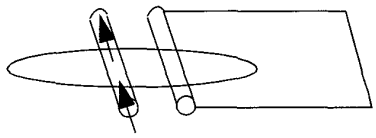

Fig. 1. Visualization of partial mutual inductance for two conductor segment. Both segment loops are assumed to close at infinity.

Partial inductances are best analyzed in terms of the normalized magnetic vector potential drop along a conductor segment due to current in that, or another segment. Consider two conductor segments, i and j, with a current I_j in segment j. The partial self inductance L_{jj} along the segment j is given by

$$L_{jj} = \frac{1}{I_j a_j}\left[\int_{a_j}\int_{l_j} A_{jj} \cdot dl_j da_j\right] \quad (1)$$

where A_{jj} is the magnetic vector potential along segment j due to the current I_j in segment j, which has a cross section a_j. The partial mutual inductance M_{ij}, which relates the induced voltage drop along segment i due to a change in the current along segment j, is given by a similar expression

$$M_{ij} = \frac{1}{I_j a_i}\left[\int_{a_i}\int_{l_i} A_{ij} \cdot dl_i da_i\right] \quad (2)$$

In (2), A_{ij} is the magnetic vector potential along segment i due to the current I_j in segment j and segment i has a cross section a_i. The magnetic vector potential A_{ij} is defined as

$$A_{ij} = \frac{\mu_0}{4\pi a_j}\left[\int_{a_j}\int_{l_j} \frac{I_j}{r_{ij}} dl_j da_j\right] \quad (3)$$

where r_{ij} is the geometric distance between two points in segment i and segment j.

Under some assumptions, such as uniform current distribution, there exist closed form expressions for partial self and mutual inductances for certain types of geometries[6]. For example, for a rectangular conductor, the partial self inductance is given by

$$L = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{w+t}\right) + \frac{1}{2} + \frac{0.2235(w+t)}{l}\right] \quad (4)$$

where w is the width, t is the thickness, and l is the length of the conductor. Similarly, the mutual inductance between two equal length parallel conductors is given by

$$M = \frac{\mu_0 l}{2\pi}\left[\ln\left(\frac{2l}{d}\right) - 1 + \frac{d}{l}\right] \quad (5)$$

where d is the distance between the conductors. By using these types of expressions and also considering the resistance and capacitance, an equivalent RLC circuit can be constructed which then can be analyzed using circuit simulation techniques.

Since the return current paths are not known *a priori*, in theory, the entire power distribution network has to be analyzed which requires solving and manipulating very large matrices. Simply discarding coupling terms to simplify the partial inductance matrix can violate conservation of flux, and lead to an unstable equivalent circuit model[14]. Although there have been recent proposals for sparsifying a partial inductance matrix in a stable manner[14][15][16][17][18], it remains impractical to use the large partial inductance matrices during the early phases of design exploration when the physical geometry information is only approximate.

An alternative for approximating the inductive effects is to use the *loop inductance* model. If the (dc) return path is known or can be estimated, then the entire loop can be modeled with a loop inductance. For example, consider the circuit shown in Fig. 2, which can be a part of a complex circuit. Let us assume that the structure shown in Fig. 2a has no dc connection to the surrounding portions of the circuit. The equivalent circuit obtained from the partial inductance approach is shown in Fig. 2b. Although this subcircuit is isolated at dc, there may be capacitive and inductive couplings to other elements. In the loop inductance model, these couplings are either neglected or their effects are approximately incorporated such that the equivalent circuit shown in Fig. 2c is obtained. The loop inductance is given by

$$L_{loop} = L_{s1} + L_{s2} - 2M \quad (6)$$

where L_{s1} and L_{s2} are the partial self inductances of the wires and M is the partial mutual inductance. The concept of using loop inductances greatly reduces the computational complexity in simulation time, when the number of wires in the system increases. Therefore, the only practical option for including the impact of inductance during design optimization is via a loop inductance approximation.

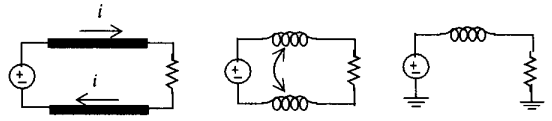

Fig. 2. (a) physical wires (b) wires under circuit models (c) loop inductance equivalent

In addition to its efficiency, the loop inductance model is especially suitable for well-designed IC structures[19][20]. For example, the clock nets may be shielded by routing power/ground wires next to them. Shielding is usually done for two reasons: to control the coupling capacitance to other nets, and to lower the inductance. For such a design the inductance can be modeled very easily using loop inductance since the shields provide the majority of the return path at the frequencies of interest. Even with shielding, however, it has to be noted the return path mechanism in on-chip nets is more complicated than that shown in Fig. 2. Because of the capacitive coupling between the wires, the current return happens everywhere along the wire. It is, however, obvious that this mechanism actually lowers the loop inductance and therefore our model given in Fig. 2 provides an upper bound for the loop inductance.

The loop inductance approach, as mentioned above, uses a series resistance-inductance combination to model the loop. Therefore, this model ignores the frequency-dependency of the resistance and inductance due to skin effect[21][22]. However, a very simple calculation reveals that the interconnections in today's chips, as well as those in the near future, will not have significant skin effect when the frequency is lower than several gigahertz, as shown in Table 1. Also note that as far as inductance is concerned, the dc solution bounds all frequencies. On the other hand, the effective resistance increases with the frequency. Hence the dc resistance may be inaccurate and a larger value can be used. Although there is not too much accuracy loss, there is a very big advantage for using frequency-independent resistance and inductance models. With simple resistance and inductance, the on-chip nets can be modeled as RLC trees. And as it will be explained later, the RLC trees can be analyzed very efficiently using simple moment based delay metrics.

Table 1: Copper skin depth @different frequency

Freq.	0.5 GHz	1.0 GHz	2.0 GHz	5.0 GHz
Skin depth	2.96 um	2.09 um	2.09 um	0.93 um

3. Objectives

In this work, we propose a methodology to estimate the minimum and maximum values for the loop inductance estimates without having to know the actual return paths. By doing this we consider the complete range of return path locations. The minimum and maximum values are actually bounds for on-chip structures with well-designed return paths. These inductance values can then be used in RLC tree modeling of on-chip nets for delay calculation. Later in this paper, we also propose an efficient testing method for the importance of inductance. In this section, we explain the RLC tree modeling of on-chip nets.

Consider the net topology shown in Fig. 3. which connects the pins A, B, and C. Each interconnect section is replaced with the required number of RLC pi models. For demonstration purposes, only one segment is used for each wire section in Fig. 3. The calculation of resistance values is straightforward. The capacitance values can be obtained either from an efficient capacitance extractor[8] or closed form expressions[7]. This paper concentrates on the calculation of inductance values. For other recent work on the on-chip inductance modeling and extraction, the readers are referred to [9][10][11][12][13]. In the next sections, we will present estimates for the minimum and maximum bounds for the inductance values.

4. Minimal Possible Inductance Value

It is well known that the loop inductance value is minimized when the return path is at the closest possible location. This is also obvious from (6): The minimum loop inductance occurs when the mutual inductance is maximum. There are, of course, limitations on the minimum value of the spacing because of the processing considerations. Considering these, it can be claimed that for the net given in Fig. 3, the minimum inductance is obtained if return paths are provided at the nearest possible location, as shown in Fig. 4. Even in this case some of the current may return from other parts of the power/ground network due to resistivity, especially at low frequencies. As the frequency increases, the current return is primarily located at the closest possible power/ground wire. There-

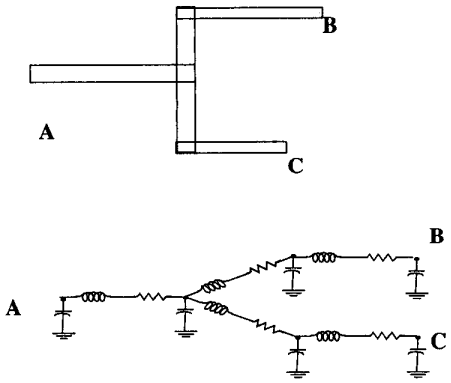

Fig. 3. A net and its RLC tree model.

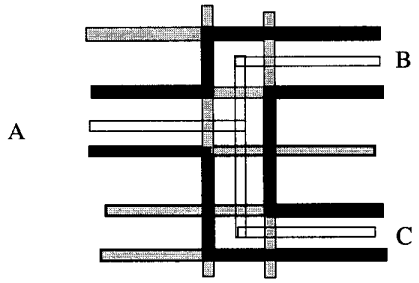

Fig. 4. Empty rectangles represent the net shown in Fig. 3. *Dotted rectangles represent the power/ground mesh network.* Black rectangles show the parts of the power/ground network where the return path are assumed to be.

fore, to find a lower bound of loop inductance we can safely use the model given in Fig. 4.

We also assume symmetrical shielding: same spacing on the both sides of the signal wire, and same width for both ground wires.

Under these assumptions we now consider a segment of the tree with its shielding wires, as shown in Fi g.5a. In the same figure the equivalent circuit to be used to find the loop inductance is also shown (Fig. 5c). It can be easily shown that the loop inductance in this case is given by

$$L_{loop} = L_s - 2M_{sg} + \frac{L_g}{2} + \frac{M_{gg}}{2} \tag{7}$$

where L_s is the partial self inductance of the wire, M_{sg} is the partial mutual inductance between the signal wire and the ground wires, L_g is the partial self inductance of the ground wires, and M_{gg} is the partial mutual inductance between the ground wires. Using (4), (5) and (7), the loop inductance can be expressed as a function of five parameters,

$$L_{loop}(w_s, w_g, s, l, t) \tag{8}$$

where w_s is the width of the signal wire, w_g is width of the ground wires, s is the spacing between the signal wire and either of the ground wires, l is the length of the three wire structure, and t is the thickness of the wires as shown in Fig.5(b).

By noting that thickness is a per layer constant parameter, and remembering that our goal is to find the loop inductance for a given signal wire width and length, we need the minimize the loop inductance with constraints on the spacing between wires and the width of the ground wires:

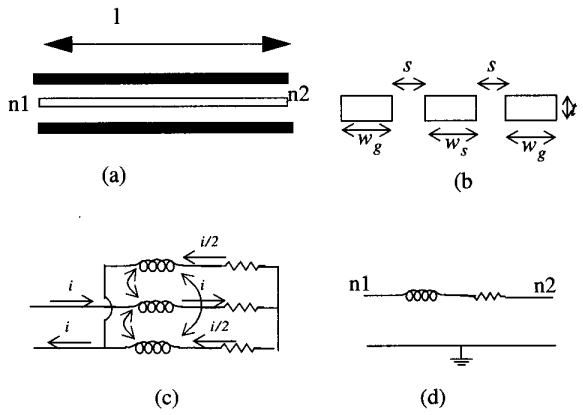

Fig. 5. (a) A segment of the net of Fig. 3 including nearby return paths; (b) The cross-section information; (c) The partial inductance model to find the loop inductance; (d) The electrical model of the segment of (a), excluding the capacitance.

$$\begin{aligned} &\text{minimize} && L_{loop} \\ &\text{subject to} && s \geq s_{min} \\ &\text{and} && w \geq w_{min} \end{aligned} \tag{9}$$

where s_{min} and w_{min} are the minimum spacing and width rules. Since we have a multivariable cost function, it can be solved using Lagrange multipliers:

$$\Lambda(s, w_g) = L_{loop} - \lambda_1(s - s_{min}) - \lambda_2(w_g - w_{min})$$

$$\nabla\Lambda(s, w_g) = \begin{bmatrix} \frac{\partial L_{loop}}{\partial s} - \lambda_1 \\ \frac{\partial L_{loop}}{\partial w_g} - \lambda_2 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{10}$$

where the derivatives can be obtained using (4), (5), and (7),

$$\begin{aligned} \frac{\partial L_{loop}}{\partial s} &= \frac{\mu_0}{2\pi}\left[-1 + \frac{3l}{w_g + w_s + 2s}\right] \\ \frac{\partial L_{loop}}{\partial w_g} &= \frac{\mu_0}{2\pi}\left[-\frac{l}{2(w_g + t)} + \frac{1.5l}{w_g + w_s + 2s} - 0.38825\right] \end{aligned} \tag{11}$$

Solving these equations, the optimal values for s and w_g for the minimum loop inductance are obtained as

$$\begin{aligned} s &= s_{min} \\ w_g &= \frac{-a1 - \sqrt{a1^2 - 4a2}}{2} \end{aligned} \tag{12}$$

where

$$\begin{aligned} a1 &= t + w_s + 2s_{min} - \frac{l}{0.38825} \\ a2 &= t(w_s + 2s_{min}) + \frac{l(w_s + 2s_{min} - 3t)}{0.7765} \end{aligned} \tag{13}$$

If this solution does not yield a valid w_g value, $w_g = w_{min}$ should be used.

As expected, the minimum loop inductance occurs when the spacing between the signal wire and ground wires is minimum. On the other hand, the optimal width of the ground wires is a function of all other parameters. To illustrate this, the dependency of the loop inductance on the ground wire width is plotted in Fig. 7 for different layers for a specific technology. By inserting the optimal values of s and w_g in (7) and by noting that t and s_{min} are constant per layer parameters, the minimum loop inductance can be characterized as a function of two parameters: w_s and l.

The exact expression of the loop inductance is a complex function and involves several logarithm and multiplication operations which can be costly inside the optimization loops. To simplify the number of floating point operations required to evaluate this expression, the minimum loop inductance can be pre-characterized as a function of width and length. This can be done either using look-up tables or simple polynomial approximations. Then, during the RLC construction the inductance value is obtained by simply evaluating these simple functions or looking at the tables by using only the width and the length of the wire that is being considered. Note that there is no search for the return paths, or closest stripe, or rail locations in the proposed approach.

5. Maximal Possible Inductance Value

An absolute upper bound for the loop inductance is obtained by assuming a return path at infinity with infinite width. In this case the loop inductance is equivalent to the partial self inductance of the wire,

$$L_{loop} = L_{self} \tag{14}$$

by letting the self inductance of the return path and the mutual inductance become zero in (6). Obviously this estimate is too pessimistic.

A more realistic scenario is to set the return paths to the power rails (or stripes). This is the case for designs in which no shielding is employed. At low frequencies, the current distribution is solely determined by the resistivity. However, at high frequencies, when the inductance actually matters, the current always takes the tightest return path. Therefore, to find the maximum loop inductance, we can use the three-wire system used in the previous section, but replace the nearby shields with the closest power rails or stripes. In this case the maximum loop inductance occurs when the signal wire is placed in the middle of two rails. If the distance between two rails (or stripes) is D, the spacing between the signal wire and ground wires becomes

$$s = \frac{D - w_g - w_s}{2} \tag{15}$$

For the width of the ground wires, the default rail (or stripe) width can be used. Then similar to the approach explained for the minimum inductance case, the maximum loop inductance can be characterized as a function of wire width and wire length.

6. Effect of inductance on delay

In the previous sections, we have constructed simple models for inductance. But these simple inductance estimates are useless without equally efficient and simple delay metrics. Several delay models have been proposed for RLC interconnect in the past few years[23][24][25]. We next explain a moment-based delay metric which, we believe, can be used together efficiently with the simple inductance models.

The Elmore delay is widely used for various applications that require a delay performance metric, but most notably as a step response delay metric for RC trees. More recently it was shown that the Elmore delay is an absolute upper bound on the ramp response delay of RC trees[28]. It is recognized, however, that the Elmore delay, the first moment of the impulse response, does not include the inductance for RLC trees. The second and all subsequent moments are functions of inductance. Therefore, higher order delay models, such as asymptotic waveform evaluation (AWE)[26], have to be used to observe the effect of inductance. Despite its efficiency, even using AWE can be too costly in terms of CPU time in the inner most loop of an optimizer. In this work, we propose to test the importance of the inductance by using central moments of the impulse response for an RLC tree. In the following we outline the methodology.

The moments of an impulse response, $h(t)$, is defined as

$$m_i = \frac{(-1)^i}{i!}\int_0^\infty t^i h(t)dt \tag{16}$$

The moments are related to the transfer function, $H(s)$, which is the Laplace transform of $h(t)$, as:

$$H(s) = m_0 + m_1 s + m_2 s^2 + m_3 s^3 + \ldots \tag{17}$$

In RLC trees, the moments can be calculated very efficiently using the path tracing algorithm. The first moment is the Elmore delay, and in RLC trees it is independent from the inductance values.

We next define the central moments. The central moments, like moments, are also borrowed from the probability theory to be used in delay characterization[27]. The second and central moments are expressed in terms of circuit moments as follows:

$$\begin{aligned} \mu_2 &= 2m_2 - m_1^2 \\ \mu_3 &= -6m_3 + 6m_1 m_2 - 2m_1^3 \end{aligned} \tag{18}$$

The central moments have geometrical interpretations. The second central moment, μ_2, is the variance of the impulse response function and it measures the spread of the curve from the center. The third central moment, μ_3, is the measure of the skewness of the function. For RC trees, μ_2 and μ_3 are always positive[28]. For RLC trees, they are measures of the type of the damping. Next we will explain the relations between μ_2 and μ_3, and inductance in a small RLC circuit. Note that we use this simple RLC model only to demonstrate the properties of the central moments.

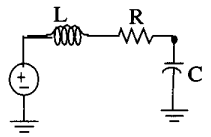

Fig. 6. A simple RLC circuit to be used to demonstrate how the central moments behave as a function of inductance.

Consider the simple RLC circuit shown in Fig. 6. The transfer function at the output node is given by

$$H(s) = \frac{1}{1 + sRC + s^2 LC} \tag{19}$$

The first few moments are calculated as

$$\begin{aligned} m_0 &= 1 \\ m_1 &= -RC \\ m_2 &= R^2C^2 - LC \\ m_3 &= -R^3C^3 + 2RLC^2 \end{aligned} \tag{20}$$

The second and third central moments are obtained as

$$\mu_2 = R^2C^2 - 2LC$$
$$\mu_3 = 2R^3C^3 - 6RLC^2 \quad (21)$$

As seen from (21), both μ_2 and μ_3 are positive and maximum when inductance is zero and they monotonically decrease as the inductance increases. They become zero at some close values($(R^2C)/2$ and $(R^2C)/3$ which is actually indication of underdamping of the step response. A detailed explanation of central moments and their relation with inductance can be found in[27].

Let us now consider two cases: An RLC tree and the same tree with zeroed inductance values. Also let us represent the corresponding circuit quantities with the superscripts RLC and RC. Comparing the second and third central moments provide a very strong indication about the effects of the inductance for the specific tree:

- $\mu_2^{RLC} \approx \mu_2^{RC}$ and $\mu_3^{RLC} \approx \mu_3^{RC}$ means inductance is not an issue for the tree which is being analyzed.
- $\mu_2^{RLC} \leq 0$ or $\mu_3^{RLC} \leq 0$ means the net has severe inductive effects such as overshooting.
- All other cases mean the step response is overdamped but the delay is affected by the inductance.

As a summary, by looking at the values of the second and third central moments we can decide on the importance of the inductance and use a suitable delay model. For instance, if inductance is an issue, a higher order delay model, such as AWE, should be used. Otherwise, Elmore delay or any other efficient delay models developed for RC type circuits can be used.

7. Results

We first compare the loop inductance values obtained analytically with the results obtained from Fasthenry. The circuit shown in Fig. 5 is used for this comparison. For analytical approximations, eqns. (4), (5), and (7) are used. The thickness and width numbers are taken from TSMC quarter micron technology[29]. As seen from Table 2, the results match very well.

Table 2: Results from analytical equations and FASTHENRY

	l=1mm t=0.6um ws=4um wg=1.5um s=0.4um	l=1mm t=0.6um ws=2um wg=1.6um s=0.4um	l=2mm t=0.6um ws=0.4um wg=1.6um s=0.4um	l=1mm t=0.92um ws=4.4um wg=2.2um s=4um
analytical	0.345nF	0.383nF	0.793nF	0.526nF
field solver	0.310nF	0.357nF	0.773nF	0.511nF

Importantly, our analytical model can be used to quickly estimate the loop inductance or changes in loop inductance as a function of wire sizes and spacings. As a demonstration, in Fig. 7, we show the loop inductance dependency on the width of the return wires for different layers of the TSMC 0.25um technology. The results in Fig. 7 correspond to the minimum loop inductance calculation described in Section 4. In Fig. 8, we display the loop inductance behavior as a function of the spacing between the signal and ground wires. Once again, these results are for the minimum loop inductance configuration described in Section4.

To demonstrate a complete analysis which includes extracting the parameters and estimating the delay via our proposed metric, we consider a 1 mm long interconnect which is divided into 10 RLC segments. The width and thickness of the wire are 0.5 and 0.58

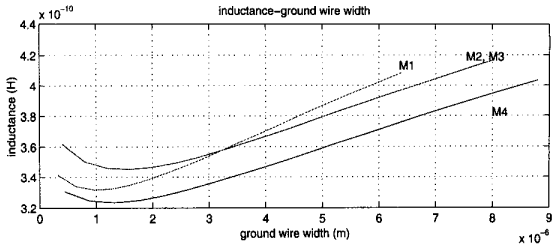

Fig. 7. Inductance values vs. Ground Wire Width @Signal Width=10x Minimum Width, Wire Length=1mm

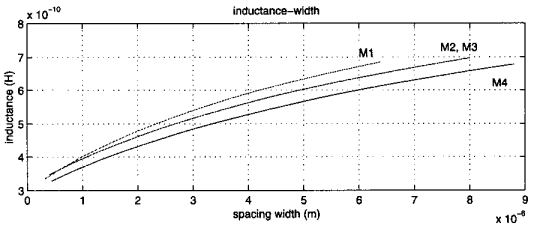

Fig. 8. Inductance value vs. Wire Spacing @Signal Wire Width=10x Minimum Width, Ground Wire Width=2um, Wire Length=1mm

microns, respectively. The resistance per square is 0.065 ohms and the capacitance per unit length is 0.00024 picofarads per microns. The line is excited with a step input voltage source with a 10 ohms source resistance and is terminated with a 25 femtofarad capacitive load. The minimum loop inductance model was calculated as 0.26 nanohenries for this 1 mm long wire. The maximum loop inductance estimate was 0.98 nanohenries assuming a 10 microns separation between the rails. The absolute maximum inductance value is the partial self inductance of the wire, which for this example had a value of 1.61nH. The second and third order central moments were calculated for this range of inductance values, and the results are summarized in Table 3. The step response delays for these cases were also analyzed with a second order AWE approximation, and are also included in the table. The Elmore delay value is 0.0215 nanoseconds, and since it is invariant to inductance it is the same for all the cases. The corresponding output waveforms are plotted in Fig. 9.

Table 3: The second and third central moments and step response delay of a 1mm long interconnect under different models of inductance.

Lloop (nH/mm)	0	0.26	0.6	0.98	1.61
μ_2	3.09e-4	2.34e-4	1.37e-4	2.84e-5	-1.49e-4
μ_3	1.06e-5	7.43e-6	3.24e-6	-1.43e-6	-9.06e-6
delay (ns)	0.0168	0.0171	0.0165	0.0195	0.0236

Comparing the central moments from the table with the waveforms in Fig. 9, it is apparent that the second and third central moments are very good indicators of the inductance. When the minimum

inductance model is used, the delay is changed very little compared to the RC case. The central moments accurately predict that the inductance effect is not significant in this case. Small changes in the central moments compared to RC case imply that the Elmore delay can still be used as the delay metric. As seen from the waveforms, the change in the slope is also small for the minimum inductance case.

In contrast, when only the partial self inductance value (last column) is used, both the second and third central moments become negative. Although the delay in this case is closer to the Elmore delay, use of the Elmore delay metric is no longer reliable since the waveshape is non-monotonic, and the slope is not easily measured. The negative values for the second and third central moments clearly indicate the underdamped response shown in Fig. 9.

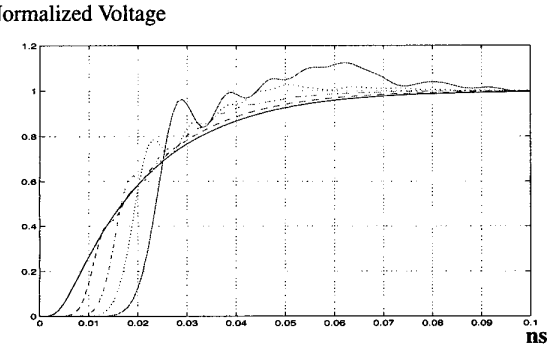

Fig. 9. The output waveform of a 1mm long interconnect for different values of inductance with a step input excitation. The solid line is for zero inductance. The dashed line is 0.26 nH/mm. The dotted-dashed line is for 0.6 nH/mm. The dotted line is for 0.98nH/mm. The other solid line which represents a strong overshoot is for 1.61 nH/mm.

8. Conclusions

We have shown new analytical models for estimating the minimum and maximum loop inductance for on-chip RLC interconnect signal paths. By avoiding the need for a field solver, and providing an equally efficient delay measure in terms of central moments of the RLC model, this work can be used for performance estimation and design optimization during the early phases of design.

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