TCAD Tool Development at Stanford University

Zhiping Yu

Center for Integrated Systems

Stanford University, Stanford, CA 94305

Also with Tsinghua University, Beijing, China
(yu@ee.stanford.edu)

Topics

- General Introduction -- Where We Are Up To?
- Device Simulation for RF, Large Signal Analysis
- QM/TED Model Development for MOS Scaling
- 3D Solid Modeling Targeted for Analyzing Interconnect/Parasitics
- Proposed Projects with Motorola

Current TCAD Activities at Stanford

- Process simulation -- TED model
- Device simulation
  - -- Harmonic balance for RF, large signal anal.
  - -- Interconnect/parasitics analysis
  - -- ESD, multi-finger structure
  - -- inverse profiling
  - -- QM model for MOSFET and scaling issue
  - -- Atomic scale investigation
- Linear mode device/circuit simulation

Quantum Mechanical Effects in MOS

- **Manifestation:**
  - -- threshold voltage (larger)
  - -- gate capacitance (smaller)
- **Physical insight:**
  - -- Boundary condition required by QM (peak of carrier profile is away from the interface)
  - -- Energy level quantization in the surface potential well

MOS Scaling Towards Sub-tenth Micron

- The evolution at a faster pace
  - -- L_{gate}/L_{eff}(μm): 0.35/0.27, 0.25/0.18, 0.18/0.13, 0.13/0.1, 0.1/0.07, 0.07/0.05
  - -- oxide thickness (Å): 75, 45, 30, 20, 15(?)
  - -- V_{DD} (V): 3.3, 2.5/1.8, 1.3, 1, ...
- The driving force -- speed

$$t_d = \frac{CV_{DD}}{I_{Dsat}} = \frac{L}{\kappa v_{sat}(1 - V_{th}/V_{DD})}$$

- The magic number $V_{th}/V_{DD} = 0.2$,and the role of κ

- **Where does t_{ox} play role: $\kappa(t_{ox})$, $V_{th}(t_{ox})$**
- **The limitations:**
  - **-- sub-threshold voltage slope of $\ln I_{DS}/V_{GS}$**
  - **-- breakdown electric field of oxide**
  - **-- tunneling current**
- **The key modeling issues:**
  - **-- effective oxide thickness (QM effects)**
  - **-- channel doping profile (TED)**

3D Solid Modeling and Interconnect/Parasitics Analysis

- **What 3D solid modeling is:**
  - -- **3D objects of wires, layers, cells, circuits**
  - -- **Layout based**
  - -- **Technology file (processing info)**
- **Configuration of software system: ACIS, AVS, custom programs**
- **Meshing and device/interconnect analysis**

Proposed Projects with Motorola

- Silicon CMOS technology
  - -- Scaling
  - -- Process/device simulation (ESD, etc.)
  - -- Device characterization
- RF power devices (Si DMOS, GaAs MESFET)
- Interconnect and parasitics
- A BIG picture: development of Java-based OO circuit/device/process simulator