Modeling, Analysis, and Design of RF LDMOS Devices Using Harmonic Balance Device Simulation

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Abstract

This paper describes how device simulation may be used for the modeling, analysis, and design of RF LDMOS devices. Improvements to device analysis needed to meet the requirements of RF devices are discussed. Key modeling regions of the LDMOS device are explored and important physical effects are characterized. The LDMOS model is compared to DC and small signal AC measurements for calibration purposes. Using the calibrated model, large signal accuracy is verified using harmonic distortion simulation and inter-modulation analysis. Predictive analysis and a study of the structure's parasitic components are also presented. Load-pull simulation is used to analyze matching network effects to determine the best choices for device impedance matching.

I. Introduction

Over the past two decades device simulators such as PISCES (aka Medici, Atlas, etc.) have played an important role in understanding device design, physics, and performance [1][2][3]. The evolution of PISCES specifically has resulted in new models for physics in order to accurately model the intrinsic device (e.g.: [4]); more advance boundary conditions to represent the matching networks around the device (e.g.: [5]); and improved numerics to achieve faster simulations with more complex structures (e.g.: [6]).

Recent changes to PISCES include additions to allow for the simulation of RF devices. An harmonic balance (HB) solver was developed to solve for the large signal steady-state performance of a semiconductor device rather than using computationally more expensive transient analysis[7][8][9]. Instead of solving for the time samples of each variable, the HB approach expands each device variable (i.e. Ψ, n, and p) as a Fourier series and solves for the coefficients X_{n0}, X_{nh}^{R}, and X_{nh}^{I} given by:

$$x_n(t) = X_{n0} + \sum_{h=1}^{H} \left(X_{nh}^{R}\cos(\omega_h t) - X_{nh}^{I}\sin(\omega_h t)\right) \tag{1}$$

The number of harmonics is limited to H where higher order frequency components are assumed to be insignificant. Upon computing the value for the Fourier coefficients, the time domain signal can be assembled from the Fourier expansion.

Harmonic balance analysis offers computational benefits over transient analysis in certain circumstances. It captures the steady state performance of a device in the presence of potentially longer time constant phenomena and avoids an excessive number of time steps in multitone analysis. Conversely, the disadvantage of HB analysis is that the matrix of equations increases proportionally to 2H+1. Given that the device simulation itself requires the solution of large matrices, special algorithms and numerics have been optimized for solving the semiconductor equations using harmonic balance techniques[9]. As a result, the user must then make trade-offs in the modeling of the device in order to minimize the size of these matrices and in turn reduce the simulation time.

Another recent improvement to PISCES involves the addition of circuit boundary conditions. Currently, tools exist for the simultaneous simulation of circuits and devices[5][10]. However, these tools are targeted for unit cell development rather than discrete component analysis. Therefore the improved boundary conditions target the simulation of a discrete device where parasitics are important for performance evaluation. Coupling the boundary conditions with HB simulation leads to a powerful tool for RF device simulation including parasitics [11][12].

Generalized linear circuits are reduced to a set of boundary conditions for the device simulator:

$$\begin{aligned} \text{DC:} \quad & G_{d0}(E_{d0} - V_{d0}) - I_{d0}(\Psi_0, n_0, p_0) = 0 \\ \text{Fundamental:} \quad & G_{d1}(E_{d1} - V_{d1}) - I_{d1}(\Psi_1, n_1, p_1) = 0 \\ \text{Overtones:} \quad & -G_{dh}V_{dh} - I_{dh}(\Psi_h, n_h, p_h) = 0 \end{aligned} \tag{2}$$

These equations relate the unknown voltage at each electrode (V_{di}) to the unknown current flowing into the electrode (I_{di}). Only one equation is added per electrode to the device matrix which has little impact on the solution time. Iterations are performed over the entire set of device equations until a self-consistent solution is attained.

Separate equations are included for the DC bias, fundamentals, and overtones. The DC and fundamental components have source terms in the external circuitry given by the (E_{di}) terms. The overtones, on the other hand, have no independent sources because the surrounding circuitry

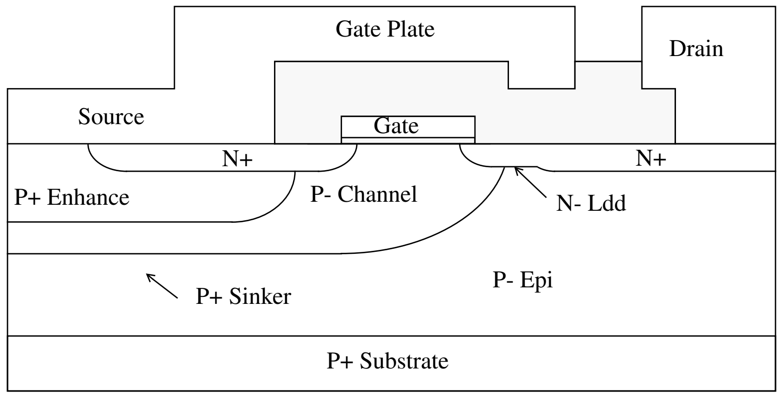


Figure 1: Cross-section of LDMOS device.

is linear, even though the system is globally non-linear because of the discrete transistor. Hence, the lack of a generating term does not imply that there are no overtones in the external circuitry.

Harmonic balance analysis and circuit boundary conditions provide PISCES with capabilities for RF device analysis. Harmonic balance allows for the simulation of the large signal steady state performance of a given device structure. External circuit boundary conditions include: the parasitic components, matching networks, and biasing networks that are important to accurately characterize and understand RF behavior. Previous work has used device simulation to characterize the DC and small signal analysis and required a circuit model to do large signal analysis[13]. This paper presents an example of modeling, analysis, and design of an RF LDMOSFET by utilizing an integrated device simulation that supports large signal steady state analysis as well as DC and AC effects in a single simulation environment.

II. LDMOS Device Physics and Modeling

In order to accurately simulate and model the LDMOS device, it is important to understand its operating principles. A cross section of the basic structure is given in Figure 1. This device was first characterized for RF applications in 1972 by Sigg.[14] The double-diffused design at that time offered advantages because it allowed for channel lengths of 1µm while the dominant technology at that time was at 5µm. With many design advances since 1972, this device offers significant improvements over an equivalent uniform channel MOSFET. For demonstration purposes a Motorola device built with 0.8 technology is studied[15][16]. The techniques presented have been applied to next generation technology development and optimization.

The laterally diffused graded channel enhances RF performance, prevents punch-through, and increases the device transconductance. These improvements are a result of increasing the electric

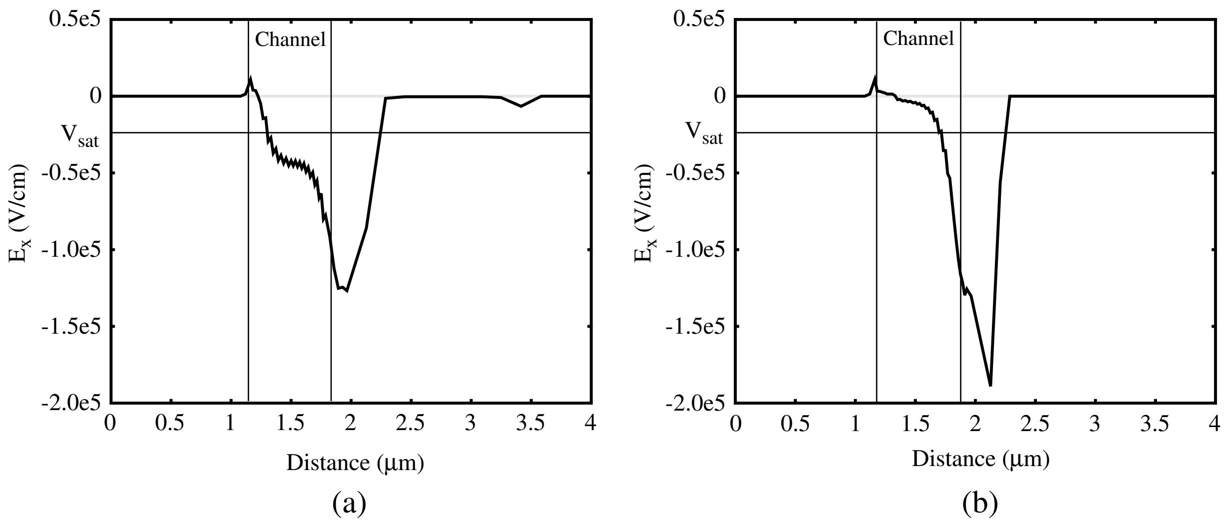


Figure 2: Comparison of the longitudal electric field in channel of an LDMOS device (a) versus a standard MOS device (b). The vertical lines indicate the edges of the channel region and the horizontal line is the approximate electric field (2×10^4 V/cm) when electrons reach velocity saturation.

field in the channel region such that the electrons reach velocity saturation. Figure 2 shows a PISCES plot of the longitudal electric field in the channel of a LDMOS device and a standard MOSFET. The device structures are the same except in the channel region where device (a) has a graded channel and device (b) has uniform doping. The integrals of the net doping profiles along the interfaces are approximately equal. The devices are biased in inversion just above threshold with 6V on the drain. The vertical lines indicate the edge of the channel and the minimum electric field to obtain velocity saturation. Electrons reach velocity saturation though the channel region for the graded channel device, but not in the uniformly doped channel.

Improvements to the device include a P+ sinker to connect the source and substrate together also eliminating extra surface bond wires. Thus only the gate and drain have surface bond wires. The elimination of bond wires on the source leads to improved RF performance in a power amplifier configuration because of the reduced source inductance.

A metal field plate (i.e. Faraday shield) reduces the electric fields at the edge of the gate, thereby increasing the breakdown voltage, reducing hot carrier generation, and reducing C_{dg}; however, C_{gs} increases. In a power amplifier application (common source), the input matching network can compensate for the additional C_{gs} while RF performance is improved by reducing the Miller capacitance (C_{dg}) between the input (gate) and the output (drain). The reduction in the cut-off

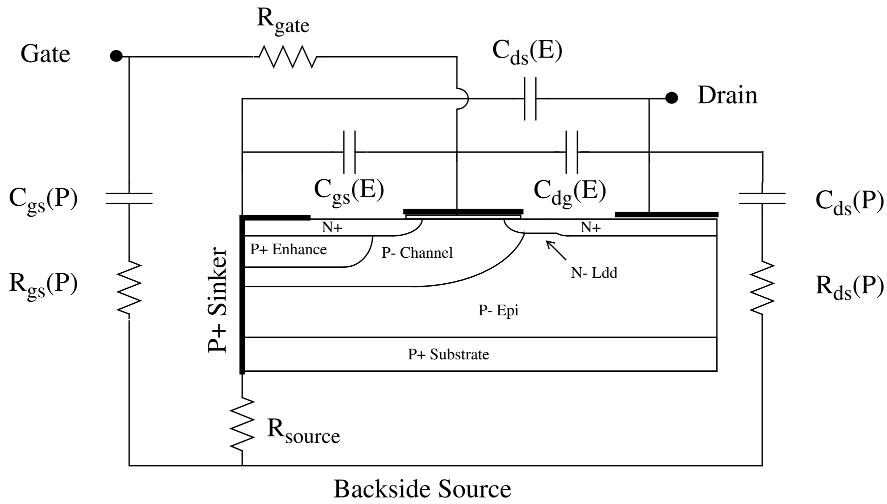


Figure 3: Model for an LDMOS device used with harmonic balance device simulation.

frequency due to the increased input capacitance is not as critical as long as it is 5 to 10 times above the operating frequency of the power amplifier.

Other important characteristics include an extended N- LDD to decrease the electric field at the drain end of the channel and to optimize R_{ds}(on), BV_{dss}, and C_{dg}. As a result, the device is capable of handling the high voltages needed in RF power applications (45V for the analyzed device).

To use RF device simulation requires modeling and calibration of the intrinsic device and parasitic components. The calibration has three goals: (1) develop a model for the device that minimizes computational time while maintaining accuracy; (2) gain understanding of the device physics affecting the performance; (3) obtain better knowledge of the parasitic components and their effect on performance. Figure 3 shows the model used to represent the LDMOS device and meets these modeling objectives.

Portions of the device have been eliminated from the physical device structure and replaced with lumped circuit components in simulation. As a result, the simulation time decreases because the number of mesh nodes is reduced, resulting in a smaller system of equations.

The criterion for replacing a section of the device is based upon the impact of physics surrounding that region. The major regions suitable for replacement in the LDMOS device are the P+ sinker/ backside contact and the surface contact structure. The P+ sinker is replaced by an electrode along the source edge of the device to act as a low resistance path connecting the source and substrate.

Rather than simulating the full substrate to the backside contact (~230 µm), a resistance is placed on this contact to represent the current path to the back-side.

In addition to the backside contacts, the surface contacts are replaced with circuit components. Figure 3 shows two contributions, one from the actual device electrode vias (E) and the other from the surface pads (P). The electrode structure contributes capacitances while the pad structure contains a capacitor and resistor in series. The resistance under the pad adds to the impedance of the circuit branch and becomes important at higher frequencies.

III. Analysis of LDMOS Structure

In this section, the model for the LDMOS structure is characterized and the results are compared to measured data. The key modeling regions addressed in this paper are the source resistance, intrinsic device regions (i.e. channel), and surrounding parasitic components. In addition, self heating effects are characterized in relation to I-V characteristics and the graded channel effects on the C-V characteristics are discussed.

In order to reduce the source inductance the device structure is designed for a backside contact which adds to the source resistance. The impact and magnitude of this resistance depends upon the pitch spacing of the fingers in the device layout. The current flows from the drain, through the channel, into the metal contacting the source (and Faraday Shield) and the sinker contact, through the sinker, and spreads into the substrate making its way to the back-side contact.

The source resistance has components from the distributed contact resistance, sinker resistance, and substrate resistance. The contact resistance is insignificant compared to the other components for this device structure and thus will not be considered. In other structures this resistance could potentially play an important role and therefore, it would need to be characterized. A PISCES simulation of the sinker structure leads to the current flow lines shown in Figure 4. The figure contains a cross section of two adjacent devices due to the fingered of the layout structure. The devices themselves are not included in the simulation since they do not directly affect the results. Instead, the source doping is extended all the way across both devices. The spreading of the current is limited and thus there is a significant effect on the actual resistance.

Figure 5 shows the resistance of one entire sinker as a function of the width of the device. The points represent simulation data and the line is a plot of

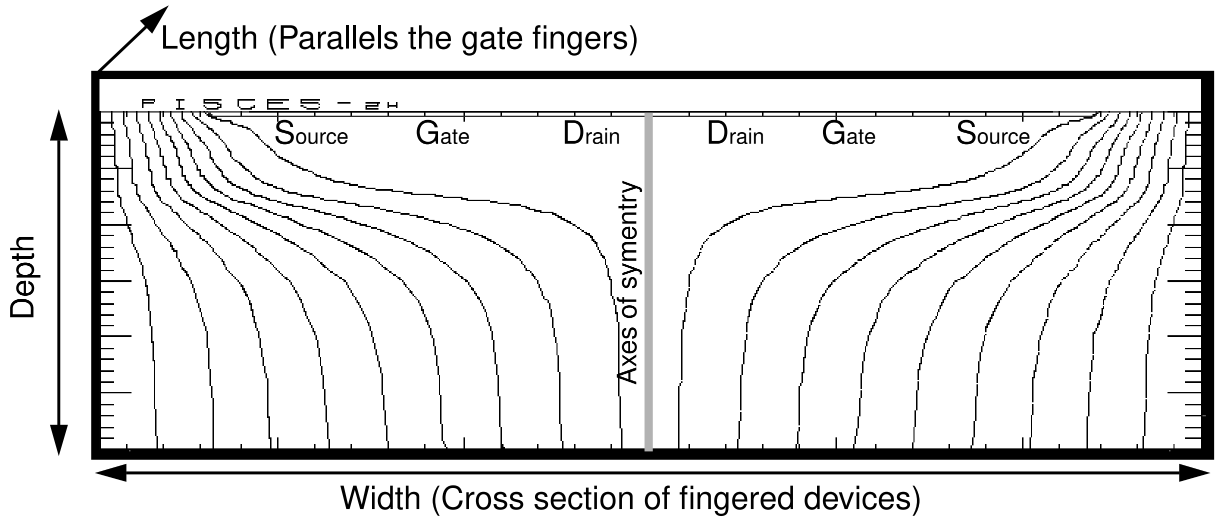


Figure 4: Current flow lines through the P+ sinker and the substrate of an LDMOS device with a backside contact.

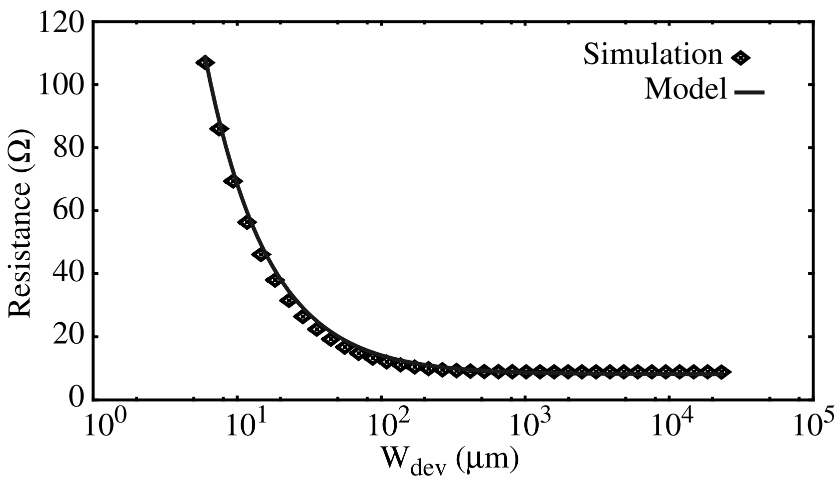


Figure 5: Source resistance as a function of device width.

$$R(W_{dev}) = \frac{1}{L_{snk}}\left(\frac{D_{snk}}{W_{snk}} + \frac{D_{sub}}{W_{max}} + \frac{D_{sub}}{W_{dev}}\right)\frac{1}{\sigma} \qquad (3)$$

where L_{snk} is the length of the sinker along the surface, W_{snk} is the width of the sinker along the surface, D_{snk} is the depth of the sinker (contacts the substrate through the P- epi layer), D_{sub} is the thickness of the substrate, W_{max} is the maximum spreading of current in the substrate, W_{dev} is the width of one device (i.e. abscissa) and σ is the substrate conductances which is considered valid for the sinker (If the conductance is significantly different then the sinker and substrate would have to be divided by their respective individual conductance values).

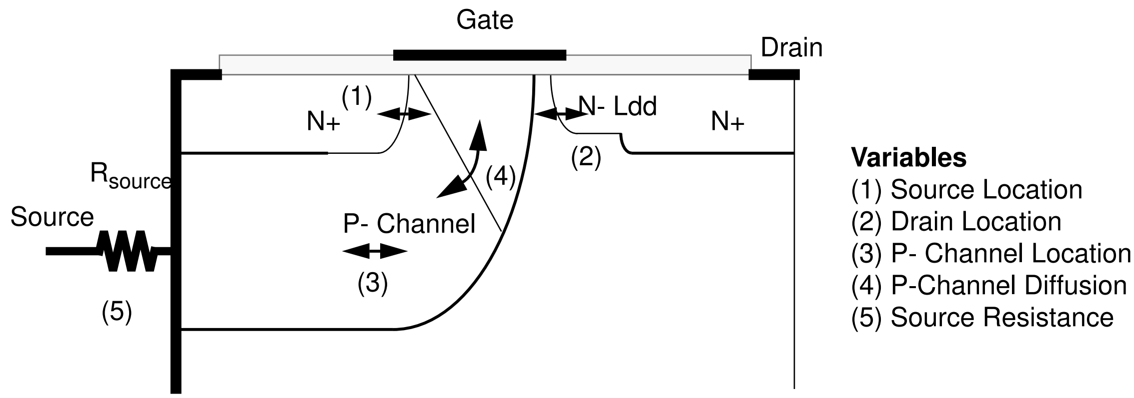


Figure 6: DOE to determine optimum 2D doping profile.

Measuring one sinker as an independent unit, yields a resistance of 8Ω. The simulation model predicts a slightly higher resistance of 8.5Ω. When device confinement is included in evaluation of the source resistance, one device sees a source resistance 46Ω. Thus, as the size of the devices are scaled, the source resistance must be reduced appropriately so as not to degrade performance due to an increase of this parasitic component.

The second key modeling region of interest is the graded channel. Only one dimensional doping profiles are simulated and calibrated with the measured data; however, the profiles must be expanded into two dimensions in order to generate the channel region of the device. The methodology chosen for this calibration is based upon design of experiments (DOE) [17]. Key PISCES parameters describing the two dimensional spreading of doping profiles are varied based upon manufacturing tolerances (Figure 6) [18]. The parameters to be varied are: the inner edge of the source and drain relative to the gate poly (1 and 2 in Figure 6); the edge of the P- Channel implant relative to the edge of the gate (3 in Figure 6); the curvature of the P- Channel region under the gate (4 in Figure 6); and the source resistance (5 in Figure 6). The fitting of the source resistance allows for a comparison of the predicted source resistance with that from the model for the source resistance.

A factorial experiment with the five variables limited by the processing characteristics was run and a statistical model was developed. Three independent statistical dependences relate the threshold voltage, transconductance, and sub-threshold slope (i.e. all three being responses) to the process variables. Simulated parameters are determined (i.e. measured "virtually") using the same methods as in the lab experiments. Upon generating a statistical model for each of the responses, they are used to determine the optimum set of parameters. The results of that optimization are shown in Figure 7 where simulated and measured I-V characteristics are presented.

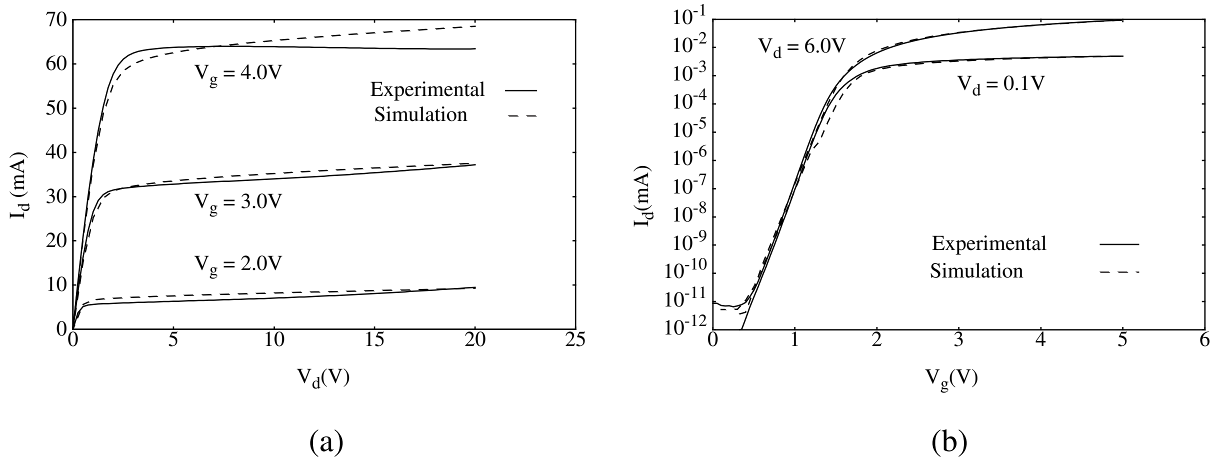


Figure 7: Comparison of simulated and measured I-V characteristics for LDMOS device.

In addition to calibrating the intrinsic LDMOS model, the statistical models may be used to do sensitivity analysis. Sensitivity analysis gives the design engineer understanding of the degree to which a parameter affects the device performance and is useful for optimizing the next generation of the technology.

In this work, RF power devices are optimized to transmit large signals where signal spikes can generate significant heating[1]. As a result, the device can exhibit a negative differential resistance as is apparent in the measured drain characteristics shown in Figure 7a. The application for which this device is targeted does not require its operation in the region of high currents; thus the exclusion of self-heating effects should not affect the results at low power levels and the error is less than 10% at high power levels.

Having calibrated and characterized the DC response, small signal analysis can provide a detailed understanding of device operation. The standard C-V characteristics are simulated under the same conditions as use in measurements. A DC value is swept while AC perturbations are applied to one contact. The AC current is obtained and the capacitance is computed from the imaginary part of the simulated admittance (y-parameters).

1. Future application of this modeling technique requires two important additions in the model. With increasing power densities, self-heating becomes important and thus the model will require that the lattice thermal diffusion equation be solved simultaneously with the semiconductor equations[19]. In addition, breakdown will limit the high power operation thus requiring the modeling of impact ionization for devices operated in that region [20][21]. Both of these effects are computationally complex [1] and require improvements in harmonic balance solution techniques[9].

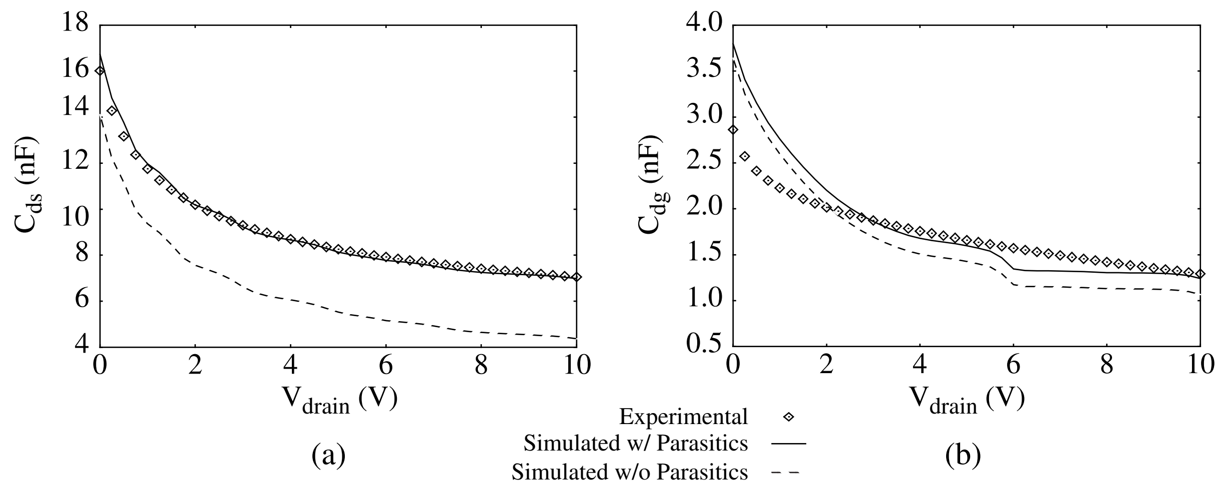


Figure 8: Measured and simulated capacitance for C_{dg} and C_{ds}.

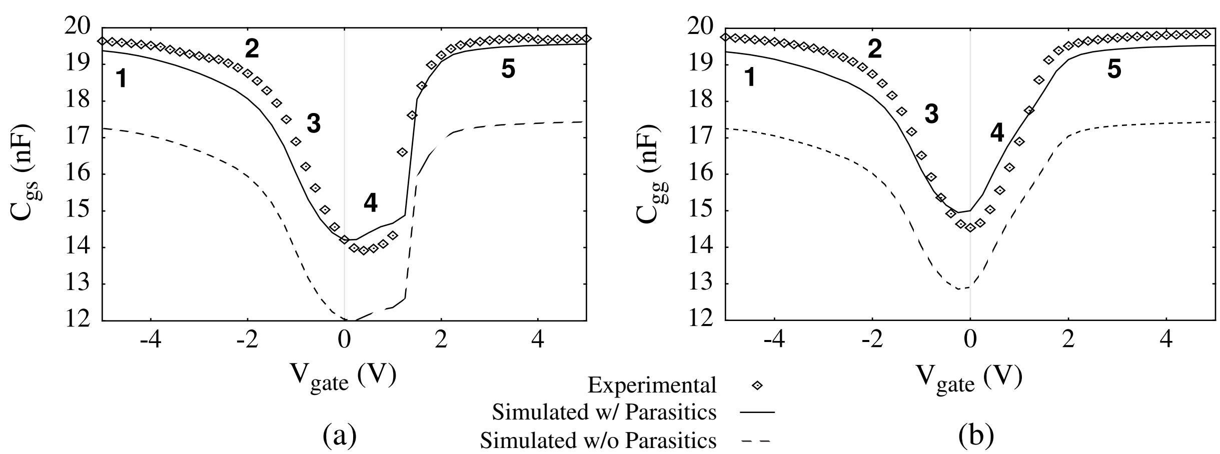


Figure 9: Measured and simulated values for C_{gs} and C_{gg} to allow for analysis of graded channel region.

Figure 8 and Figure 9a show the standard C-V plots for C_{dg}, C_{ds}, and C_{gs} measured at 1MHz; the plots show small signal characteristics with and without parasitics. Since specific parasitic components affect each curve independently, their values are adjusted from their initially computed values. For example, the pad impedance can be computed from a one dimensional PISCES simulation of the structure.

In addition, the C-V measurements can provide detailed information about the channel region. Figures 9a and Figure 9b shows two forms of measurements for C_{gs} (drain floating) and C_{gg} (drain & source grounded) respectively. Starting with a negative V_{gs} in Region 1, the channel is in accumulation. With increasing V_{gs}, the drain side of the device enters depletion; the source side is

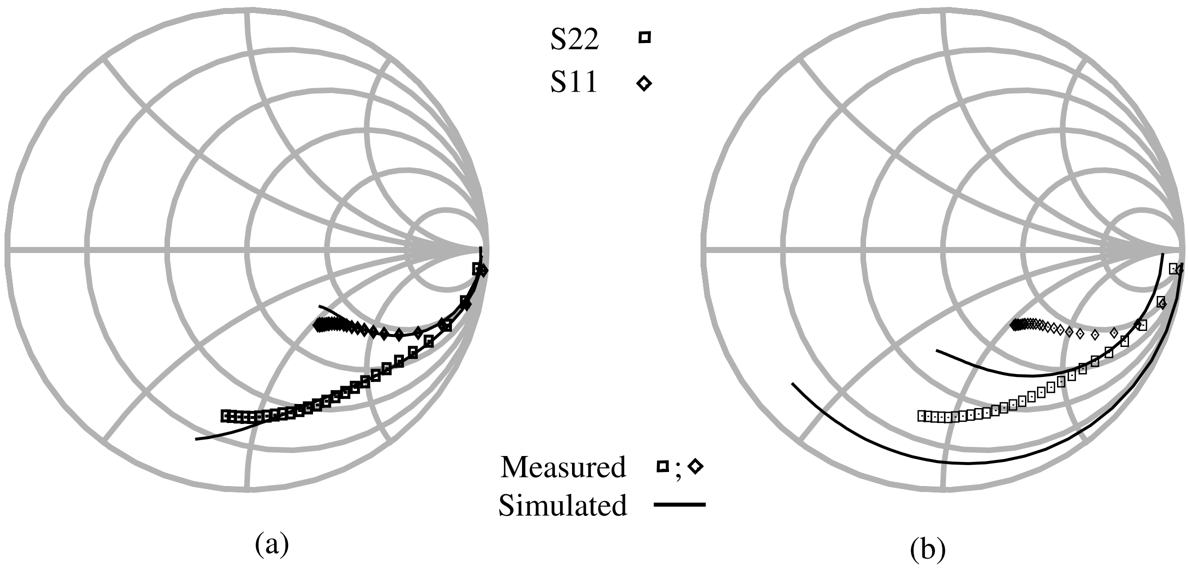


Figure 10: LDMOS impedances looking into the device (a) with and (b) without parasitic components.

in accumulation; and the center of the channel is at flat-band for tens of millivolts (Region 2). As the gate voltage continues to increase the depletion layer reduces the capacitance until around V_{gs}=0V (Region 3). At this point the drain side of the device enters inversion (Region 4). When measuring C_{gs} there is no current path through the drain side inversion layer and the capacitances stays low. When measuring C_{gg} there is a drain inversion by-pass capacitance in parallel with the source side depletion capacitance. Since the inversion capacitance is large and the inversion layer moves across the channel from drain side to source side; the net capacitance measurement increases with voltage as the inversion layer moves across the channel. When the source side of the channel inverts, C_{gs} immediately switches to the inversion capacitance whereas the C_{gg} had slowly approach that value. Pieracci etal. have used this property of the graded channel device in order to estimate doping profile based upon the incremental threshold voltage [22].

S-parameters provide an evaluation of the high frequency accuracy of the model. Because of the difficulty in measuring the full multi-cell device, a single cell of the structure is measured and compared to a single cell model. The device is biased under the typical conditions for its targeted application. The measured S-parameters match the simulated S-parameters up to about 6GHz which encompasses up to the 7th order harmonic for the 850MHz application. Figure 10 and Figure 11 show that the parasitic components contribute significantly to the impedances looking into the device and lead to a degradation in the small signal gain of the structure. Hence, layout

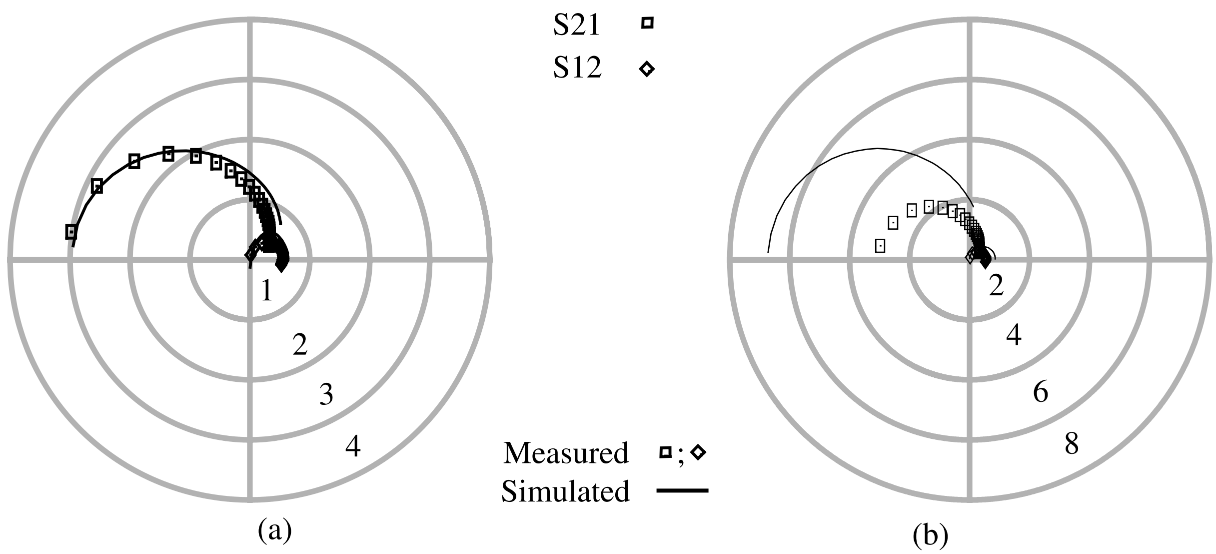


Figure 11: LDMOS gain (a) with and (b) without parasitic components.

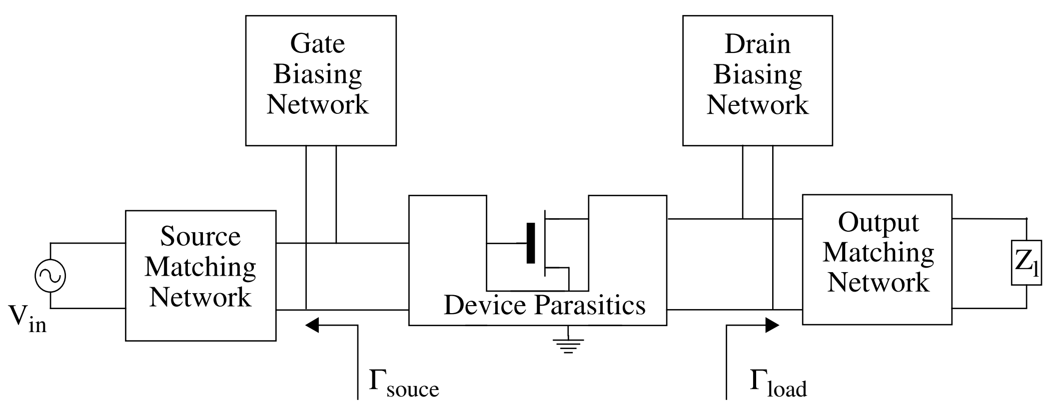


Figure 12: Configuration of a power amplifier. The biasing networks set the load lines and the matching networks provide for transfer of RF power.

optimization and reduction of parasitic components is a key design factor in developing next generation technology.

IV. Evaluation of Device RF Performance

The previous sections described how the intrinsic device simulation and parasitic analysis can be used to better understand performance trade-offs. In this section, the model is used to evaluate RF performance for the measurement set-up shown in Figure 12. The RF performance gauges include the transducer gain (G_t), power added efficiency (PAE), and inter-modulation distortion (IMD).

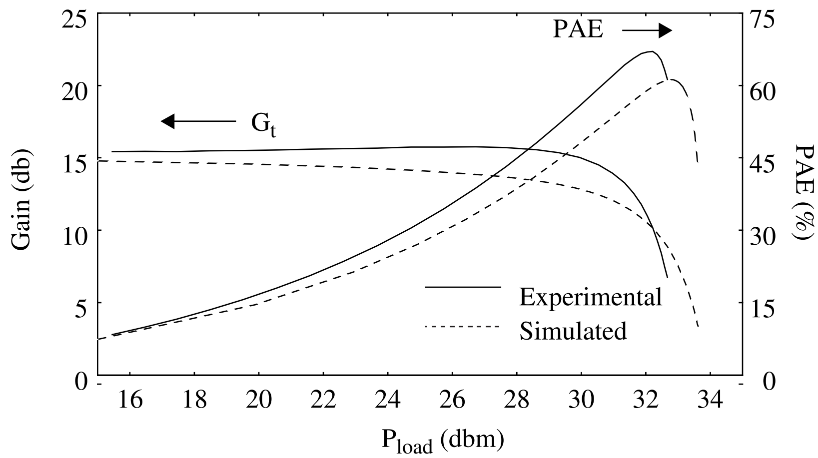


Figure 13: Simulated and measured RF responses for gain and efficiency of a power amplifier.

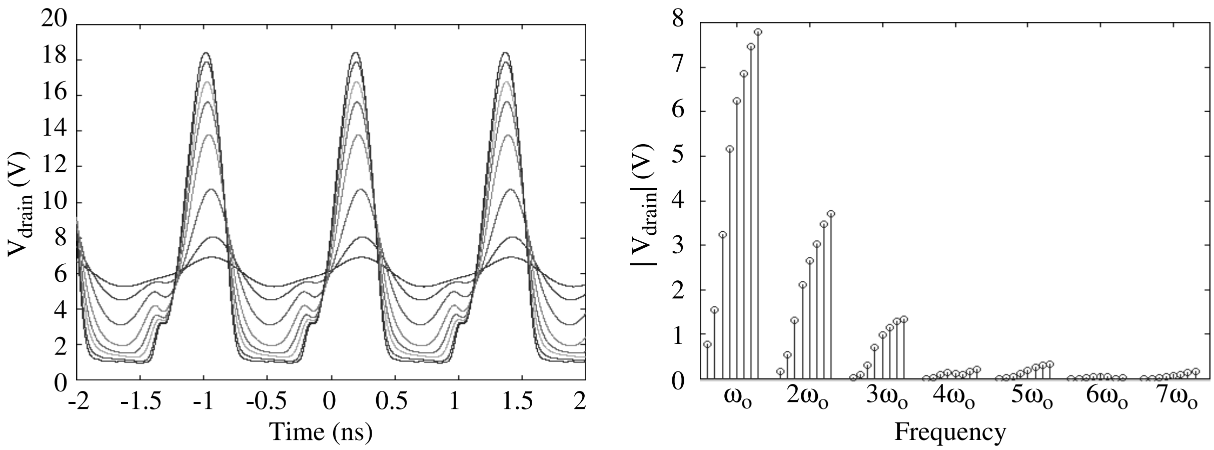
For single tone harmonic distortion analysis, a large signal sinusoid is applied at the input to the power device (V_{in}) and the steady state large signal response is computed numerically. The transducer gain and power added efficiency characterize the performance of the device. The gain is given by

$$G = 10\log\left(\frac{P_{avs}}{P_{load}}\right) \tag{4}$$

which takes the ratio of the output power delivered to the load and the power available from the source (P_{avs}). The power added efficiency gives the percentage of power that goes into amplification of the signal and is given by:

$$\text{PAE} = \left(\frac{P_{load} - P_{avs}}{I_{avg} V_{dc}}\right) \times 100\% \tag{5}$$

Figure 13 compares the simulated gain and efficiency with experimental data for an input frequency of 850Mhz using matching networks optimized for the device application (refer to Section V). The gain and efficiency are plotted versus the output power (P_{load}) since the power amplifier has to meet a minimum output power specification for the cell phone industry standard. The gain at low power is equivalent to the small signal gain. At an input power of -30dbm, the simulated response of 15.1db agrees well with the measured response of 15.4db. The gain rolls off at higher power levels because the device operates in g_m compression and the output power is limited by the saturation current. The efficiency is low for small P_{load} because the device drains



(a) (b)

Figure 14: (a) Time domain signal and (b) frequency spectrum of the drain voltage in an harmonic distortion large signal sinusoidal simulation. The larger magnitude of the signal indicates increasing power along the gain curve.

more power due to Class A operation. Efficiency increases until just after the gain starts to roll off. At this point, P_{avs} approaches P_{load} resulting in very little power added to the input signal.

Although the curves differ depending on the specific region of operation, the two results show an over good agreement consistent with several factors that can affect the results. The strongest influencing factor is that of the matching networks. The matching networks used in the simulation are those determined experimentally by a load-pull system. (Section V discusses simulated load-pull analysis.) In spite of a good match for the I-V and C-V characteristics this matching network is optimized for the manufactured device used in the measurement with all of its inherent process variations and not the specific device in the model[2]. In addition to the matching network, the gain roll-off is associated with the edge of the linear and saturation region as the device enters g_m compression (i.e. high drain current and high gate voltage). Under this condition, the device exhibits self-heating thus causing degradation in performance. As stated previously, the simulator neglects these self-heating effects and over predicts the performance by about 10%.

Using the results of the harmonic balance device simulation, it is possible to examine the signals in the time domain as well as their associated spectra. Figure 14 shows the drain voltage in both the time domain and the frequency domain for increasing power. At low voltage levels the device

2. In actual power amplifier circuits, it is often necessary to provide a variable resistor or capacitor on the circuit board to provide for tuning of the matching networks and other resonant circuits in order to meet the manufacturing specifications.

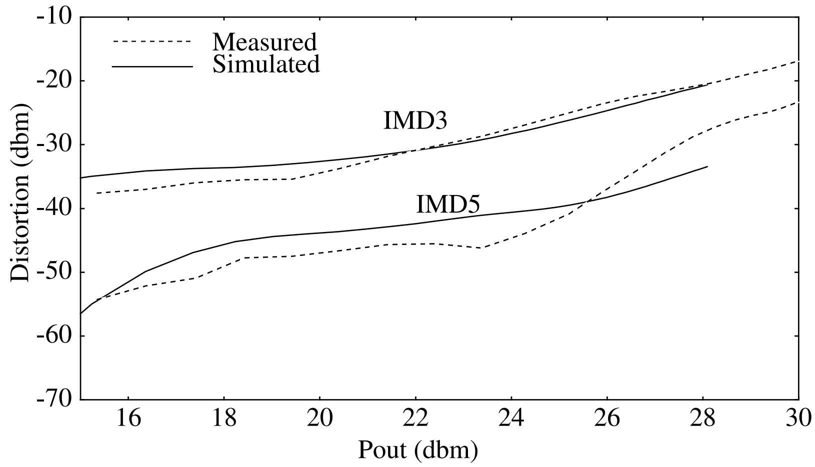


Figure 15: Simulated and measured inter-modulation distortion of the power amplifier.

operates in Class A. As the power level increases, the voltage cannot swing below threshold and thus enters Class AB operation. As the power level continues to increase, the drain voltages is limited by G_m compression and thus upper swing becomes limited. The spectrum exhibits this effect as higher order frequency components become more apparent.

Inter-modulation distortion (IMD) provides a way to characterize linearity of the device when two closely spaced tones are applied in the frequency domain. Harmonics are not only created at multiples of the frequencies, but also at integer sums and differences of the frequencies. This leads to the generation of an harmonic in the base band which can not be filtered. The amount of IMD is characterized by computing the ratio of power in the generated harmonics referenced to the fundamentals.

Using an 8th order simulation, the inter-modulation distortion for the 3rd order and 5th order harmonics are computed for simulation frequencies of f_1=851MHz and f_2=849MHz. The simulated results are compared to experimental data in Figure 15, showing good qualitative and quantitative agreement.

V. Predictive Analysis and Optimization

Having verified the RF performance of the physical model, it is now possible to use simulation to evaluate performance in design variations and process control. Since parasitic components are important in the device performance, this section examines those components through process variations and the matching networks required for optimum power transfer.

Knowing which parasitics have the largest impact on the performance can lead to judicious selection of the parasitics for subsequent design optimization. A DOE is used to analyze the impact of three components at their high and low values as observed in manufacturing. R_g is selected because it is determined by the silicide processing step and hence, can be adjusted. C_{gs} is related to the Faraday shield of the device and the value of L_s (source inductance) is difficult to model physically due to back-side contact effects.

The effects of the parasitic components on gain and efficiency are shown graphically in Figure 16. The general effects of the parasitic components on the amplifier performance are apparent, but the important observations come from the degree to which these parasitics affect the performance. In the gain curves, both R_g and L_s have a similar impact within the limits chosen for these parameters. When both parameters are at the high level, the gain is the lowest and likewise when both are at their low levels, the gain reaches its highest value. When one increases and the other decreases, very little improvement is observed. C_{gs} has only a minor impact on the gain and "modulates" the curve about the solution established by R_g and L_s. The efficiency curves clearly show that the strongest effect can be attributed to the gate resistance. C_{gs} has the next strongest effect and L_s has the least impact on performance.

In addition to the parasitics components considered above, an RF device engineer can also modify the intrinsic device structure to address improvements as technology evolves. Sato-Iwanga has shown how using a similar modeling approach, the inter-modulation components of a MESFET is studied[23]. Jang shows the importance of mixed circuit and device simulation for RF performance analysis of BJT's[24].

Gain, efficiency, and linearity are affected by the matching networks in the circuit. An application for this device requires that gain meets a minimum specification and efficiency is maximized for that application. Input and output matching networks have limited interactions with each other and are thus tuned independently. The input matching network is tuned to minimize reflections back to the signal source using a best guess for the output matching network. To determine the best output matching network, the reflection coefficient looking towards the load (Γ_{load} in Figure 12) is varied by sweeping the load across a range of values where the best response is expected (i.e. a load-pull)[25]. For each matching network, the gain and efficiency are measured for a constant input power of 20dbm and plotted over the range of the network's reflection coefficients.

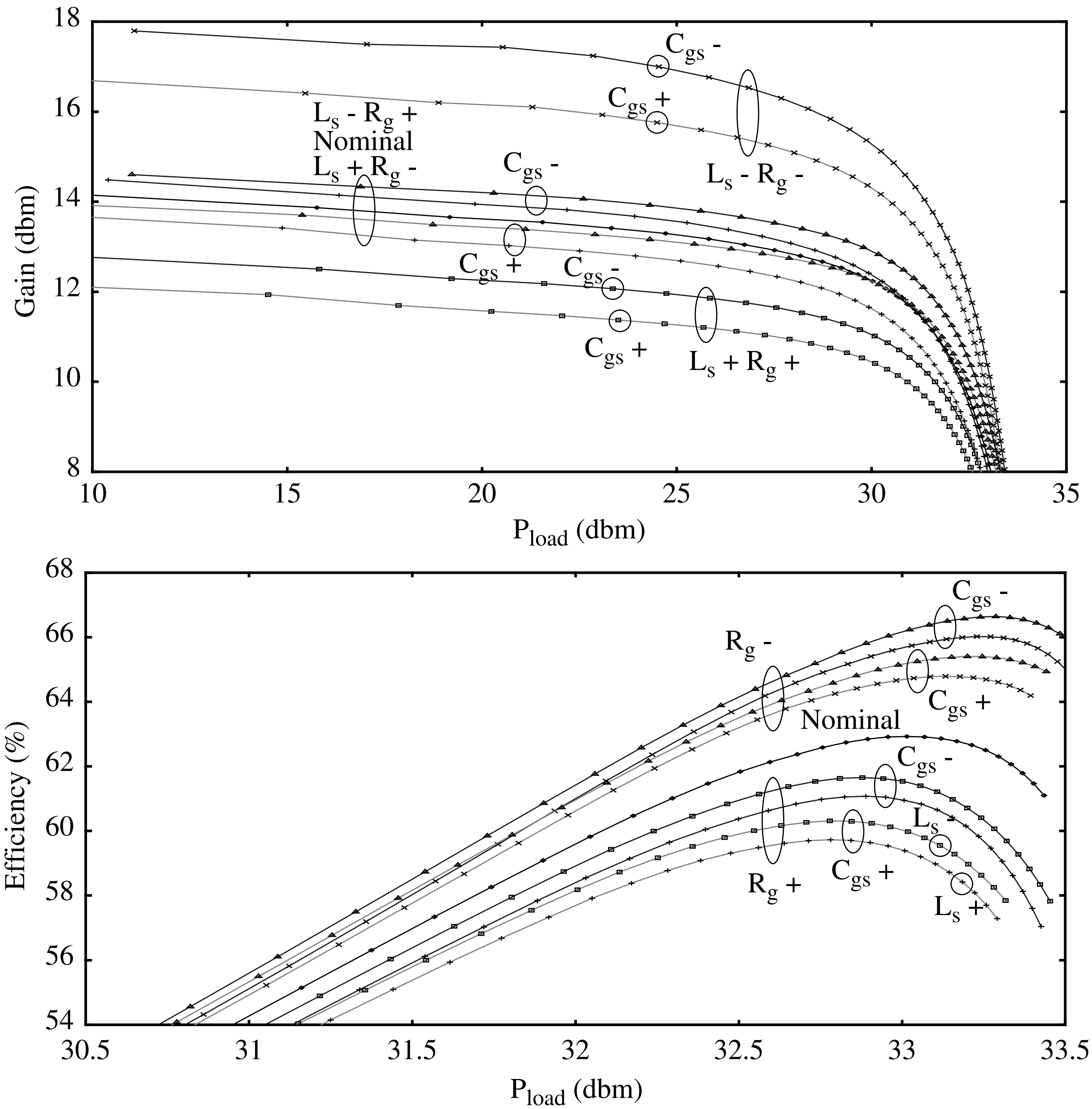


Figure 16: Simulated effects of parasitic components on the gain and efficiency of the LDMOS device. The "+" and "-" indicate whether the variable is at it's manufacturing high or low value.

Figure 17 shows experimental contour plots for gain and efficiency on a Smith chart which is used to represent the different reflection coefficients. (Note that the impedances on the Smith chart are normalized to 10Ω rather than the standard 50Ω to obtain greater visibility.) The white point on the graph indicates the matching network used to generate the earlier plots of gain and efficiency. The selection criteria for this point depends upon the application for the device. The alignment of

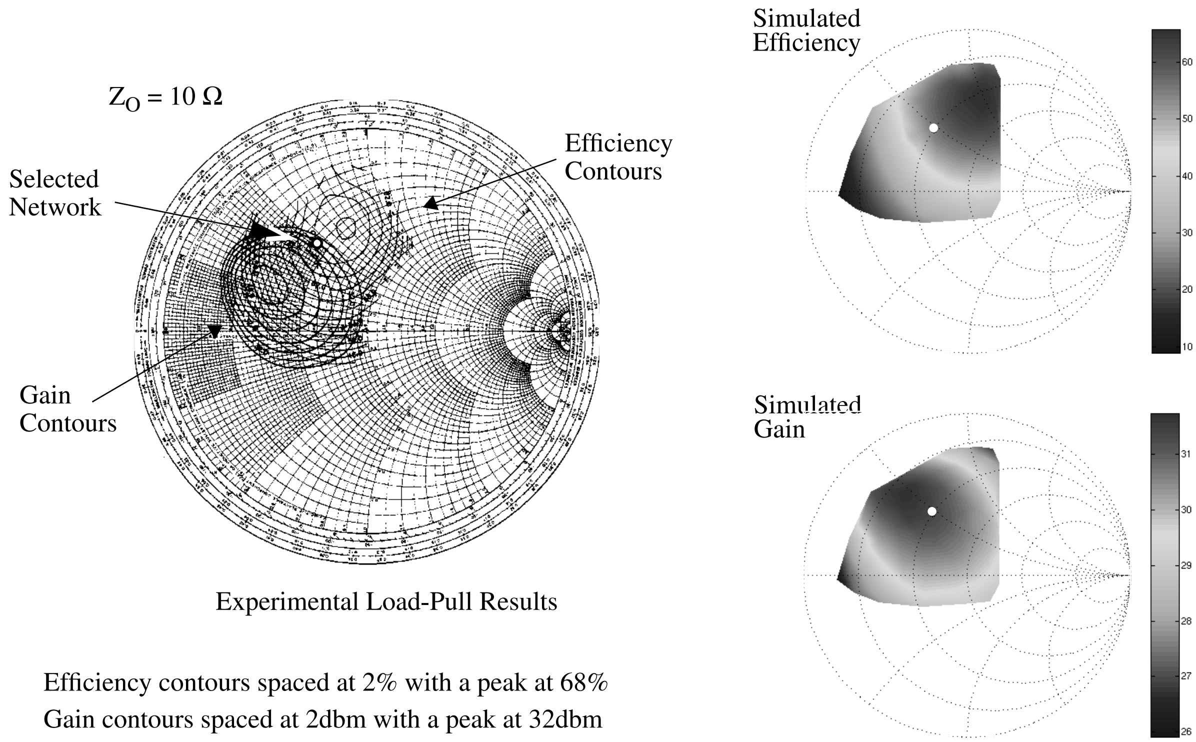


Figure 17: Comparison of experimental and simulated load-pull analysis. The darken point represents that matching network used in the earlier RF response.

the maxima and the shape of the contours demonstrate that the simulated results (Figure 17) agree with the experimental data.

There are some important criteria for load-pull simulations. Load-pull equipment is designed to optimize the impedance for a specific reflection coefficient given that it can be realized by different combinations of physical components. In simulation the matching network is specified with physical components based upon the layout of the fixture for the application in which the device is utilized. If the physical components are chosen poorly, reflections back into the device or filtering may affect the performance of the device through higher order harmonics. Hence, care has been taken so that the choice of components maximizes the performance of the device for a given reflection coefficient of the output matching network.

VI. Conclusions

This paper discusses the modeling, analysis, and design of LDMOS transistors using advance device simulation. Improvements to PISCES tool allow for large signal steady state analysis (harmonic balance) and the inclusion of parasitic components in those simulations. The LDMOS structure is modeled and calibrated based on I-V and C-V data. This analysis also leads to a more detailed understanding of the underlying device performance and physics. With the calibrated model, RF performance curves for large signal gain, efficiency, and linearity of the LDMOS model are verified. This paper presents a number of simple design examples yet the methodology employed can be easily expanded to more critical design analysis and ultimately support shorter design cycles.

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